12 Channel HVA Board

Hardware Design and Test Document

Rev. 1.5

Revision History

Date	Rev	Author	Comment
10/29/02	1.1	Rob Yamashita	Initial Document
12/10/02	1.2	Rob Yamashita	Fixed DAC Test and High Voltage Amplifier Test Procedure. Added Table of context
2/10/03	1.3	Rob Yamashita	Fixed dip switch settings in test procedure and in manual address selection
2/11/03	1.4	Rob Yamashita	Created PDF and added datasheets.
2/24/03	1.5	Rob Yamashita	Added rework instructions

1 12 Channel HVA Board

1.1 Overview

The 12 Channel HVA board is used drive piezo material on a telescope. Each channel can swing the voltage from -400V to +400V. Each channel on the board is individually addressable through one of two DAC on board. Dip switches set the upper three address bits for the board allowing the address range on the board to go from 0-95. This makes it possible for 8 boards to be placed in one chassis, while still allowing each channel to be addressed individually.

1.2 Technical Specification

- **12 individual High Voltage Amplifier channels**
- **+/-400 Volt Output Range**

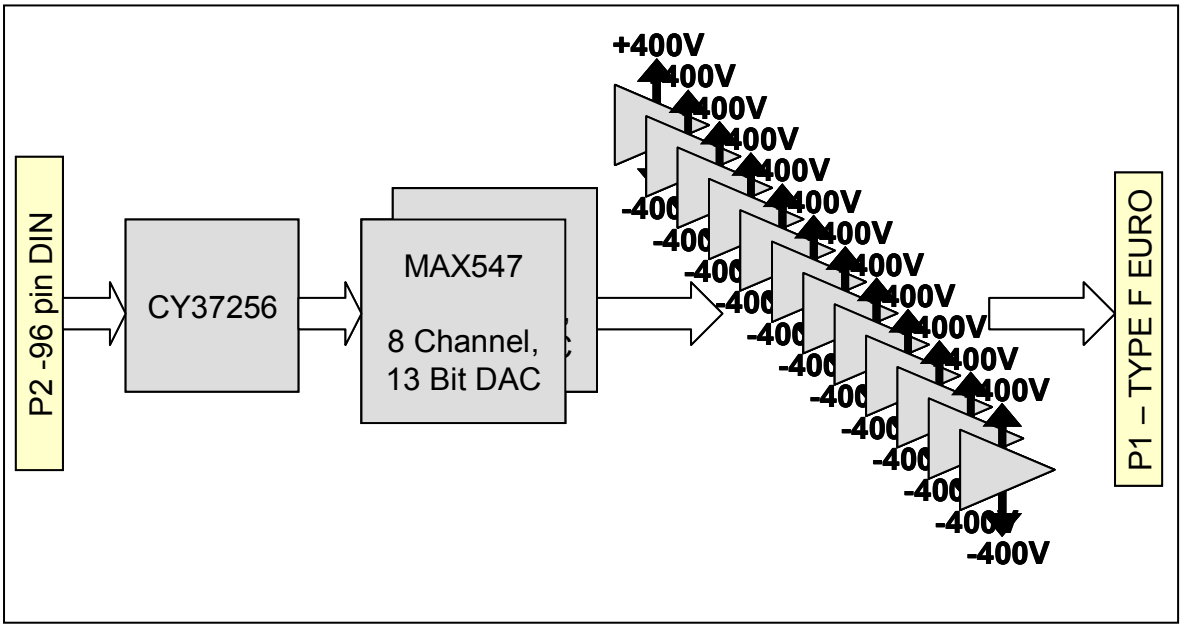
Power Requirements

- **+5V ≈ 2.5A**
- **-5V ≈ 80mA**
- **+15V**
- **-15V**
- **+400V**
- **-400V**

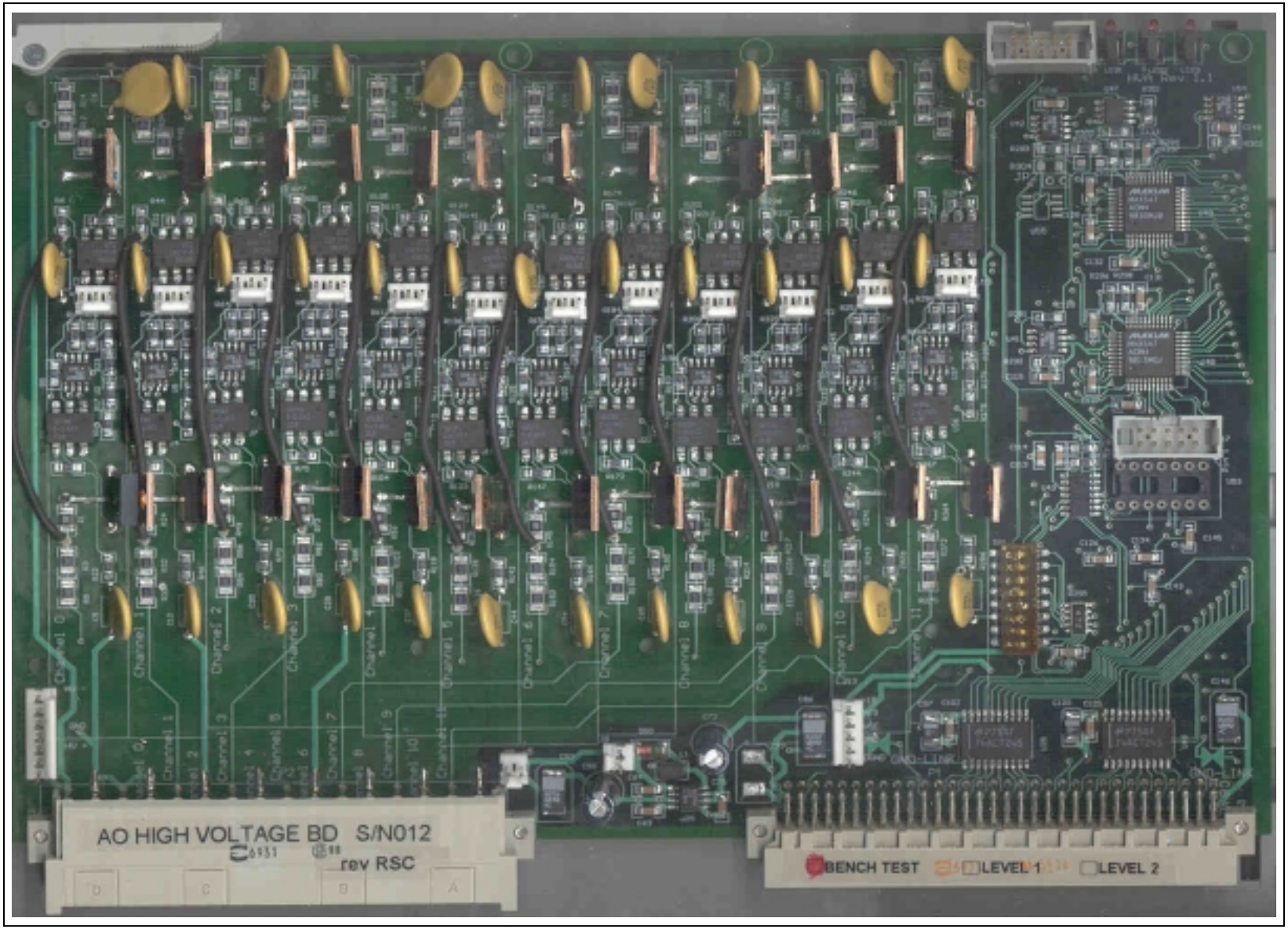
1.3 Mechanical Specification

- Eurocard 6U (160mm x 233.35mm) Form Factor
- P2 96 pin DIN Connector
- P1 32 pin TYPE-F-EURO
- 4 Layer PCB construction

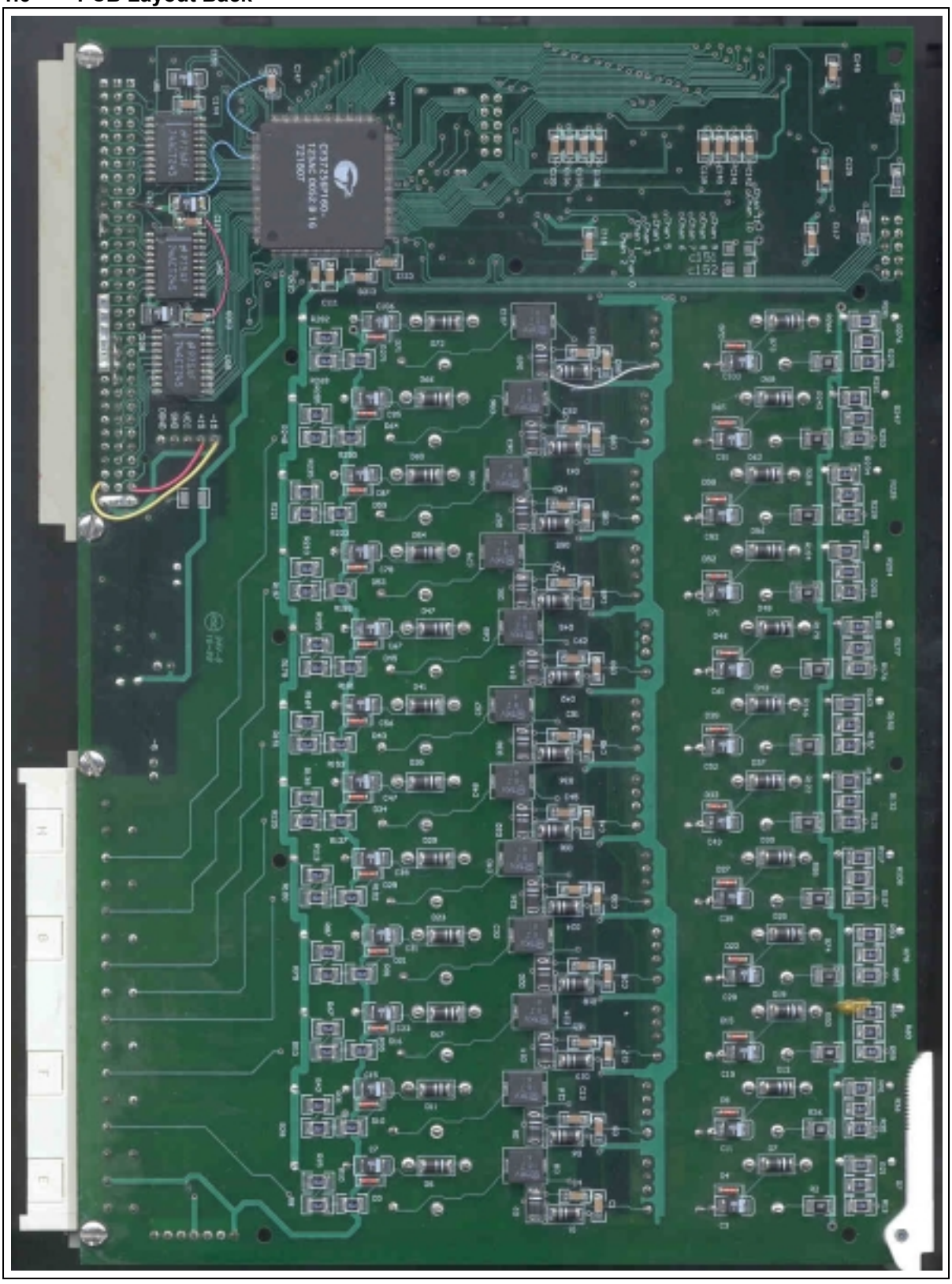
1.4 Block Diagram



1.5 PCB Layout Front

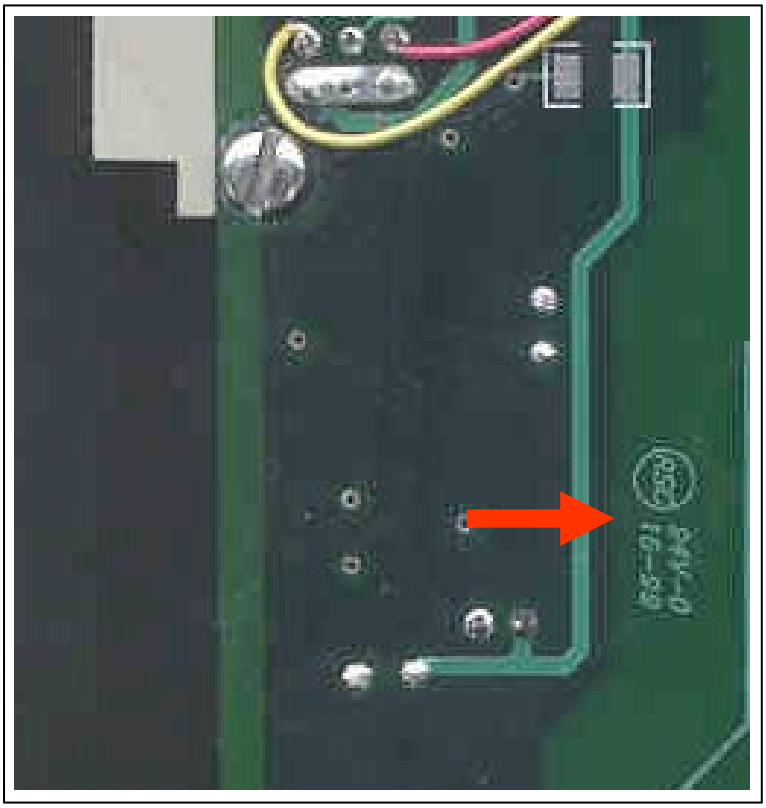

AO HIGH VOLTAGE BD S/N012
rev RSC
BENCH TEST
LEVEL 1
LEVEL 2

1.6 PCB Layout Back



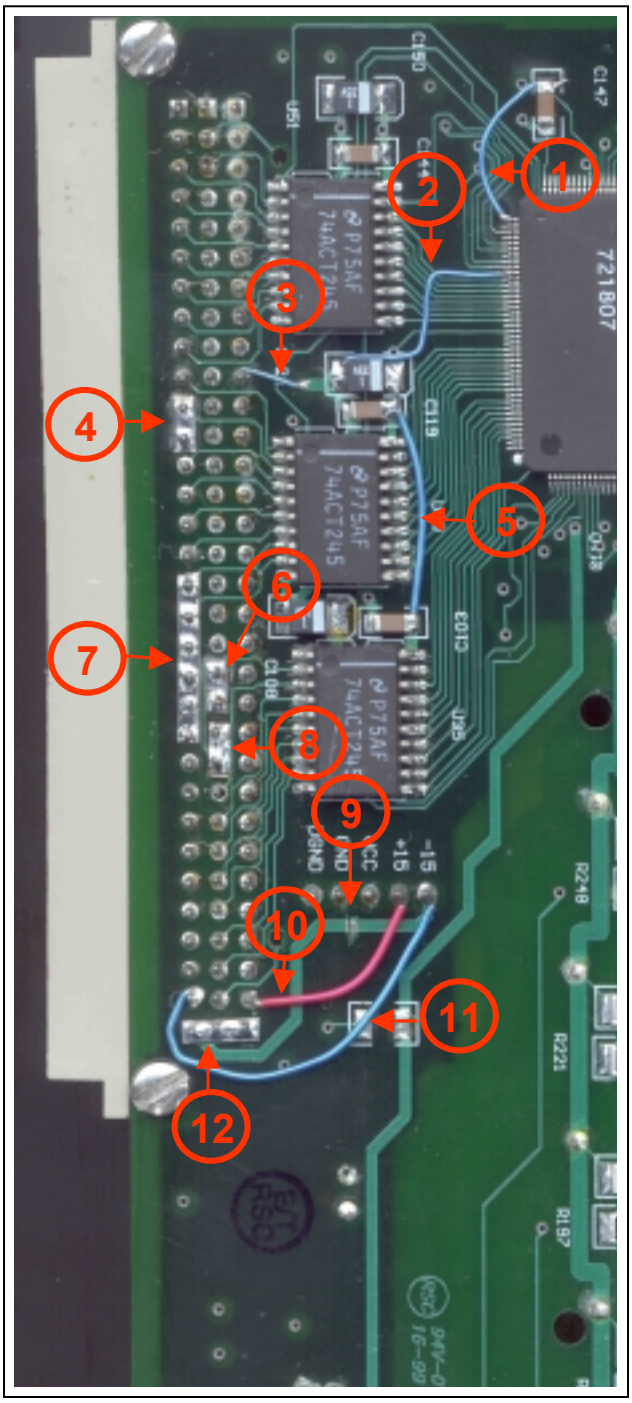
1.7 Rework Instruction

This rework instruction is for board with the marking pointed out by red arrow in picture below.

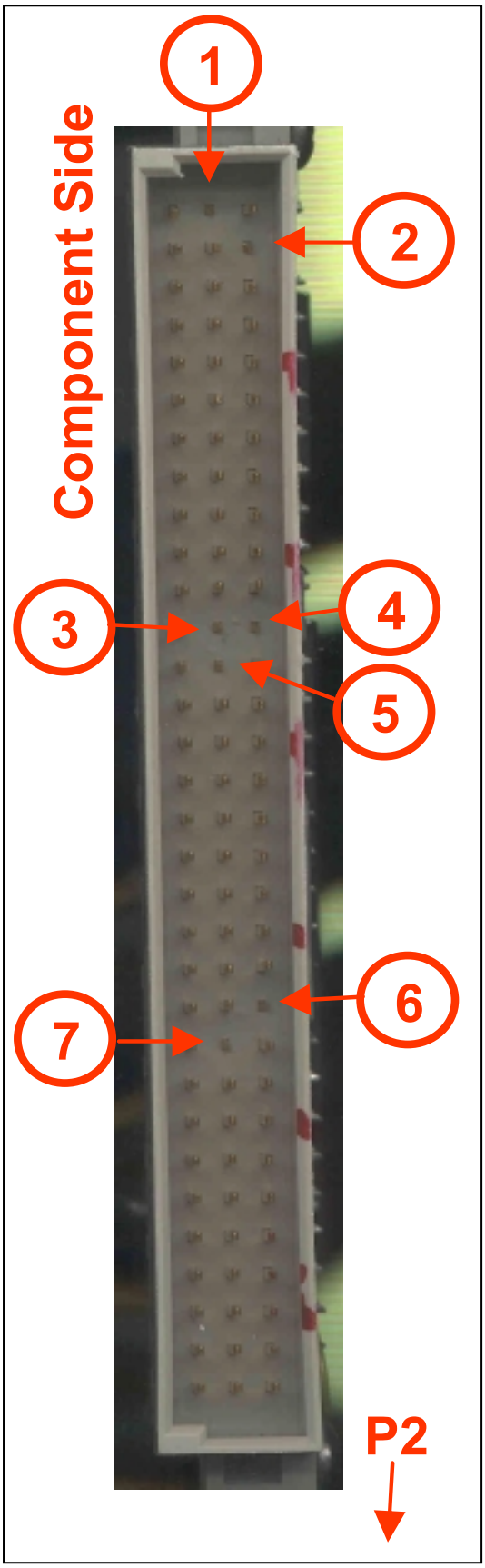


The following picture displays all of the rework required on the front of the PCB.

The following picture displays all of the rework required on the back side of the PCB.



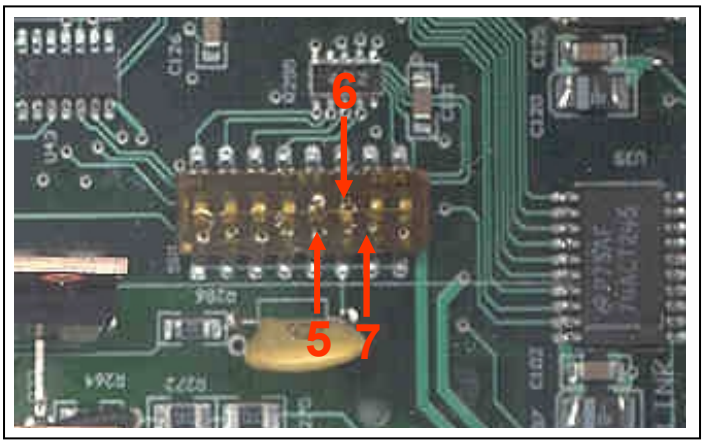
The following picture shows the pins that need to be cut off of connector P1.


Component Side
1
2
3
4
5
6
7
P2

1.8 Manual Address Range Select

- Switches 5-7 set upper address bits

Switch			Address Range
5	6	7	
ON	ON	ON	**0-11**
OFF	ON	ON	**12-23**
ON	OFF	ON	**24-31**
OFF	OFF	ON	**32-47**
ON	ON	OFF	**48-59**
OFF	ON	OFF	**60-71**
ON	OFF	OFF	**72-83**
OFF	OFF	OFF	**84-95**



2 Test Procedure

2.1 High Voltage Amplifier Low Voltage Bench Test
High Voltage Amplifier Channel Low Voltage Bench Test

Requirements

Function Generator
Oscilloscope, 2 channel
DC Power Supply with 5V, 15V and -15V outputs
Cables to connect power supply and Function generator to board

Procedure

2.1.1. Set up Function Generator to create a square wave with a 4ms period and amplitude +/-200mV.
2.1.2. Connect power supply GND to J13 pins 1 and 2, +5V to pin 3, +15V to pin 4 and -15V to pin 5.
2.1.3. Also connect +15V to J1 pin 7 and -15V to pin 1.
2.1.4. Turn on power supply.
2.1.5. Connect output of Function Generator to J2 pin 3 and GND from the Function Generator to pin 1.
2.1.6. Also connect the output and GND from the Function Generator to channel 1 of the Oscilloscope.
2.1.7. Connect the GND from the second channel of the Oscilloscope to J1 pin 4 and probe R9 pin 2(side closest to P1).

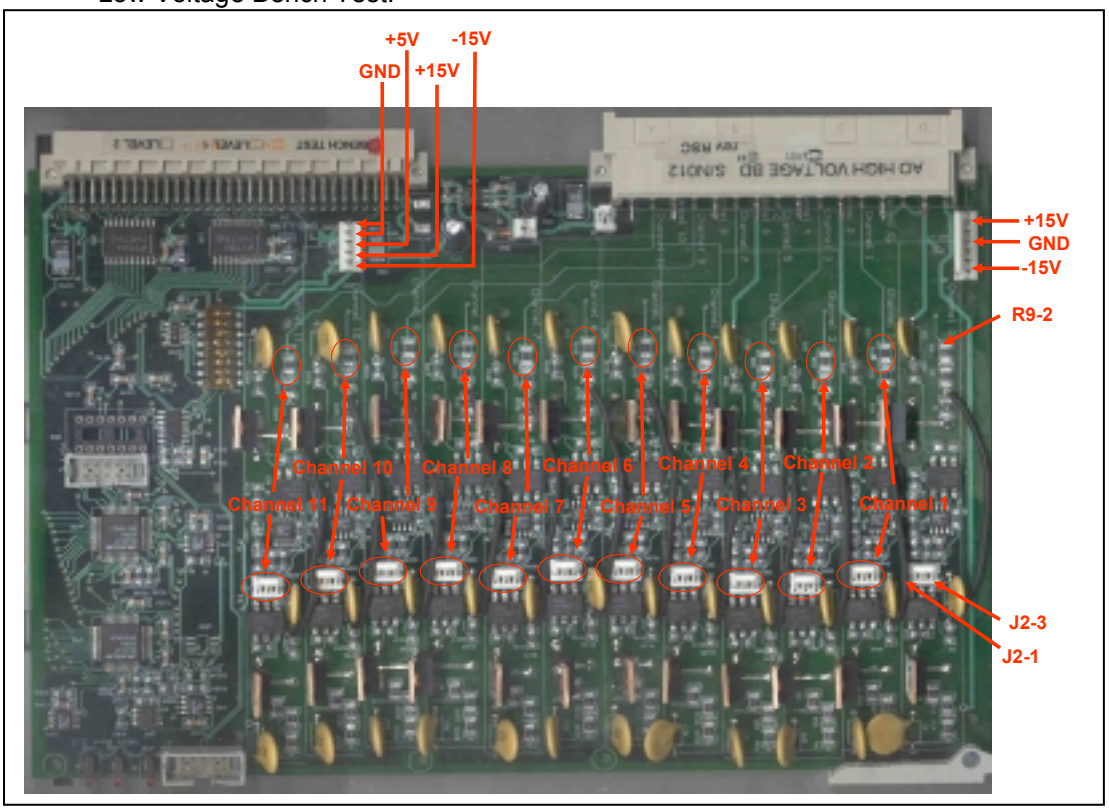
Check to see that

a. Waveform on channel 2 of the Oscilloscope swings from -15V to +15V.
b. Waveform on channel 2 of the Oscilloscope is 180° phase shifted version of channel 1.
c. Transitions are fast and not rounded at the top.

2.1.8. If any of the above criteria are not met, channel fails test. Keep track of board Serial Number and channel for debugging later.

2.1.9. Repeat steps 5-9 using corresponding connector in step 5 and corresponding resistor in step 7 for each of the channels.

2.1.10. If all channels pass testing, board has passed High Voltage Amplifier Channel Low Voltage Bench Test.



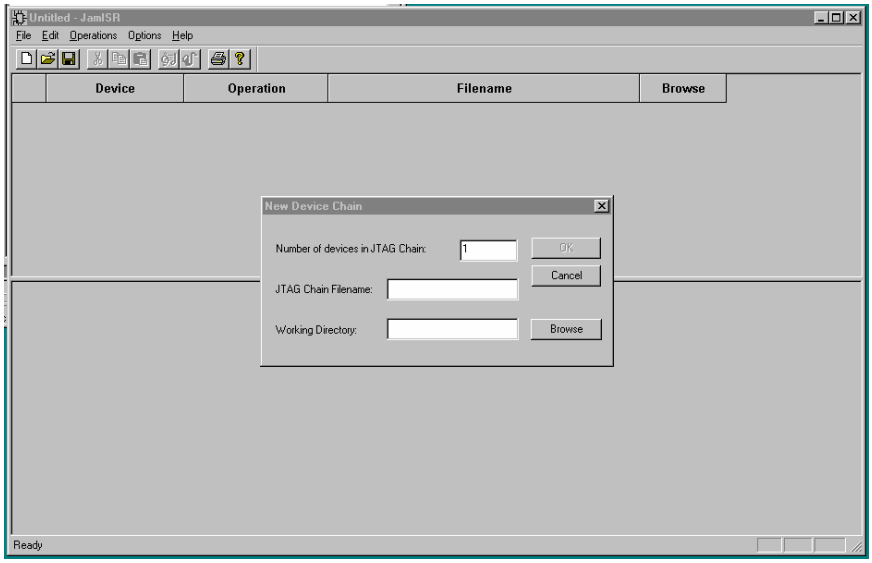
2.2 CPLD Programming

Requirements

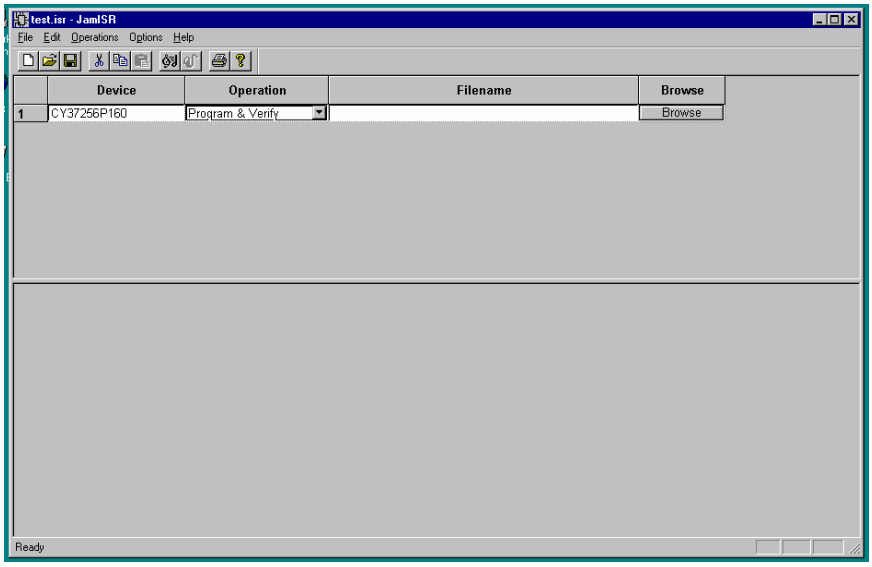
Cypress ISR programming software
Cypress UltraISR programming cable
5V power supply
Programming file – hva.jed

Procedure

1. Plug Cypress UltraISR programming cable into Parallel port of pc and start Cypress ISR programming software.
2. Select 'New' from the 'File' menu



3. Type ‘1’ in the ‘Number of devices in JTAG Chain’ text box.
4. Type a filename in the ‘JTAG Chain Filename’ text box.
5. Browse and select or type in the directory that you would like to save the programming session in.
6. Press ‘Ok’



7. In the ‘Devices’ box select ‘CY37256P160’.
8. In the ‘Operation’ box select ‘Program & Verify’.
9. Use the ‘Browse’ button to locate and set the path and filename in the ‘filename’ text box to ‘*path*\...\hva.jed’.
10. Press the  button to compose the programming file.
11. Plug 5V power and GND into header J13 pin 5 and pin 1 respectively.

Note: Pin 1 is the pin closest to connector P2.

12. Connect Cypress UltraISR programming cable to header J16. Connector should be polarized, but if not ensure that pin 1 of cable connects to pin 1 of header.

Note: Pin 1 of header is the pin closest to LED1 and the nearest board edge.

13. Turn on power supply.

14. Press the  button to program the CPLD. Programming may take several second to complete
15. Check log that is displayed to see that CPLD programmed and verified successfully.

If programming or verify was not successful-

a. Verify that the path and filename are correct in the 'filename' textbox. If not, repeat from step 9.
b. Check to see that power and ground are connected correctly and that supply voltage is set to 5V DC. If not, repeat form step 11.
c. Check to see that part is correct and it is soldered correctly to board. If not, correct problem and repeat from step 11.

16. Turn off power supply and disconnect cables.

2.3 DAC Test

Requirements

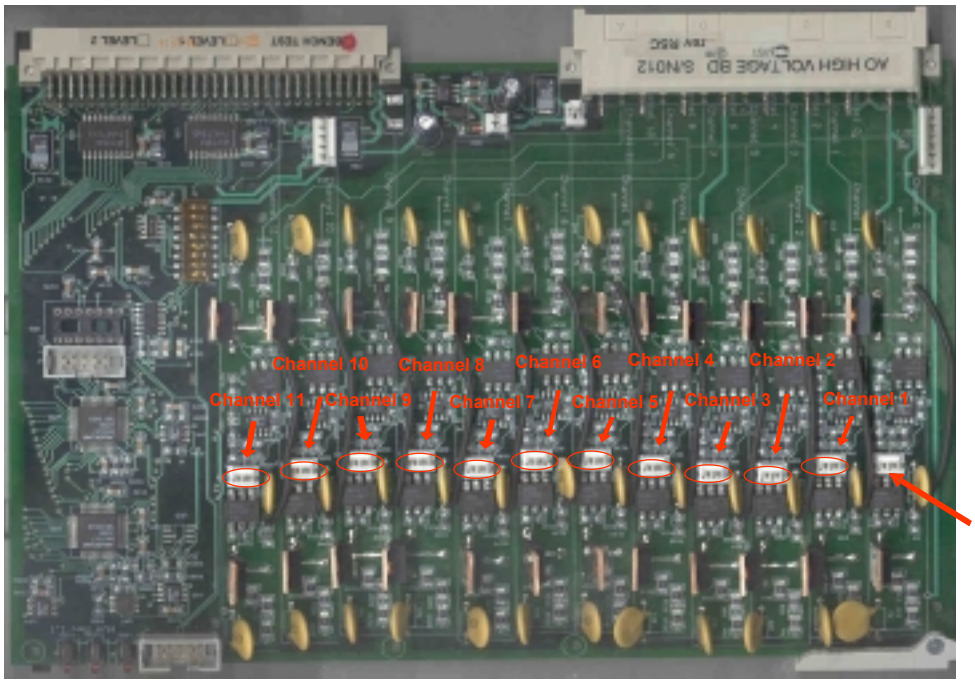
2 Multifunction Boards
1 Chassis
2 PCs with Linux OS
2 FC-FC Multimode Fiber Optic Cables
Oscilloscope

Procedure

1. On AOUIM open 3 Xterm windows
2. In first Xterm window type '**rlogin –l ao aoicm**' and hit return
3. Type the password, '**wai!mea**' and hit return.
4. Change to the '**dio32**' directory.
5. Type '**su aroot**' and hit return.
6. Type the password, '**wai!mea**' and hit return.
7. Type '**start_dio**' and hit return. This should start dio32.
8. In second Xterm window type '**rlogin –l ao aoicm**' and hit return.
9. Type the password, '**wai!mea**', and hit return.
10. Change to '**dio32**' directory.
11. Type '**cat /dev/rtf0**' and hit return.
12. In the third Xterm window, type '**rlogin –l ao aoicm**' and hit return.
13. Type the password, '**wai!mea**' and hit return.
14. Change to the '**dio32**' directory.
15. Type '**cat > /dev/rtf1**' and hit return.
16. You should now be able to see the commands that you type in Xterm 3 show up in Xterm window 2. To test this type '**test**' in Xterm 3. If you do not see 'test' in Xterm 2
    a. Hit '**ctrl-c**' in Xterm 3.
    b. In Xterm 3, type '**exit**' and hit return.
    c. Hit '**ctrl-c**' in Xterm 2.
    d. In Xterm 2, type '**exit**' and hit return.
    e. In Xterm 1, type '**stop_dio**' and hit return.
    f. Repeat from step 7.
17. Make sure that all dip switches on SW1 are in the 'ON' position
18. Plug board that you would like to test into chassis.
19. Connect oscilloscope GND to J2 pin 1 and channel 1 to J2 pin 2.
20. Turn on power by flipping switch on front of chassis
21. In window #2 type 'a i' and hit return.
22. Type '**f a 0**' and hit return to direct commands to channel 0.
23. Type '**f m 1**' and hit return to set the test pattern to sawtooth.
24. Type '**f p 10000**' and hit return to set the period of the pulse to 10000 ms.
25. Type '**f b**' and hit return to start pattern generation.
26. Check the oscilloscope to see a saw tooth pattern is being generated.
    If output stays constant on oscilloscope

a. Turn off chassis power by flipping switch on front of chassis.
b. Wait 5-10 seconds and turn power back on.
c. Check if pattern is being generated.
d. If not repeat a-c 4 times.
e. If still no output, move oscilloscope probe to corresponding connector on channel 2 and type '**f a 1**' and hit return, then repeat steps 21-24.
f. If still no output there may be a problem with the DAC. Turn off chassis and remove board.
g. Check for assembly errors around U48 and U49.

27. Type '**f e**' and hit return
28. Type '**f a** ' and the next channel number, then hit return.
29. Move oscilloscope probe and ground pin to corresponding connector on channel and repeat steps 23-27 until all channels 0-11 have all been tested, noting pass/fail of all channels.



If all channels pass the previous test, continue onto the next test starting from step 28. The next test is to check the addressing of the DAC, to make sure that there isn't any aliasing. If any of the channels failed the previous test go to step 71, debug board and retest.

30. Connect oscilloscope GND to J2 pin 1 and channel 1 to J2 pin 2.
31. Type '**f a 0**' and hit return to direct commands to channel 0.
32. Type '**f b**' and hit return to start pattern generation.
33. Check the oscilloscope to see a saw tooth pattern is being generated.
34. Move oscilloscope GND and probe to the corresponding pins on the connector for Channel 1.
35. Check that channel is NOT outputting the sawtooth pattern. If output remains flat, the channel has passed test.
36. Move oscilloscope to next channel and repeat step 33 until all channels have been tested, noting pass/fail of all channels.
37. Move oscilloscope to channel 6.
38. Type '**f e**' and hit return.
39. Type '**f a 6**' and hit return.

40. Type '**f b**' and hit return.
41. Check the oscilloscope to see that sawtooth pattern is being generated.
42. Move oscilloscope to next channel.
43. Check that channel is NOT outputting the sawtooth pattern. If output remains flat, channel has passed the test.
44. Move oscilloscope to next channel and repeat step 41 until all channels have been tested, noting pass/fail of all channels.
45. Type '**f e**' and hit return.

If all channels pass the previous test, continue onto the next test starting from step 44. The next test is to check that the dip switch controlling the upper address bits is working properly. If any of the channels failed the previous test go to step 71, debug board and retest.

46. Move switch #5 on SW1 to the on position.
47. Move oscilloscope GND and probe to channel 0.
48. Type '**f a 12**' and hit return.
49. Type '**f b**' and hit return.
50. Check oscilloscope to make sure that the sawtooth pattern is being generated.
51. Type '**f e**' and hit return.
52. Type '**f a 0**' and hit return.
53. Type '**f b**' and hit return.
54. Check to make sure that the sawtooth pattern is NOT being generated.
55. Type '**f e**' and hit return.
56. Type '**f a 24**' and hit return.
57. Type '**f b**' and hit return.
58. Check to make sure that the sawtooth pattern is NOT being generated.
59. Type '**f e**' and hit return.
60. Move switch #5 on SW1 to the off position and switch #6 on SW1 to the on position.
61. Type '**f a 24**' and hit return.
62. Type '**f b**' and hit return.
63. Check oscilloscope to make sure that the sawtooth pattern is being generated.
64. Type '**f e**' and hit return.
65. Type '**f a 0**' and hit return.
66. Type '**f b**' and hit return.
67. Check to make sure that the sawtooth pattern is NOT being generated.
68. Type '**f e**' and hit return.
69. Type '**f a 12**' and hit return.
70. Type '**f b**' and hit return.
71. Check to make sure that the sawtooth pattern is NOT being generated.
72. Type '**f e**' and hit return.
73. Turn off power and remove board.
74. If there are more boards to test repeat from step 17. Else go on to step 75.
75. Press '**ctrl-c**' in Xterm 3.
76. Type '**exit**' in Xterm 3 and hit return.
77. Press '**ctrl-c**' in Xterm 2.
78. Type '**exit**' in Xterm 2 and hit return.
79. In Xterm 1 type '**stop_dio**' and hit return.
80. Type '**exit**' and hit return.

2.4 High Voltage Amplifier Test

Requirements

2 Multifunction Boards
1 Chassis
2 PCs with Linux OS
2 FC-FC Multimode Fiber Optic Cables

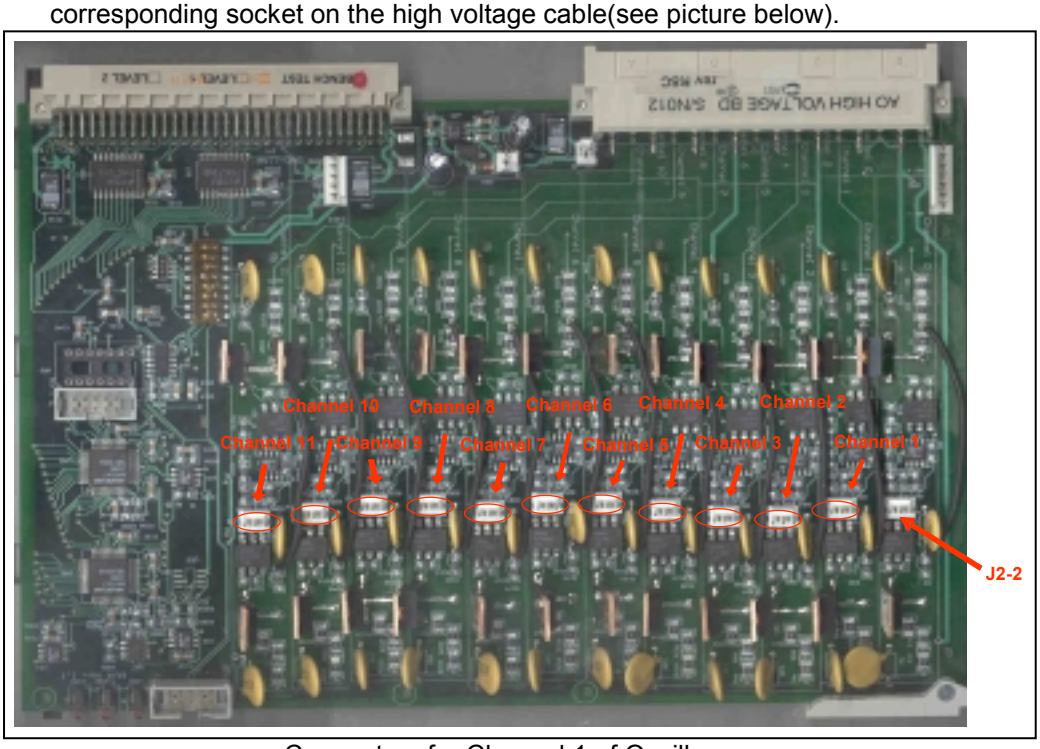
High Voltage Oscilloscope
High Voltage Cable
Piezo Material with two leads connected to it

NOTE: You will be working with +/-400 volts with this test. Make sure to follow ALL steps in the order that they are written. Failure to do so could result in serious electrical shock.

Procedure

1. On AOUIM open 3 Xterm windows
2. In first Xterm window type '**rlogin –l ao aoicm**' and hit return
3. Type the password, '**wai!mea**' and hit return.
4. Change to the '**dio32**' directory.
5. Type '**su aroot**' and hit return.
6. Type the password, '**wai!mea**' and hit return.
7. Type '**start_dio**' and hit return. This should start dio32.
8. In second Xterm window type '**rlogin –l ao aoicm**' and hit return.
9. Type the password, '**wai!mea**', and hit return.
10. Change to '**dio32**' directory.
11. Type '**cat /dev/rtf0**' and hit return.
12. In the third Xterm window, type '**rlogin –l ao aoicm**' and hit return.
13. Type the password, '**wai!mea**' and hit return.
14. Change to the '**dio32**' directory.
15. Type '**cat > /dev/rtf1**' and hit return.
16. You should now be able to see the commands that you type in Xterm 3 show up in Xterm window 2. To test this type '**test**' in Xterm 3. If you do not see 'test' in Xterm 2
    a. Hit '**ctrl-c**' in Xterm 3.
    b. In Xterm 3, type '**exit**' and hit return.
    c. Hit '**ctrl-c**' in Xterm 2.
    d. In Xterm 2, type '**exit**' and hit return.
    e. In Xterm 1, type '**stop_dio**' and hit return.
    f. Repeat from step 7.
17. Make sure that all dip switches on SW1 are in the 'OFF' position
18. Plug board that you would like to test into slot one of the chassis.
19. Connect oscilloscope channel 1 to J2 pin 2.
20. Turn on power by flipping switch on front of chassis
21. In window #2 type 'a i' and hit return.
22. Type '**f a 0**' and hit return to direct commands to channel 0.
23. Type '**f m 1**' and hit return to set the test pattern to sawtooth.
24. Type '**f p 10000**' and hit return to set the period of the pulse to 10000 ms.
25. Type '**f b**' and hit return to start pattern generation.
26. Check the oscilloscope to see a saw tooth pattern is being generated.
    If output stays constant on oscilloscope
    a. Turn off chassis power by flipping switch on front of chassis.
    b. Wait 5-10 seconds and turn power back on.
    c. Check if pattern is being generated.
    d. If not repeat a-c 4 times.
27. Type '**f e**' and hit return
28. Connect GND connector from oscilloscope to one of the leads on the Piezo material and stick it into socket 15 on the high voltage cable.
29. Connect probe of channel 2 on the oscilloscope to the other lead on of the Piezo material and stick it into socket 1 of the high voltage cable.
30. Turn on high voltage power supply, switch on back of chassis.
31. Type '**f b**' and then hit return.
32. Check to see that the voltage from channel 2 roughly follows the sawtooth pattern on channel 1 of the oscilloscope. See example below.
33. Type '**f e**' and then hit return.

34. Turn off high voltage power supply, switch on back of chassis.
    NOTE: This is a very important step. +/-400V is being carried on the high voltage cable and if you do not turn off the high voltage supply before doing step #34 there is a high risk for electrical shock.
35. Type '**f a** ' and the next channel number, then hit return.
36. Move oscilloscope channel 1 probe to the corresponding connector on channel(see picture below) the next channel and the oscilloscope channel 2 probe to the corresponding socket on the high voltage cable(see picture below).

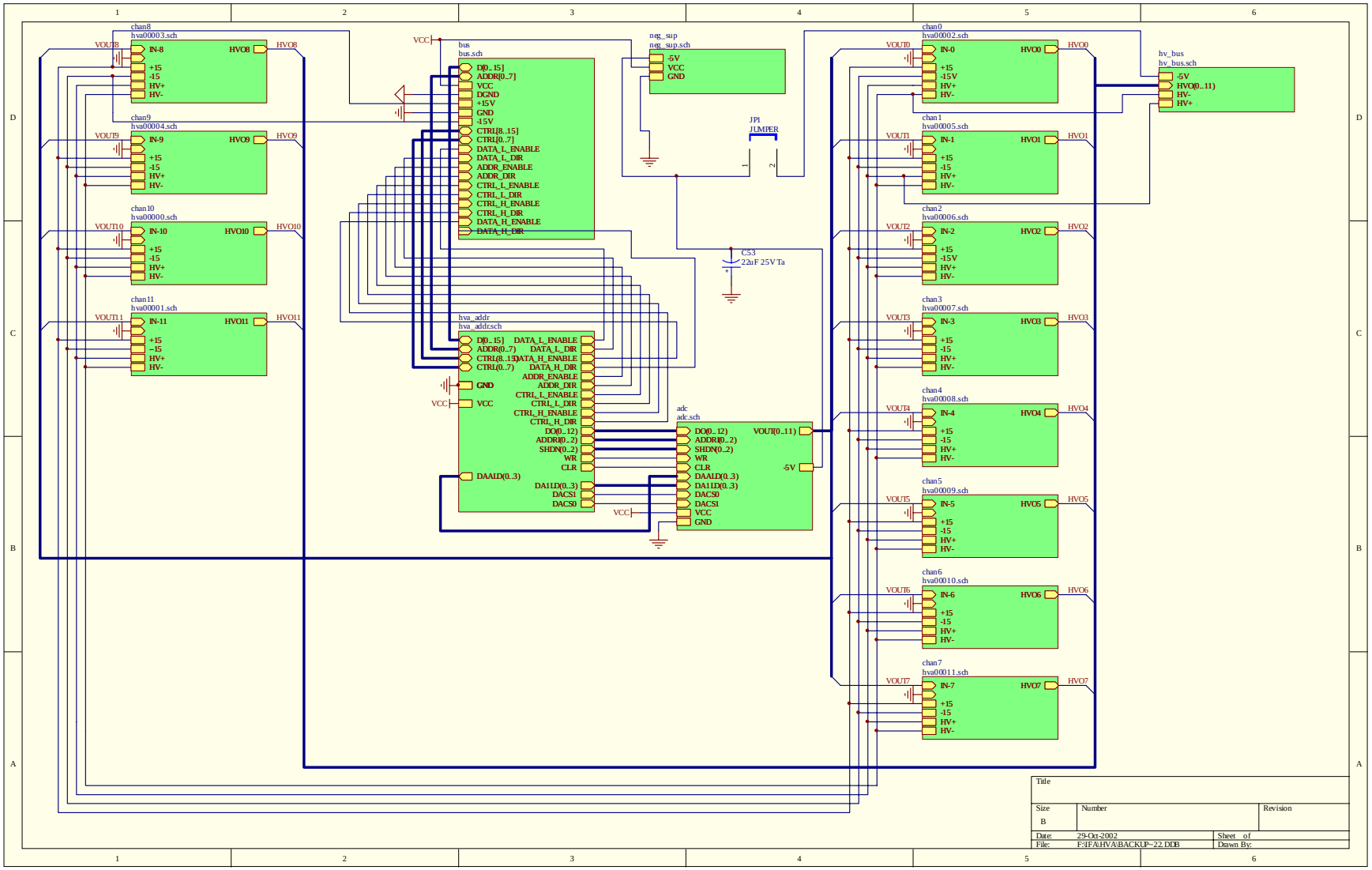


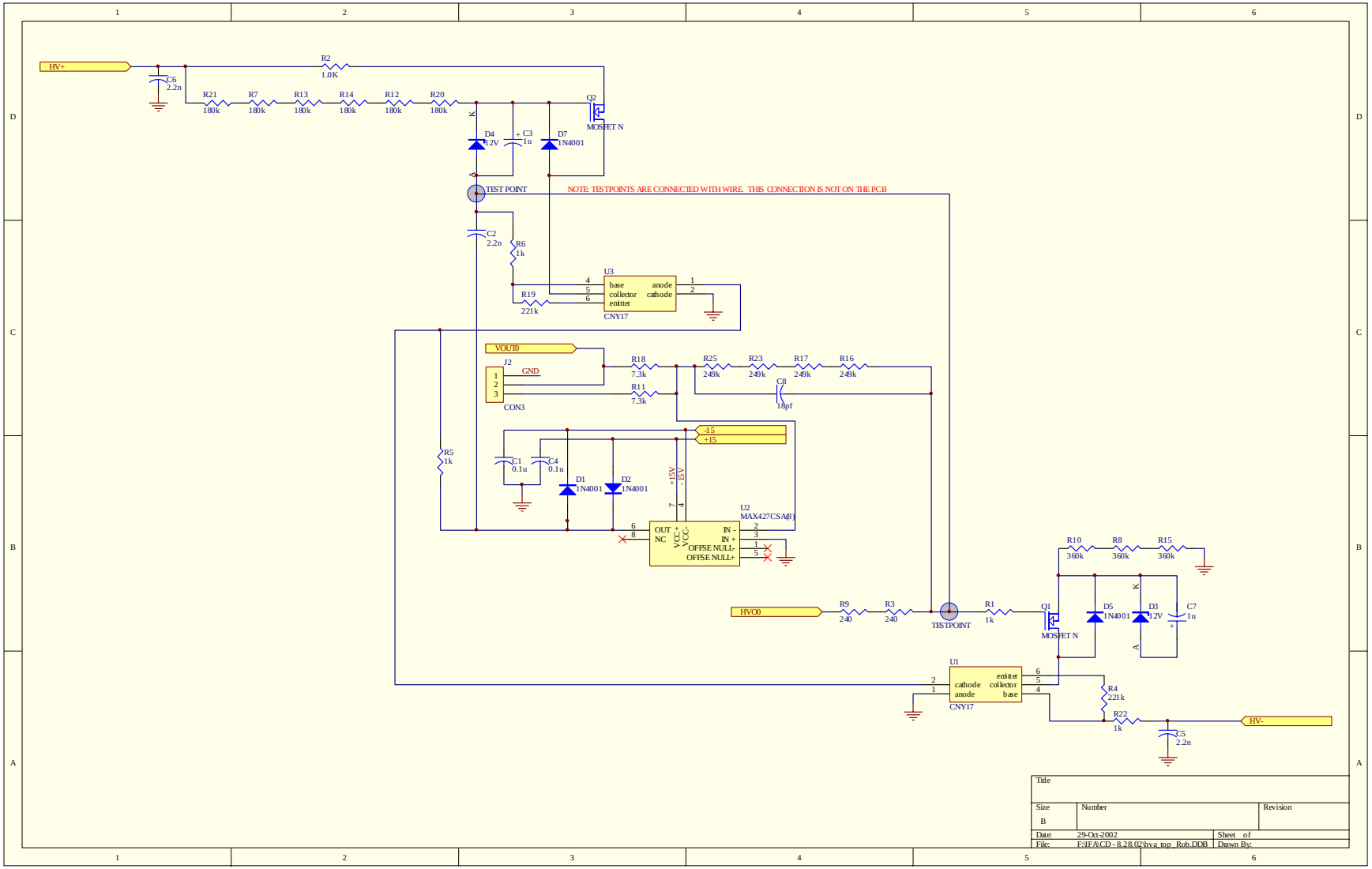
Connectors for Channel 1 of Oscilloscope

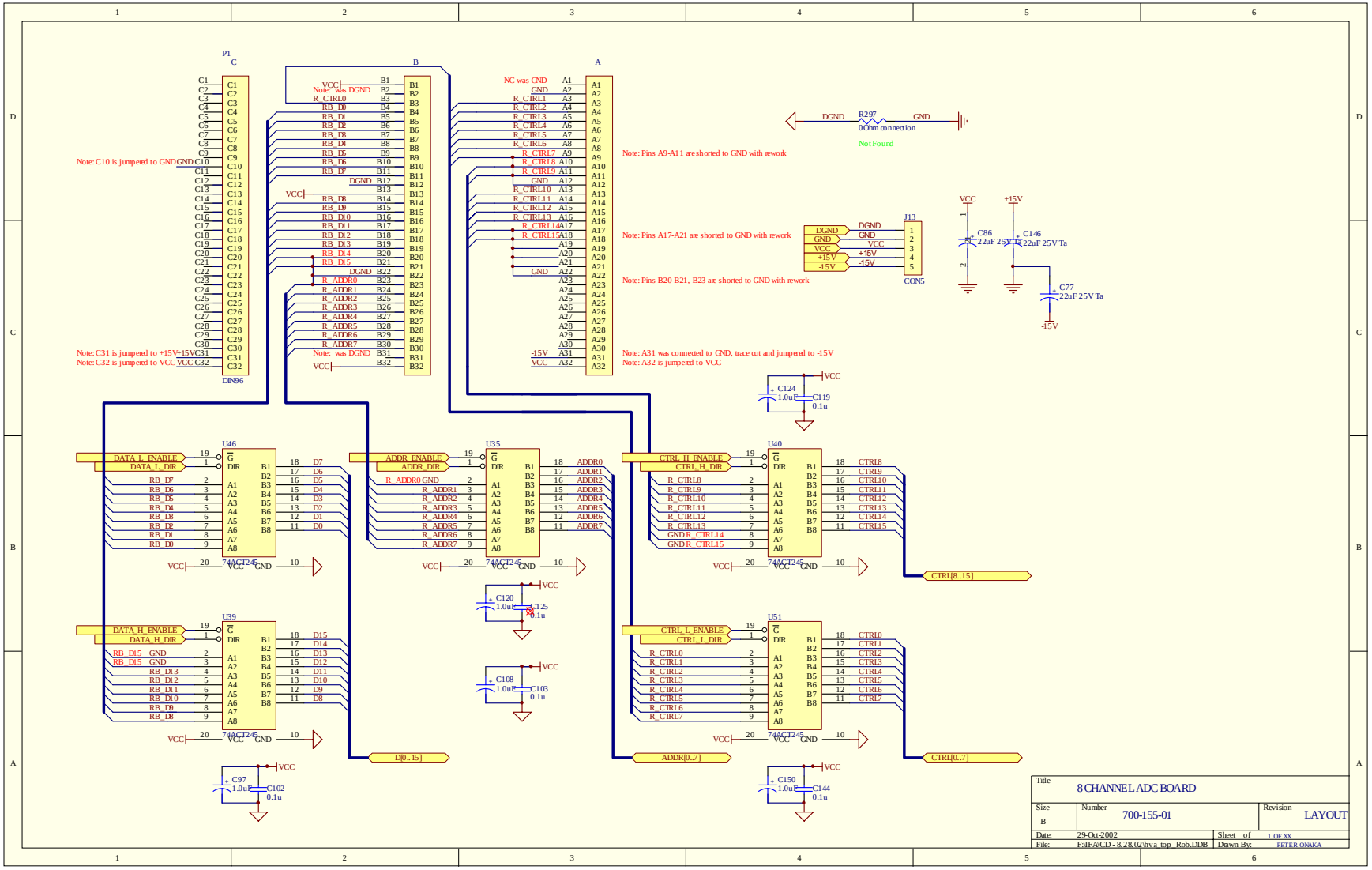
37. Repeat steps 23-34 until all channels 0-11 have all been tested, noting pass/fail of all channels.
38. Turn off power and remove board.
39. If there are more boards to test repeat from step 17. Else go on to step 40
40. Press '**ctrl-c**' in Xterm 3.
41. Type '**exit**' in Xterm 3 and hit return.
42. Press '**ctrl-c**' in Xterm 2.
43. Type '**exit**' in Xterm 2 and hit return.
44. In Xterm 1 type '**stop_dio**' and hit return.
45. Type '**exit**' and hit return.

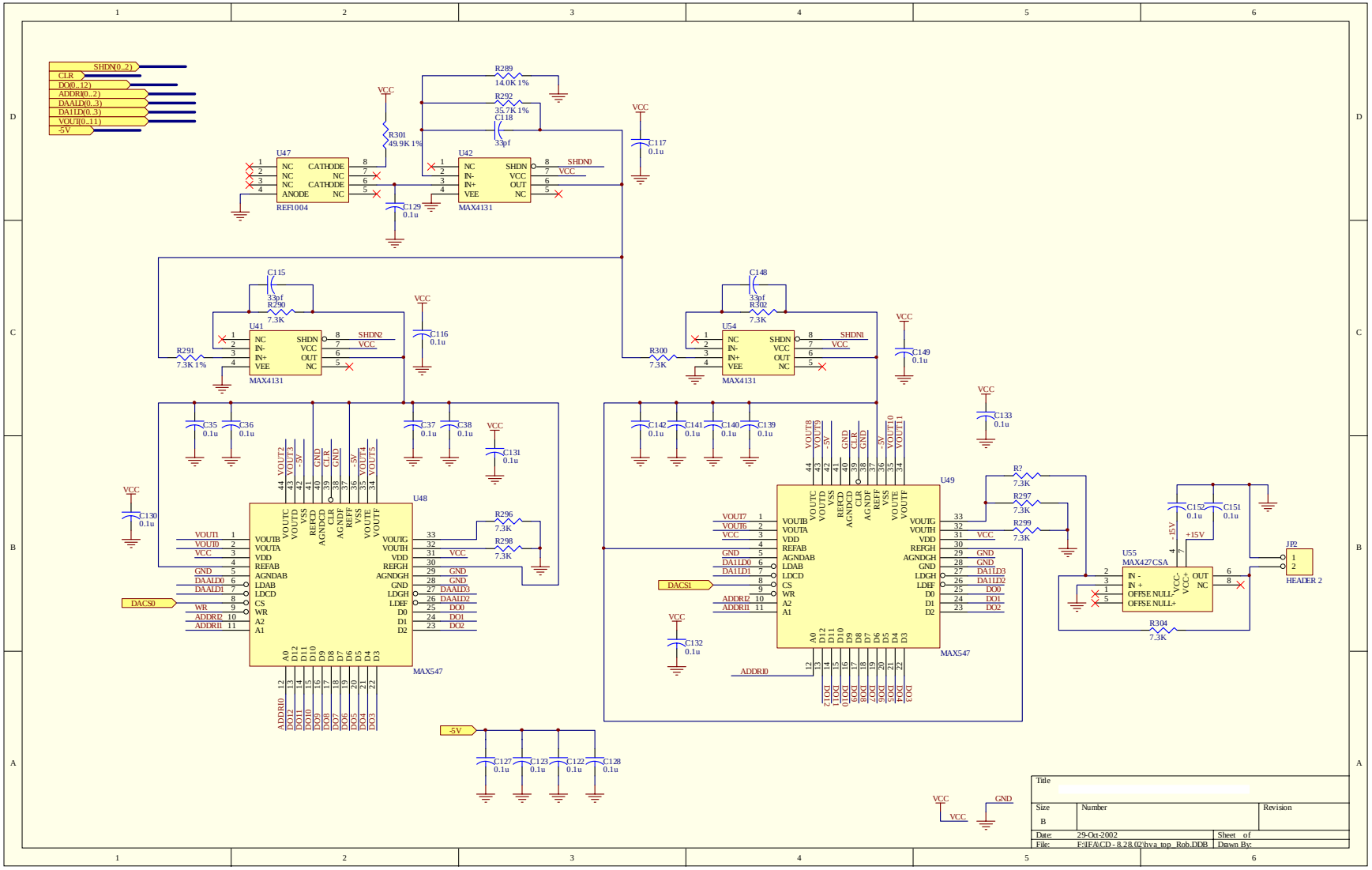
3 Schematic

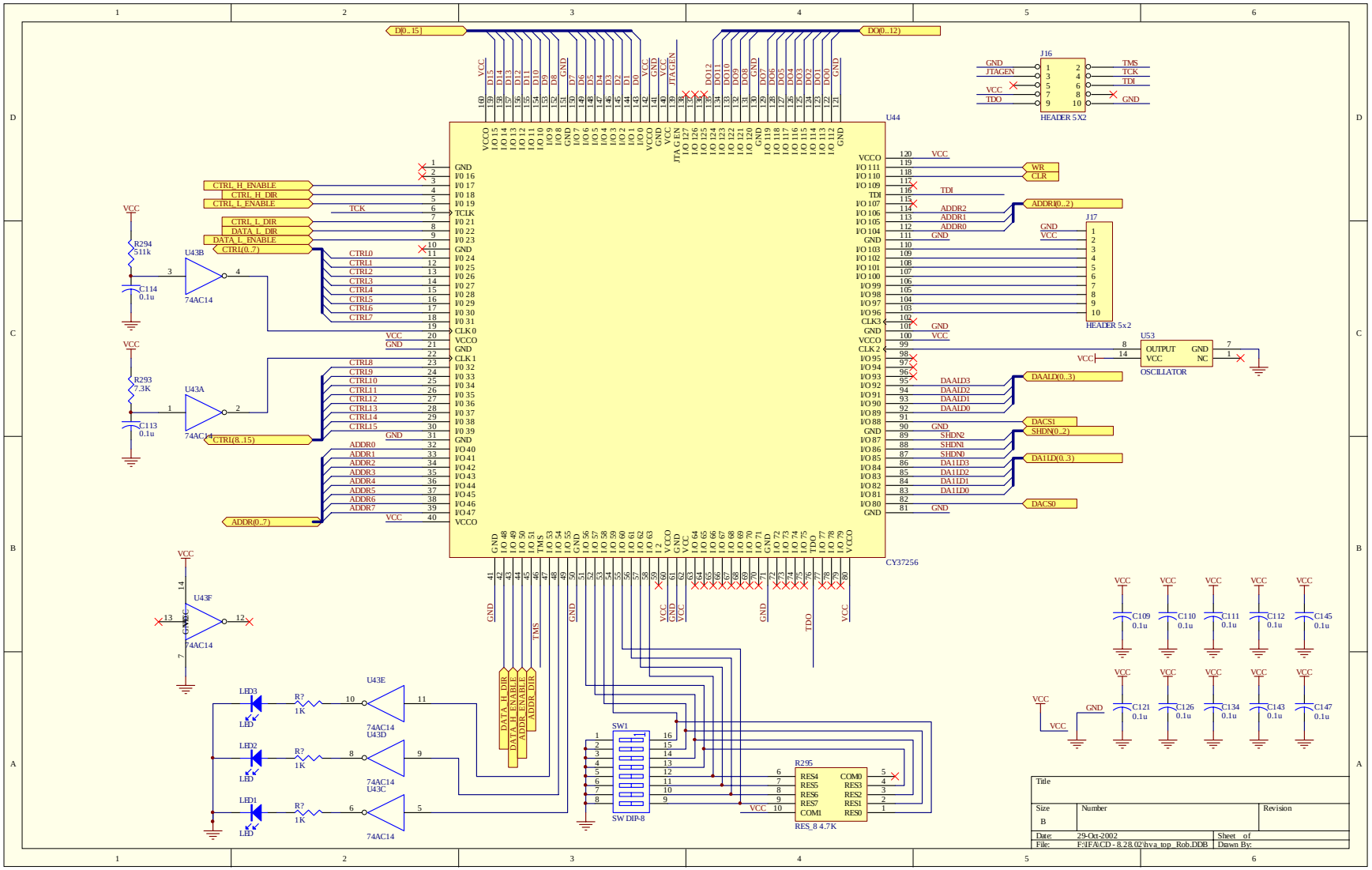
Note: that schematic only shows one channel of High Voltage Amplifier. Each channel is identical in design.

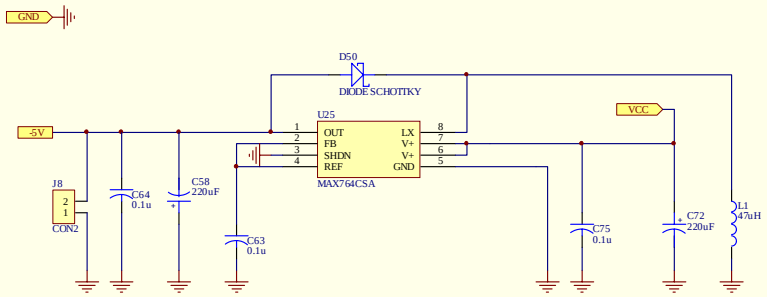

chan8
hva00003.sch
VOUT8
IN-8
HVO8
HVO8
+15
-15
HV+
HV-
chan9
hva00004.sch
VOUT9
IN-9
HVO9
HVO9
chan10
hva00000.sch
VOUT10
IN-10
HVO10
HVO10
chan11
hva00001.sch
VOUT11
IN-11
HVO11
HVO11
VCC
bus
bus.sch
D[0..15]
ADDR[0..7]
VCC
DGND
+15V
GND
-15V
CTRL[8..15]
CTRL[0..7]
DATA_L_ENABLE
DATA_L_DIR
ADDR_ENABLE
ADDR_DIR
CTRL_L_ENABLE
CTRL_L_DIR
CTRL_H_ENABLE
CTRL_H_DIR
DATA_H_DIR
DATA_H_ENABLE
DATA_H_DIR
neg_sup
neg_sup.sch
-5V
VCC
GND
JP1
JUMPER
C53
22uF 25V Ta
hva_addr
hva_addr.sch
D[0..15]
ADDR(0..7)
CTRL(8..15)
CTRL(0..7)
GND
VCC
DATA_L_ENABLE
DATA_L_DIR
DATA_H_ENABLE
DATA_H_DIR
ADDR_ENABLE
ADDR_DIR
CTRL_L_ENABLE
CTRL_L_DIR
CTRL_H_ENABLE
CTRL_H_DIR
DO[0..12)
ADDR[0..2)
SHDN[0..2)
WR
CLR
DAALD(0..3)
DA11D(0..3)
DACS1
DACS0
adc
adc.sch
DO[0..12)
ADDR[0..2)
SHDN[0..2)
WR
CLR
DAALD(0..3)
DA11D(0..3)
DACS0
DACS1
VCC
GND
VOUT[0..11)
-5V
chan0
hva00002.sch
VOUT0
IN-0
HVO0
HVO0
-15V
HV+
HV-
chan1
hva00005.sch
VOUT1
IN-1
HVO1
HVO1
-15
chan2
hva00006.sch
VOUT2
IN-2
HVO2
HVO2
chan3
hva00007.sch
VOUT3
IN-3
HVO3
HVO3
chan4
hva00008.sch
VOUT4
IN-4
HVO4
HVO4
chan5
hva00009.sch
VOUT5
IN-5
HVO5
HVO5
chan6
hva00010.sch
VOUT6
IN-6
HVO6
HVO6
chan7
hva00011.sch
VOUT7
IN-7
HVO7
HVO7
hv_bus
hv_bus.sch
-5V
HVO[0..11)
HV-
HV+
Title
Size
B
Number
Revision
Date: 29-Oct-2002
Sheet of
File: F:\IFA\HVA\BACKUP~22.DDB
Drawn By:


HV+
R2
1.0K
C6
2.2n
R21
180k
R7
180k
R13
180k
R14
180k
R12
180k
R20
180k
Q2
MOSFET N
D4
12V
C3
1u
D7
1N4001
TEST POINT
NOTE: TESTPOINTS ARE CONNECTED WITH WIRE. THIS CONNECTION IS NOT ON THE PCB
C2
2.2n
R6
1k
R19
221k
U3
base
collector
emitter
anode
cathode
CNY17
VOUT0
J2
GND
CON3
R18
7.3k
R11
7.3k
R25
249k
R23
249k
R17
249k
R16
249k
C8
18pf
R5
1k
-15
+15
C1
0.1u
C4
0.1u
D1
1N4001
D2
1N4001
U2
MAX427CSA(8)
OUT
NC
VCC+
VCC-
IN -
IN +
OFFSE NULL-
OFFSE NULL+
HVO0
R9
240
R3
240
TESTPOINT
R1
1k
Q1
MOSFET N
R10
360k
R8
360k
R15
360k
D5
1N4001
D3
12V
C7
1u
U1
cathode
anode
emitter
collector
base
CNY17
R4
221k
R22
1k
C5
2.2n
HV-
Title
Size
B
Number
Revision
Date: 29-Oct-2002
Sheet of
File: F:\JFA\CD - 8.28.02\hva_top_Rob.DDB
Drawn By:


P1
DIN96
Note: C10 is jumpered to GND
Note: C31 is jumpered to +15V
Note: C32 is jumpered to VCC
Note: Pins A9-A11 are shorted to GND with rework
Note: Pins A17-A21 are shorted to GND with rework
Note: Pins B20-B21, B23 are shorted to GND with rework
Note: A31 was connected to GND, trace cut and jumpered to -15V
Note: A32 is jumpered to VCC
R297
0Ohm connection
Not Found
J13
CON5
C86
22uF 25V Ta
C146
22uF 25V Ta
C77
22uF 25V Ta
C124
1.0uF
C119
0.1u
C120
1.0uF
C125
0.1u
C108
1.0uF
C103
0.1u
C97
1.0uF
C102
0.1u
C150
1.0uF
C144
0.1u
U46
U35
U40
U39
U51
74ACT245
DATA_L_ENABLE
DATA_L_DIR
ADDR_ENABLE
ADDR_DIR
CTRL_H_ENABLE
CTRL_H_DIR
DATA_H_ENABLE
DATA_H_DIR
CTRL_L_ENABLE
CTRL_L_DIR
D[0..15]
ADDR[0..7]
CTRL[8..15]
CTRL[0..7]
8 CHANNEL ADC BOARD
Title
Size
B
Number
700-155-01
Revision
LAYOUT
Date: 29-Oct-2002
Sheet of 1 OF XX
File: F:\JFA\CD - 8.28.02\hva_top_Rob.DDB
Drawn By: PETER ONAKA


SHDN[0..2]
CLR
DO[0..12]
ADDR[0..2]
DAALD[0..3]
DA1LD[0..3]
VOUT[0..11]
-5V
R289
14.0K 1%
R292
35.7K 1%
C118
33pf
R301
49.9K 1%
VCC
U47
REF1004
U42
MAX4131
SHDN0
C117
0.1u
C129
0.1u
C115
33pf
R290
7.3K
U41
MAX4131
SHDN2
C116
0.1u
R291
7.3K 1%
C148
33pf
R302
7.3K
U54
MAX4131
SHDN1
C149
0.1u
R300
7.3K
C35
0.1u
C36
0.1u
C37
0.1u
C38
0.1u
C131
0.1u
C130
0.1u
U48
MAX547
DACS0
R296
7.3K
R298
7.3K
C142
0.1u
C141
0.1u
C140
0.1u
C139
0.1u
C133
0.1u
U49
MAX547
DACS1
C132
0.1u
R7
7.3K
R297
7.3K
R299
7.3K
U55
MAX427CSA
C152
0.1u
C151
0.1u
-15V
+15V
R304
7.3K
JP2
HEADER 2
C127
0.1u
C123
0.1u
C122
0.1u
C128
0.1u
GND
Title
Size
B
Number
Revision
Date: 29-Oct-2002
Sheet of
File: F:\JFA\CD - 8.28.02\hva_top_Rob.DDB
Drawn By:


D[0..15]
DO[0..12]
U44
CY37256
J16
HEADER 5X2
J17
HEADER 5x2
U53
OSCILLATOR
U43B
U43A
U43F
U43E
74AC14
SW1
SW DIP-8
R295
RES_8 4.7K
CTRL_H_ENABLE
CTRL_H_DIR
CTRL_L_ENABLE
CTRL_L_DIR
DATA_L_ENABLE
CTRL[0..7]
CTRL[8..15]
ADDR[0..7]
ADDR[0..2)
DAALD[0..3)
DA1LD[0..3)
SHDN[0..2)
DACS1
DACS0
WR
CLR
TCK
TDI
TMS
TDO
VCC
GND
Title
Size
B
Number
Revision
Date: 29-Oct-2002
Sheet of
File: F:\IFA\CD - 8.28.02\hva_top_Rob.DDB
Drawn By:



Title		
Size: B	Number	Revision
Date: 29-Oct-2002		Sheet of
File: F:\IFA\CD - 8.28.02\hva_top_Rob.DDB		Drawn By:

4 Datasheets

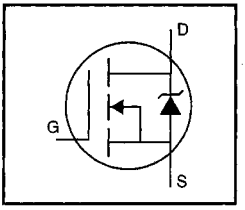
4.1 IRFBG20

International IOR Rectifier

IRFBG20

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 1000V

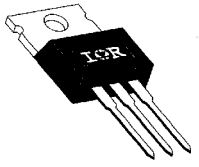
$R_{DS(on)}$ = 11Ω

I_D = 1.4A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

DATA SHEETS

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	1.4	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	0.86	
I_{DM}	Pulsed Drain Current ①	5.6	
P_D @ T_C = 25°C	Power Dissipation	54	W
	Linear Derating Factor	0.43	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	200	mJ
I_{AR}	Avalanche Current ①	1.4	A
E_{AR}	Repetitive Avalanche Energy ①	5.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	1.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	2.3	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	1000	—	—	V	V_{GS}=0V, I_D= 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	1.2	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	11	Ω	V_{GS}=10V, I_D=0.84A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250μA
g_{fs}	Forward Transconductance	1.0	—	—	S	V_{DS}=50V, I_D=0.84A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	100	μA	V_{DS}=1000V, V_{GS}=0V
		—	—	500		V_{DS}=800V, V_{GS}=0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	38	nC	I_D=1.4A
Q_{gs}	Gate-to-Source Charge	—	—	4.9		V_{DS}=400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	22		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	9.4	—	ns	V_{DD}=500V
t_r	Rise Time	—	17	—		I_D=1.4A
$t_{d(off)}$	Turn-Off Delay Time	—	58	—		R_G=18Ω
t_f	Fall Time	—	31	—		R_D=370Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	500	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	52	—		V_{DS}=25V
C_{rss}	Reverse Transfer Capacitance	—	17	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	1.4	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	5.6		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	T_J=25°C, I_S=1.4A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	130	190	ns	T_J=25°C, I_F=1.4A
Q_{rr}	Reverse Recovery Charge	—	0.46	0.69	μC	di/dt=100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=50V, starting T_J=25°C, L=193mH R_G=25Ω, I_{AS}=1.4A (See Figure 12)

③ I_{SD}≤1.4A, di/dt≤60A/μs, V_{DD}≤600, T_J≤150°C

④ Pulse width ≤ 300 μs; duty cycle ≤2%.

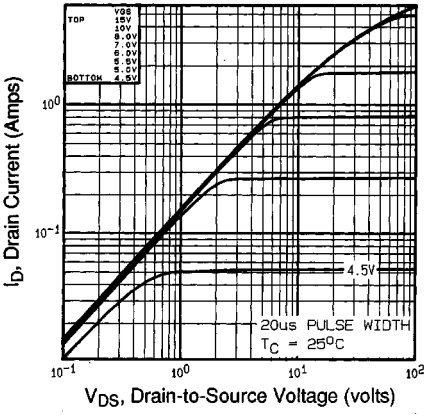


Fig 1. Typical Output Characteristics, T_C=25°C

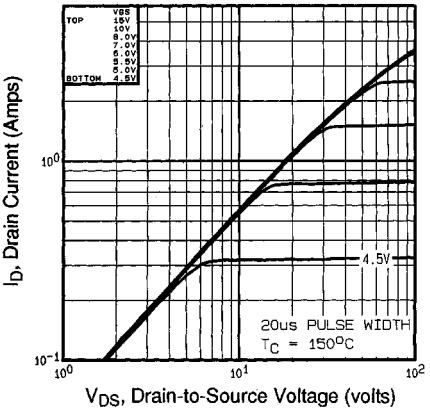


Fig 2. Typical Output Characteristics, T_C=150°C

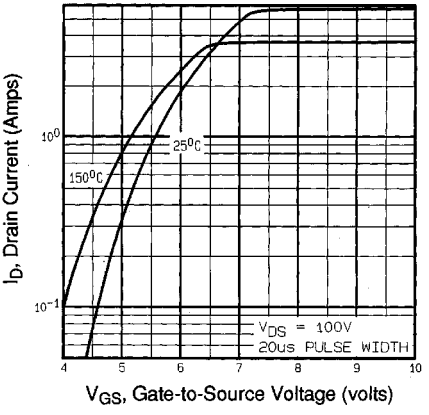


Fig 3. Typical Transfer Characteristics

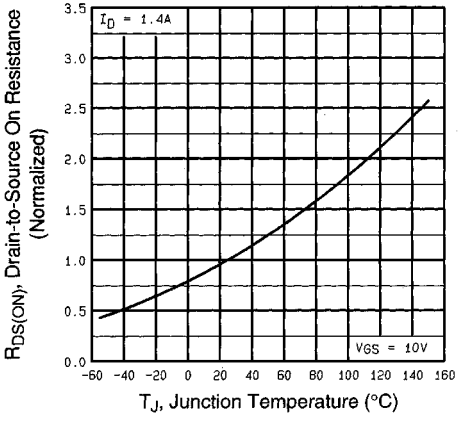


Fig 4. Normalized On-Resistance Vs. Temperature

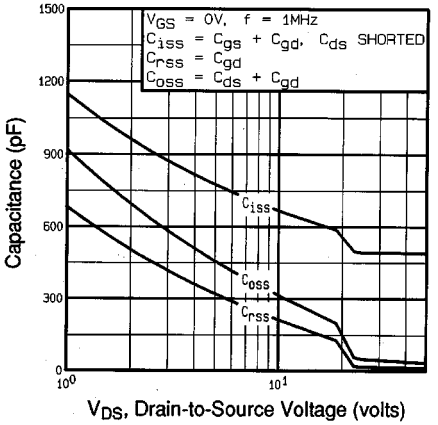


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

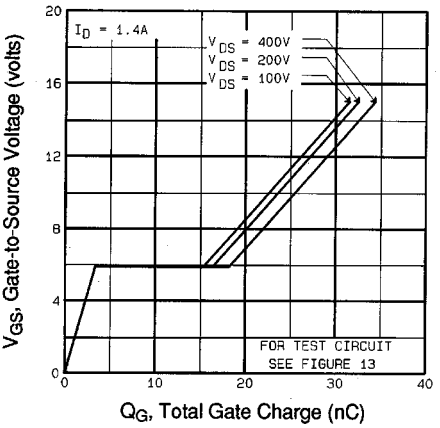


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

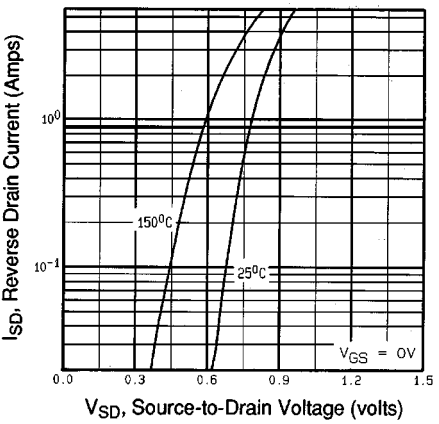


Fig 7. Typical Source-Drain Diode Forward Voltage

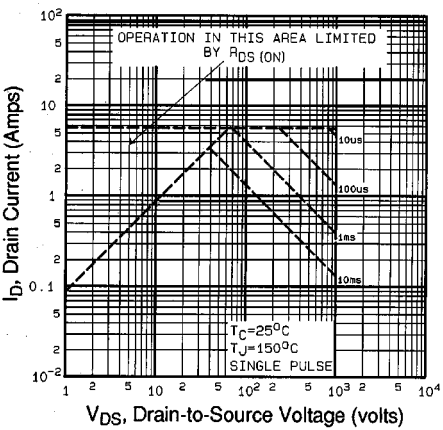


Fig 8. Maximum Safe Operating Area

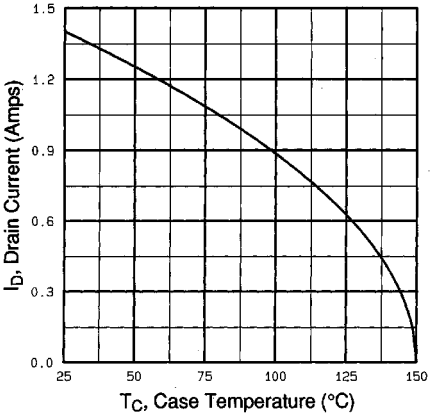


Fig 9. Maximum Drain Current Vs. Case Temperature

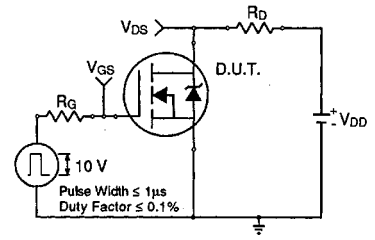


Fig 10a. Switching Time Test Circuit

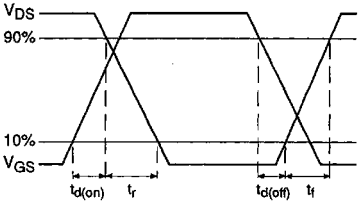


Fig 10b. Switching Time Waveforms

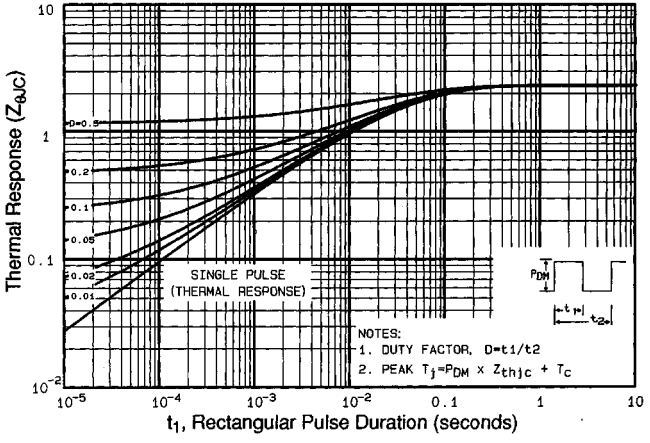


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

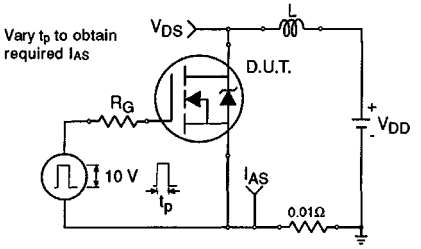


Fig 12a. Unclamped Inductive Test Circuit

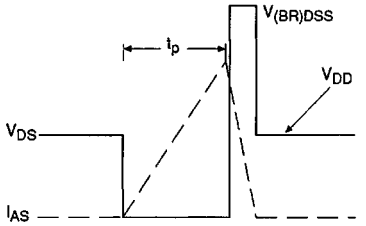


Fig 12b. Unclamped Inductive Waveforms

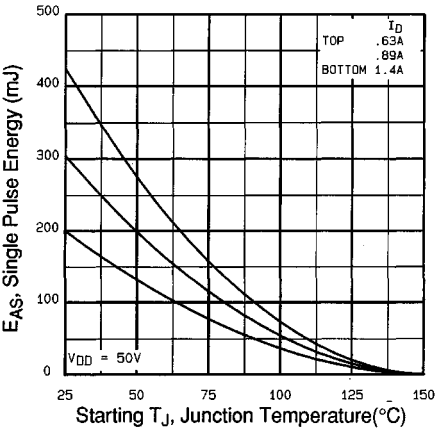


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

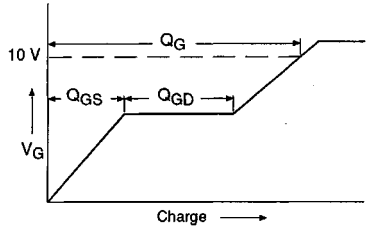


Fig 13a. Basic Gate Charge Waveform

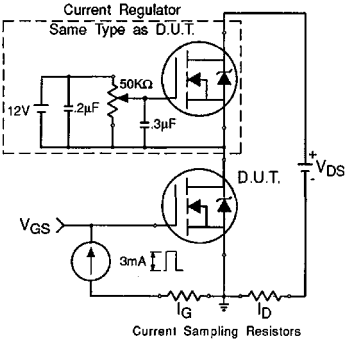


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1509

Appendix C: Part Marking Information – See page 1516

Appendix E: Optional Leadforms – See page 1525

International IOR Rectifier

4.2 IRG4PH50U

PD - 91574B

International
IOR Rectifier

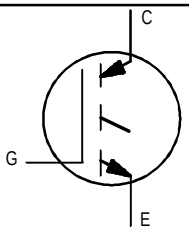
IRG4PH50U

INSULATED GATE BIPOLAR TRANSISTOR

Ultra Fast Speed IGBT

Features

- UltraFast: Optimized for high operating frequencies up to 40 kHz in hard switching, >200 kHz in resonant mode
- New IGBT design provides tighter parameter distribution and higher efficiency than previous generations
- Optimized for power conversion; SMPS, UPS and welding
- Industry standard TO-247AC package



n-channel

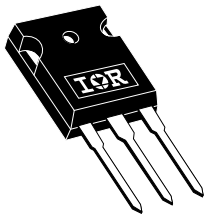
V_{CES} = 1200V

$V_{CE(on)\ typ.}$ = 2.78V

@V_{GE} = 15V, I_C = 24A

Benefits

- Higher switching frequency capability than competitive IGBTs
- Highest efficiency available
- Much lower conduction losses than MOSFETs
- More efficient than short circuit rated IGBTs



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	45	A
I_C @ T_C = 100°C	Continuous Collector Current	24	
I_{CM}	Pulsed Collector Current ①	180	
I_{LM}	Clamped Inductive Load Current ②	180	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	170	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.64	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	g (oz)

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.20	—	V/°C	V_{GE} = 0V, I_C = 1.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.56	3.5	V	I_C = 20A
		—	2.78	3.7		I_C = 24A — V_{GE} = 15V
		—	3.20	—		I_C = 45A — See Fig.2, 5
		—	2.54	—		I_C = 24A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-13	—	mV/°C	V_{CE} = V_{GE}, I_C = 250µA
g_{fe}	Forward Transconductance ⑤	23	35	—	S	V_{CE} = 100V, I_C = 24A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 24V, T_J = 25°C
		—	—	5000		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	160	250	nC	I_C = 24A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	27	40		V_{CC} = 400V — See Fig. 8
Q_{gc}	Gate - Collector Charge (turn-on)	—	53	83		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	35	—	ns	
t_r	Rise Time	—	15	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	200	350		I_C = 24A, V_{CC} = 960V
t_f	Fall Time	—	290	500		V_{GE} = 15V, R_G = 5.0Ω
E_{on}	Turn-On Switching Loss	—	0.53	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	1.41	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	1.94	2.6		
$t_{d(on)}$	Turn-On Delay Time	—	31	—	ns	T_J = 150°C
t_r	Rise Time	—	18	—		I_C = 24A, V_{CC} = 960V
$t_{d(off)}$	Turn-Off Delay Time	—	320	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	280	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	5.40	—	mJ	See Fig. 11, 14
E_{on}	Turn-On Switching Loss	—	0.35	—	mJ	T_J = 25°C, V_{GE} = 15V, R_G = 5.0Ω
E_{off}	Turn-Off Switching Loss	—	1.43	—		I_C = 20A, V_{CC} = 960V
E_{ts}	Total Switching Loss	—	1.78	2.9		Energy losses include "tail"
		—	4.56	—		See Fig. 9, 10, 11, 14, T_J = 150°C
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	3600	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	160	—		V_{CC} = 30V — See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	31	—		f = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

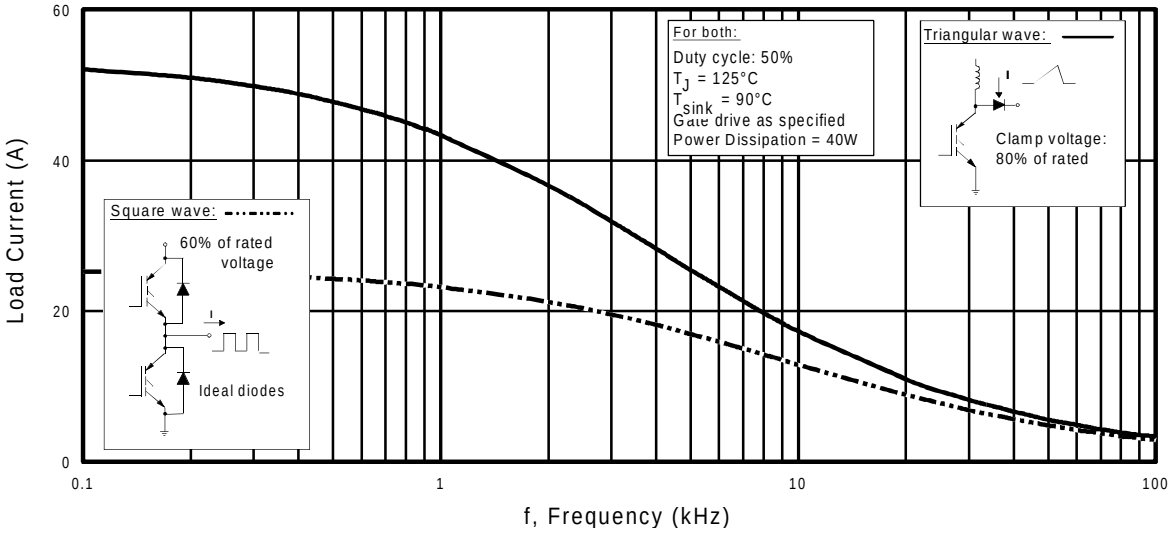


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

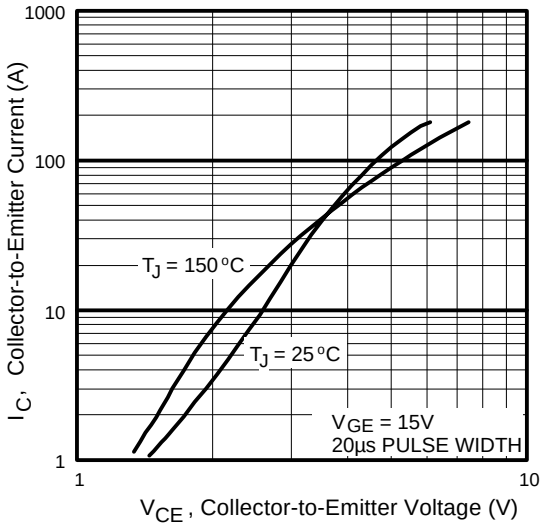


Fig. 2 - Typical Output Characteristics

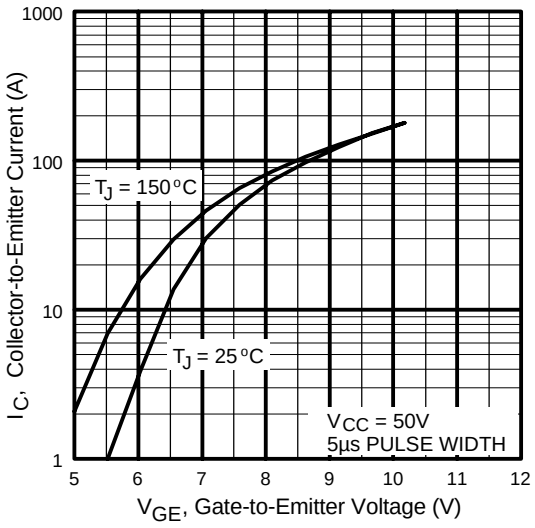


Fig. 3 - Typical Transfer Characteristics

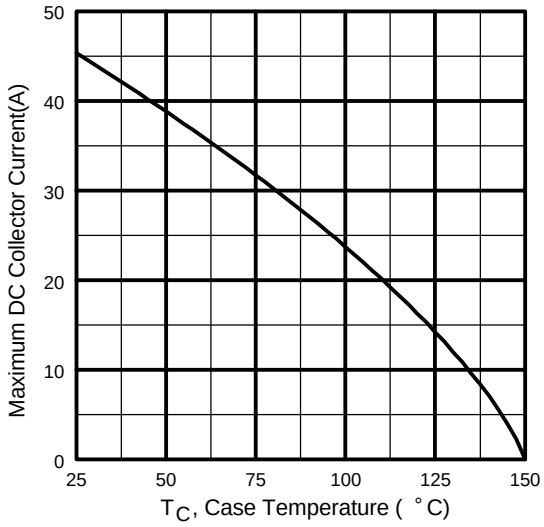


Fig. 4 - Maximum Collector Current vs. Case Temperature

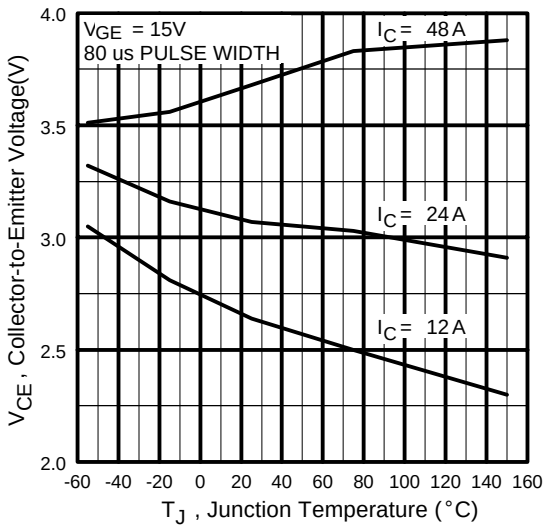


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

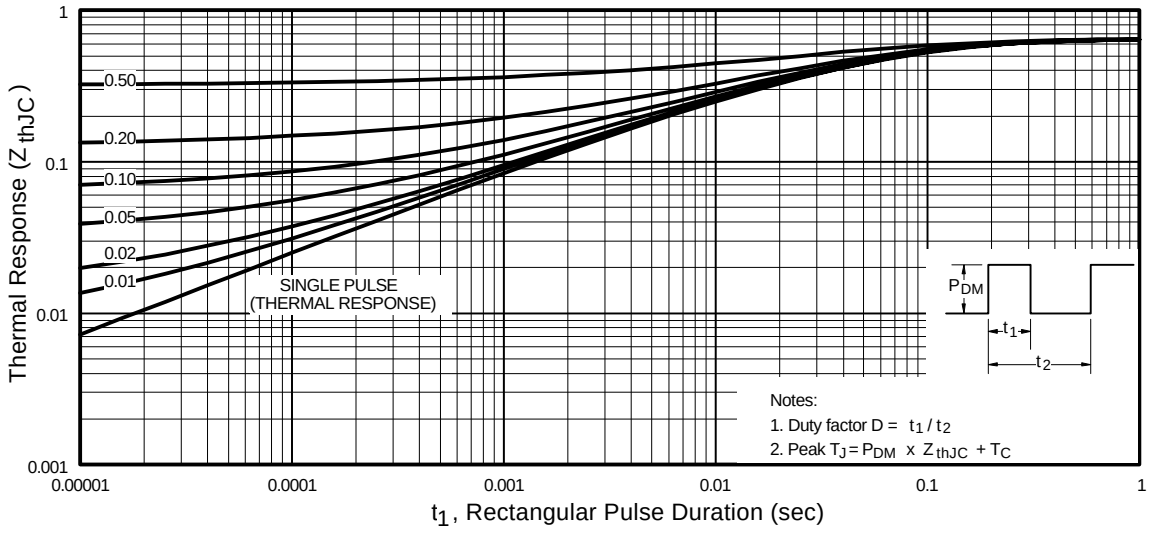


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

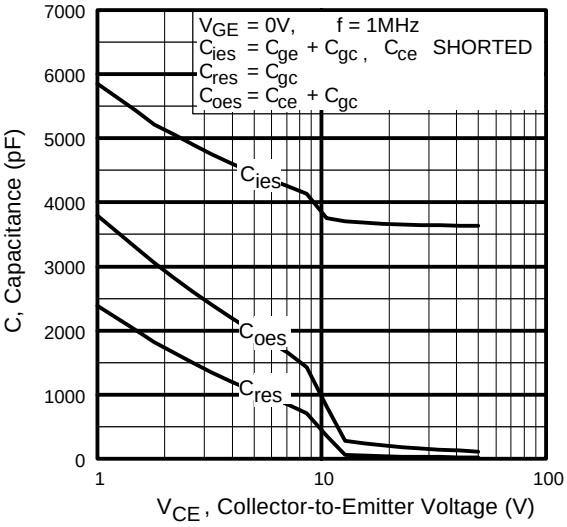


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

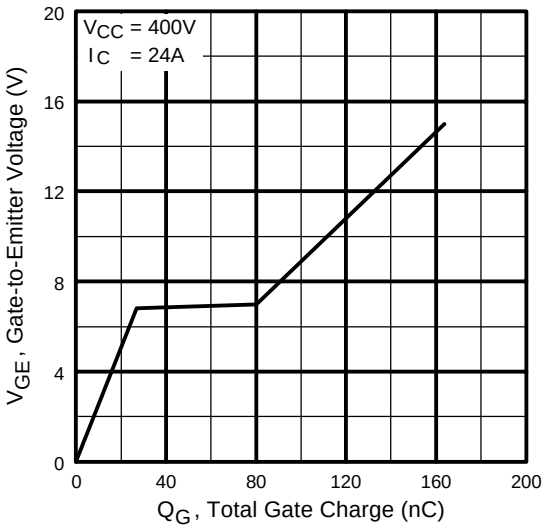


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

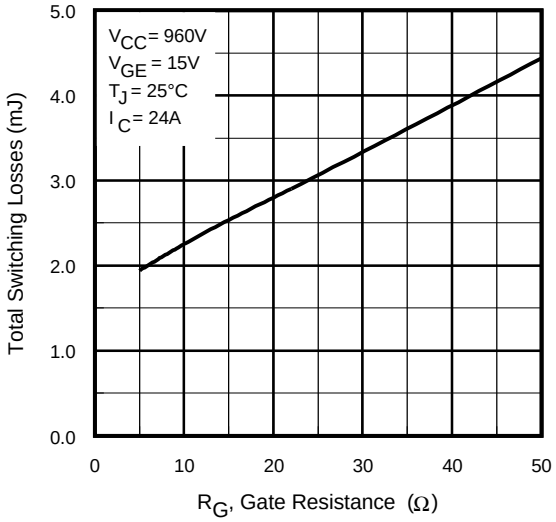


Fig. 9 - Typical Switching Losses vs. Gate Resistance

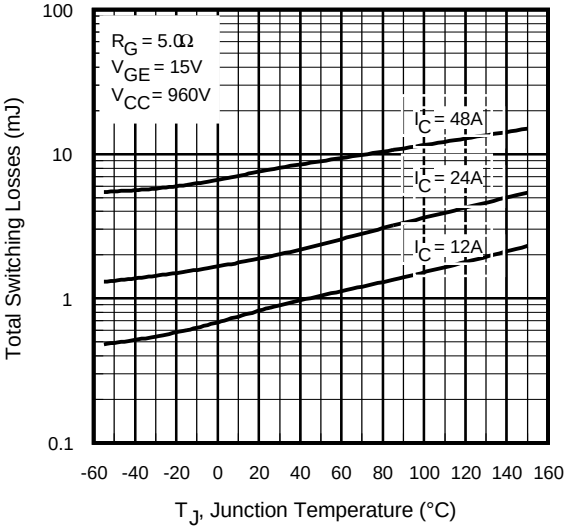


Fig. 10 - Typical Switching Losses vs. Junction Temperature

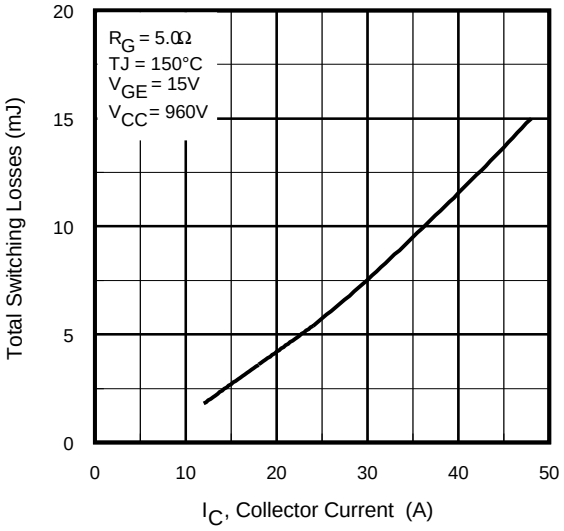


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

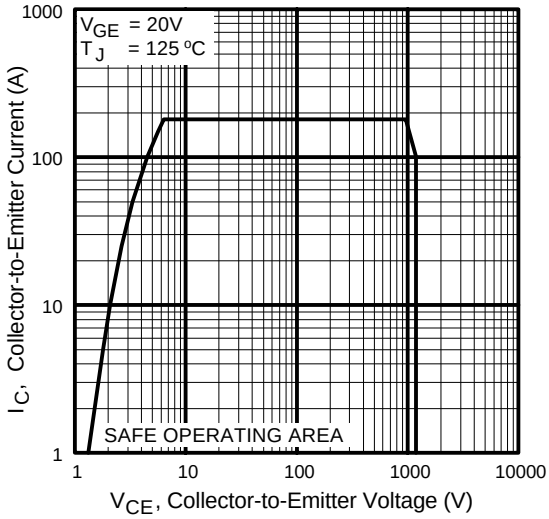


Fig. 12 - Turn-Off SOA

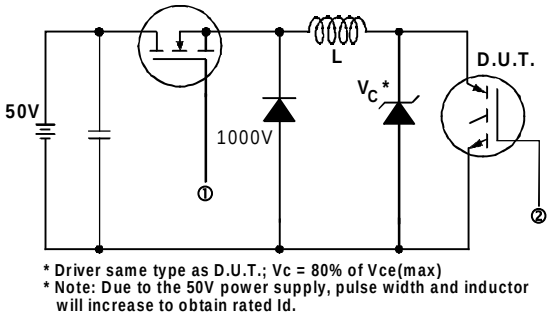


Fig. 13a - Clamped Inductive Load Test Circuit

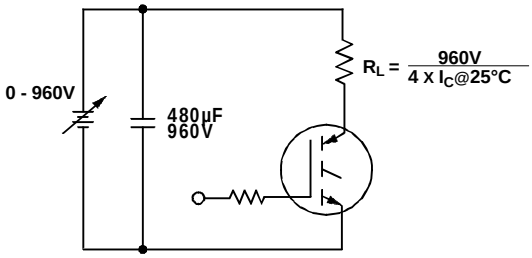


Fig. 13b - Pulsed Collector Current Test Circuit

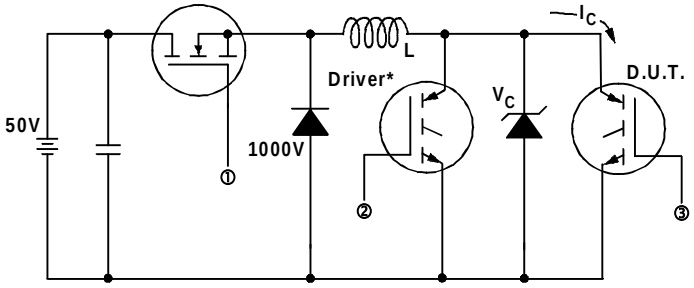


Fig. 14a - Switching Loss Test Circuit

*** Driver same type as D.U.T., VC = 960V**

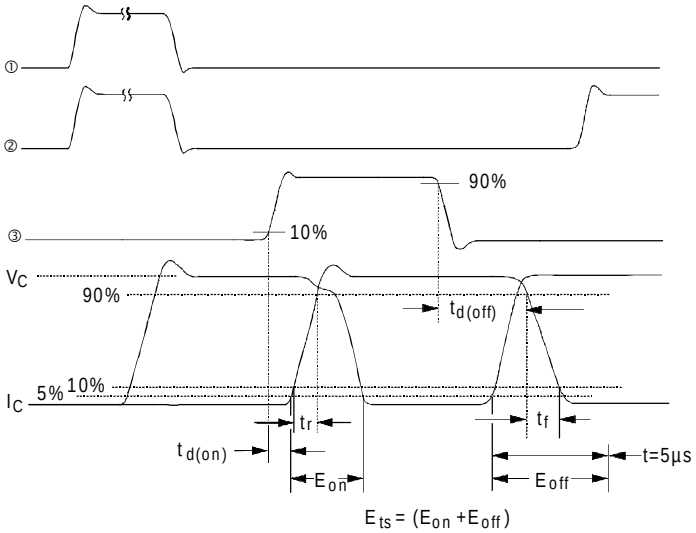
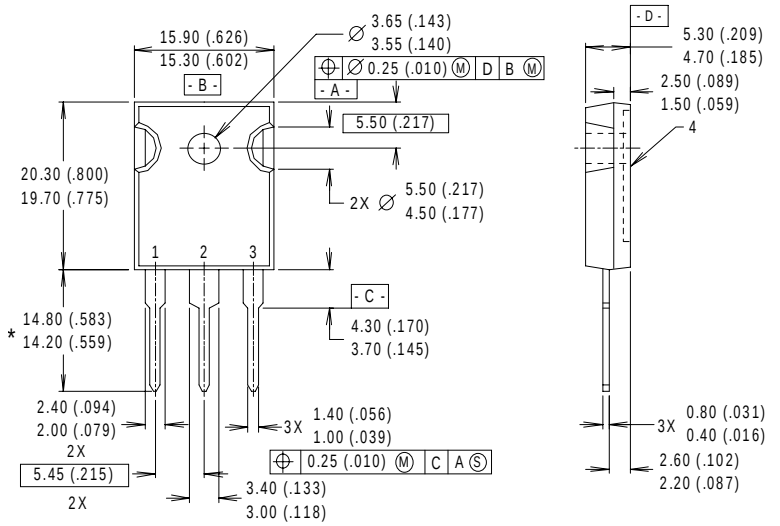


Fig. 14b - Switching Loss Waveforms

Case Outline and Dimensions — TO-247AC



NOTES:
1 DIMENSIONS & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
4 CONFORMS TO JEDEC OUTLINE TO-247AC.

LEAD ASSIGNMENTS
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

* LONGER LEADED (20mm) VERSION AVAILABLE (TO-247AD) TO ORDER ADD "-E" SUFFIX TO PART NUMBER

CONFORMS TO JEDEC OUTLINE TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331
IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630
IR TAIWAN:16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936
http://www.irf.com/ Data and specifications subject to change without notice. 01/02

4.3 74AC14

FAIRCHILD SEMICONDUCTOR™

November 1988
Revised December 1999

74AC14 • 74ACT14
Hex Inverter with Schmitt Trigger Input

General Description

The 74AC14 and 74ACT14 contain six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The 74AC14 and 74ACT14 have hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

Features

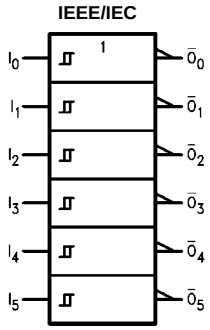
- I_{CC} reduced by 50%
- Outputs source/sink 24 mA
- 74ACT14 has TTL-compatible inputs

Ordering Code:

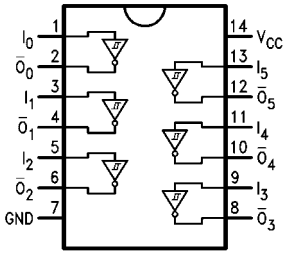
Order Number	Package Number	Package Description
74AC14SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74AC14SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MS-153, 4.4mm Wide
74AC14PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT14SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74ACT14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MS-153, 4.4mm Wide
74ACT14PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
I_n	Inputs
$\overline{O}_n$	Outputs

Function Table

Input	Output
A	**$\overline{O}$**
L	H
H	L

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Typ	T_A = −40°C to +85°C Guaranteed Limits		Units	Conditions
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 µA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	I_{OH} = 12
		4.5		3.86	3.76		I_{OH} = 24 mA
		5.5		4.86	4.76		I_{OH} = 24 mA (Note 2)
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 µA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	I_{OL} = 12
		4.5		0.36	0.44		I_{OL} 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 2)
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		±0.1	±1.0	µA	V_I = V_{CC}, GND
V_{t+}	Maximum Positive Threshold	3.0		2.2	2.2	V	T_A = Worst Case
		4.5		3.2	3.2		
		5.5		3.9	3.9		
V_{t-}	Minimum Negative Threshold	3.0		0.5	0.5	V	T_A = Worst Case
		4.5		0.9	0.9		
		5.5		1.1	1.1		
$V_{H(MAX)}$	Maximum Hysteresis	3.0		1.2	1.2	V	T_A = Worst Case
		4.5		1.4	1.4		
		5.5		1.6	1.6		
$V_{H(MIN)}$	Minimum Hysteresis	3.0		0.3	0.3	V	T_A = Worst Case
		4.5		0.4	0.4		
		5.5		0.5	0.5		
I_{OLD}	Minimum Dynamic	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 3)	5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		2.0	20.0	µA	V_{IN} = V_{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V) (Note 5)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	3.3	1.5	9.5	13.5	1.5	15.0	ns
		5.0	1.5	7.0	10.0	1.5	11.0	
t_{PHL}	Propagation Delay	3.3	1.5	7.5	11.5	1.5	13.0	ns
		5.0	1.5	6.0	8.5	1.5	9.5	

Note 5: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$	$T_A = -40°C$ to $+85°C$		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$
	Input Voltage	5.5	1.5	2.0	2.0		or $V_{CC} - 0.1V$
V_{IL}	Maximum LOW Level	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$
	Output Voltage	5.5	1.5	0.8	0.8		or $V_{CC} - 0.1V$
V_{OH}	Minimum HIGH Level	4.5	4.49	434	4.4	V	$I_{OUT} = -50\mu A$
	Output Voltage	5.5	5.49	5.4	5.4		
						V	$V_{IN} = V_{IL}$ or V_{IH}
		4.5		3.86	3.76		$I_{OH} = -24$ mA
		5.5		4.86	4.76		$I_{OH} = -24$ mA (Note 6)
V_{OL}	Maximum LOW Level	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
	Output Voltage	5.5	0.001	0.1	0.1		
						V	$V_{IN} = V_{IL}$ or V_{IH}
		4.5		0.36	0.44		$I_{OL} = 24$ mA
		5.5		0.36	0.44		$I_{OL} = 24$ mA (Note 6)
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	µA	$V_I = V_{CC}$, GND
$V_{H(MAX)}$	Maximum Hysteresis	4.5		1.4	1.4	V	T_A = Worst Case
		5.5		1.6	1.6		
$V_{H(MIN)}$	Minimum Hysteresis	4.5		0.4	0.4	V	T_A = Worst Case
		5.5		0.5	0.5		
V_{t+}	Maximum Positive	4.5		2.0	2.0	V	T_A = Worst Case
	Threshold	5.5		2.0	2.0		
V_{t-}	Minimum Negative	4.5		0.8	0.8	V	T_A = Worst Case
	Threshold	5.5		0.8	0.8		
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current (Note 7)	5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent	5.5		2.0	20.0	µA	$V_{IN} = V_{CC}$
	Supply Current						or GND

Note 6: All outputs loaded; thresholds on input associated with output under test.

Note 7: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for ACT

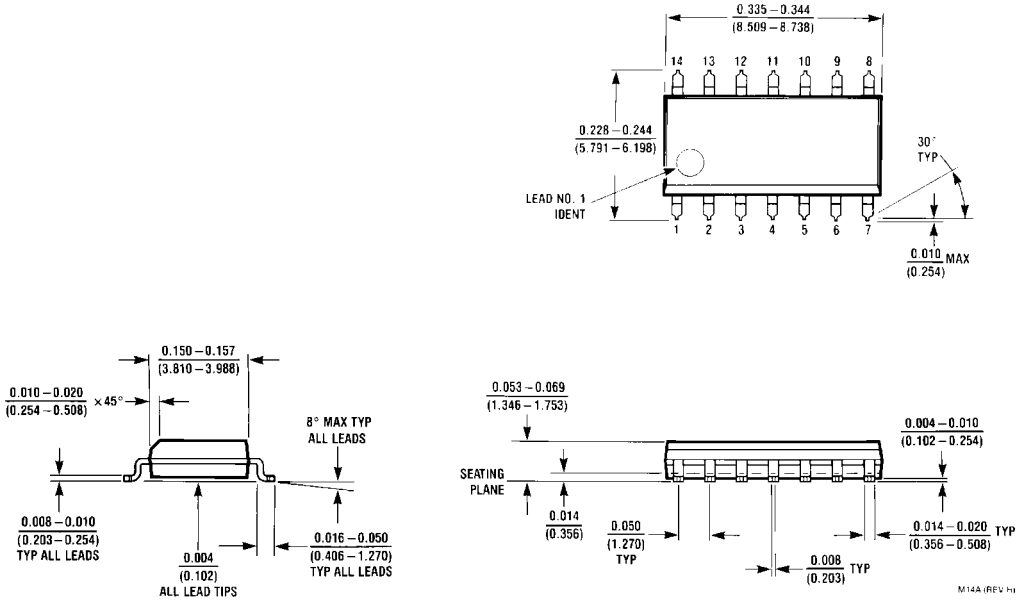
Symbol	Parameter	V_{CC} (V) (Note 8)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay Data to Output	5.0	3.0	8.0	10.0	3.0	11.0	ns
t_{PHL}	Propagation Delay Data to Output	5.0	3.0	8.0	10.0	3.0	11.0	ns

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

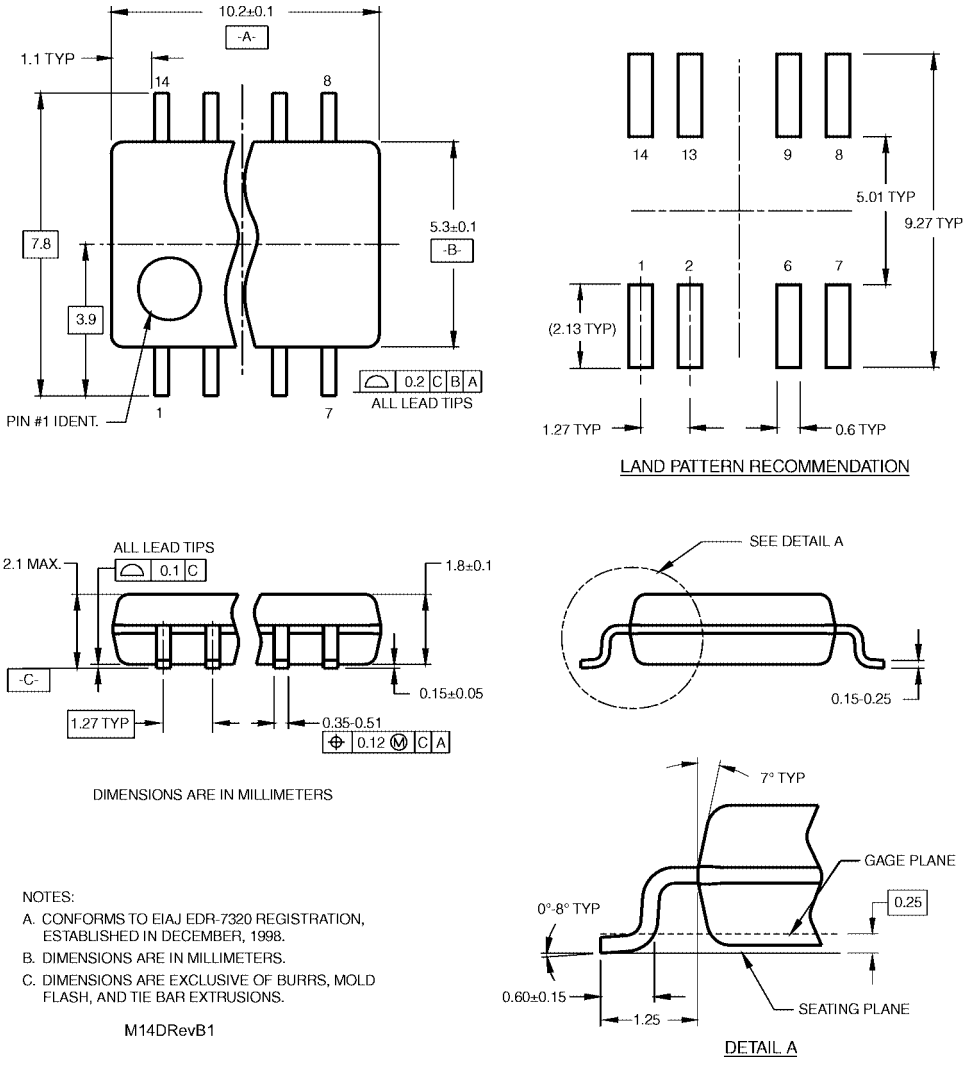
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance for AC for ACT	25.0 80	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

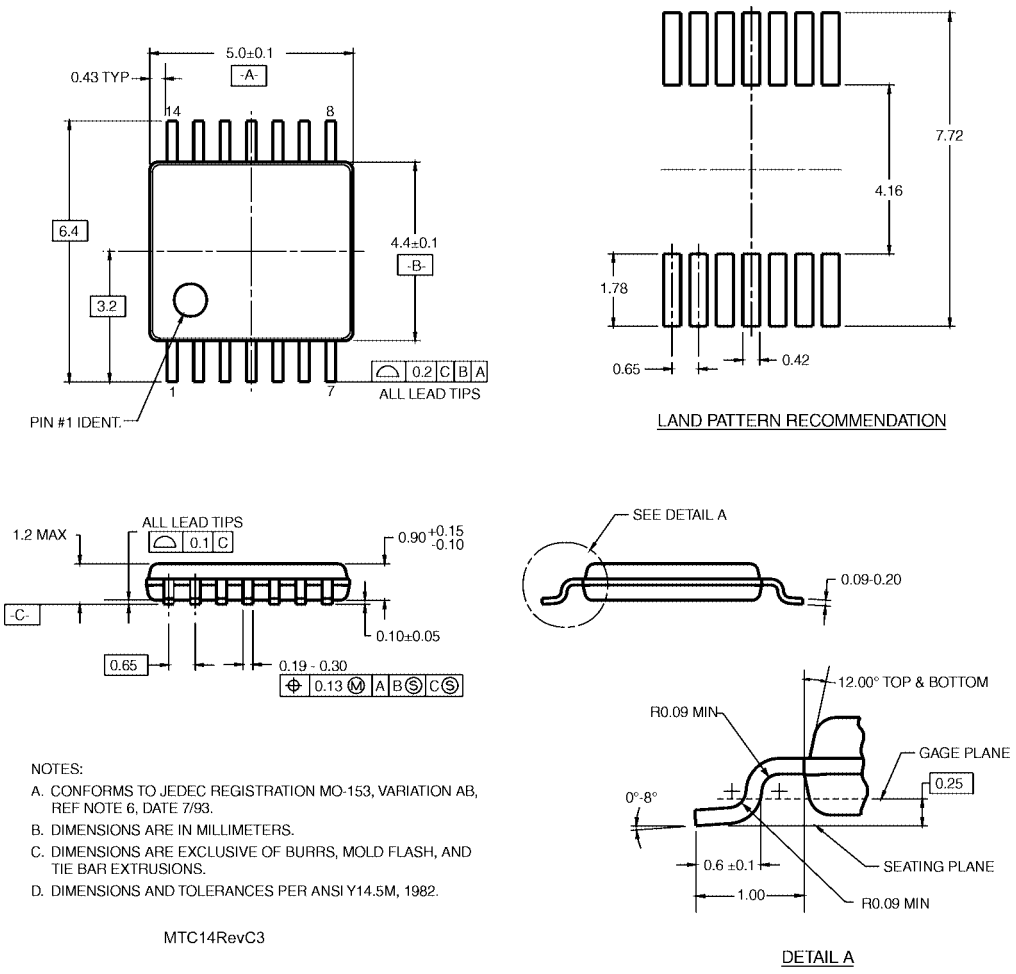
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

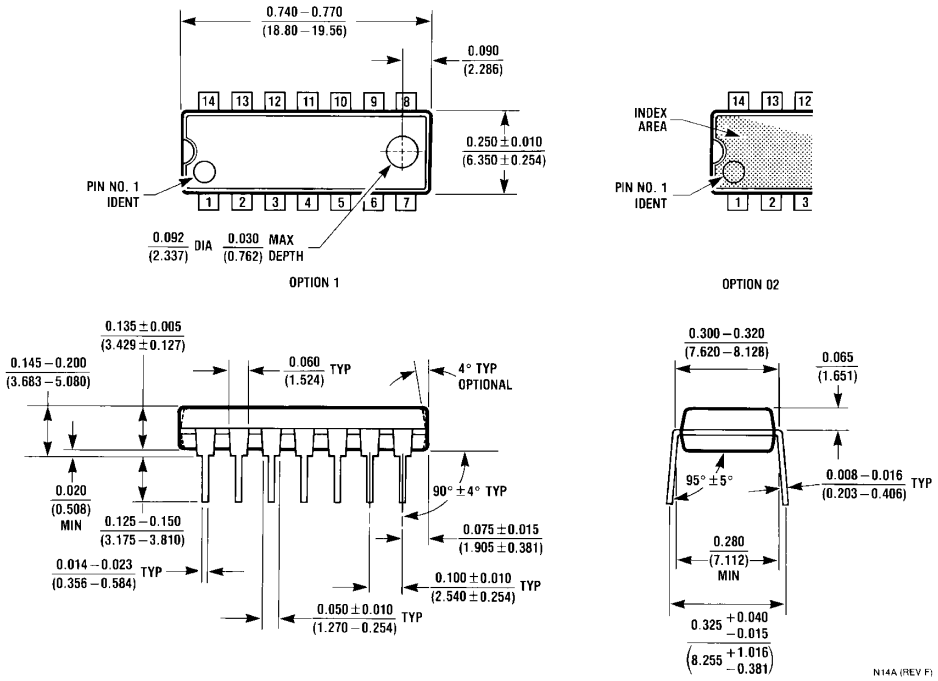
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

4.4 74AC245

FAIRCHILD SEMICONDUCTOR™

November 1988
Revised November 1999

74AC245 • 74ACT245
Octal Bidirectional Transceiver with 3-STATE Inputs/Outputs

General Description

The AC/ACT245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at both the A and B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

Features

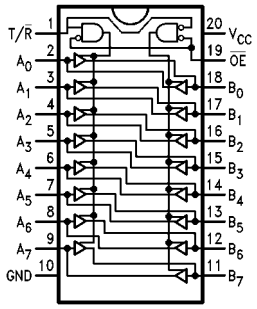
- I_{CC} and I_{OZ} reduced by 50%
- Noninverting buffers
- Bidirectional data path
- A and B outputs source/sink 24 mA
- ACT245 has TTL-compatible inputs

Ordering Code:

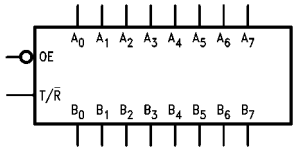
Order Number	Package Number	Package Description
74AC245SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300” Wide Body
74AC245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC245PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
74ACT245SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300” Wide Body
74ACT245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ACT245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT245PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering code.

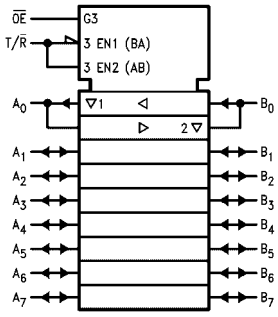
Connection Diagram



Logic Symbols



IEEE/IEC



Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A 3-STATE Inputs or 3-STATE Outputs
B_0–B_7	Side B 3-STATE Inputs or 3-STATE Outputs

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate (ΔV/Δt)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	T_A = +25°C	T_A = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level	3.0	1.5	2.1	2.1		V_{OUT} = 0.1V
	Input Voltage	4.5	2.25	3.15	3.15	V	or V_{CC} − 0.1V
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level	3.0	1.5	0.9	0.9		V_{OUT} = 0.1V
	Input Voltage	4.5	2.25	1.35	1.35	V	or V_{CC} − 0.1V
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level	3.0	2.99	2.9	2.9		
	Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.46		I_{OH} = −12 mA
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 2)
V_{OL}	Maximum LOW Level	3.0	0.002	0.1	0.1		
	Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.44		I_{OL} = 12 mA
		4.5		0.36	0.44	V	I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 2)
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V_I = V_{CC}, GND
I_{OLD}	Dynamic Output	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}	Current Minimum (Note 3)	5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V_{IN} = V_{CC} or GND
I_{OZT}	Maximum I/O						V_I (OE) = V_{IL}, V_{IH}
	Leakage Current	5.5		± 0.3	± 3.0	μA	V_I = V_{CC}, GND
							V_O = V_{CC}, GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24$ mA
		5.5		4.86	4.76		$I_{OH} = -24$ mA (Note 5)
V_{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24$ mA
		5.5		0.36	0.44		$I_{OL} = 24$ mA (Note 5)
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	Dynamic Output Current Minimum (Note 6)	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.3	±3.0	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V) (Note 7)	$T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	3.3	1.5	5.0	8.5	1.0	9.0	ns
		5.0	1.5	3.5	6.5	1.0	7.0	
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	3.3	1.5	5.0	8.5	1.0	9.0	ns
		5.0	1.5	3.5	6.0	1.0	7.0	
t_{PZH}	Output Enable Time	3.3	2.5	7.0	11.5	2.0	12.5	ns
		5.0	1.5	5.0	8.5	1.0	9.0	
t_{PZL}	Output Enable Time	3.3	2.5	7.5	12.0	2.0	13.5	ns
		5.0	1.5	5.5	9.0	1.0	9.5	
t_{PHZ}	Output Disable Time	3.3	2.0	6.5	12.0	1.0	12.5	ns
		5.0	1.5	5.5	9.0	1.0	10.0	
t_{PLZ}	Output Disable Time	3.3	2.0	7.0	11.5	1.5	13.0	ns
		5.0	1.5	5.5	9.0	1.0	10.0	

Note 7: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

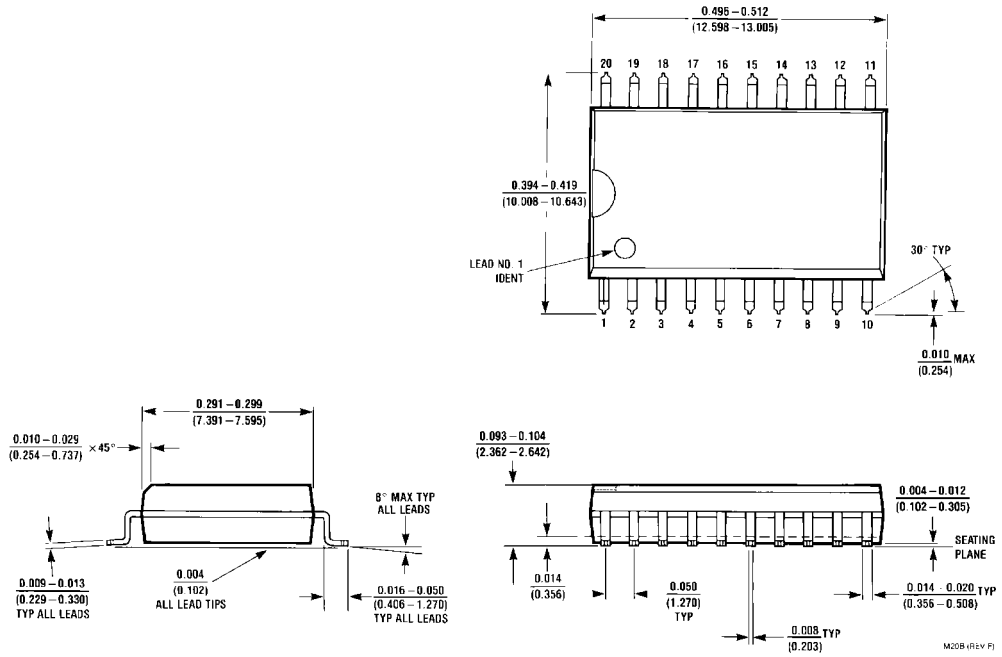
Symbol	Parameter	V_{CC} (V) (Note 8)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	5.0	1.5	4.0	7.5	1.5	8.0	ns
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	5.0	1.5	4.0	8.0	1.0	9.0	ns
t_{PZH}	Output Enable Time	5.0	1.5	5.0	10.0	1.5	11.0	ns
t_{PZL}	Output Enable Time	5.0	1.5	5.5	10.0	1.5	12.0	ns
t_{PHZ}	Output Disable Time	5.0	1.5	5.5	10.0	1.0	11.0	ns
t_{PLZ}	Output Disable Time	5.0	2.0	5.0	10.0	1.5	11.0	ns

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

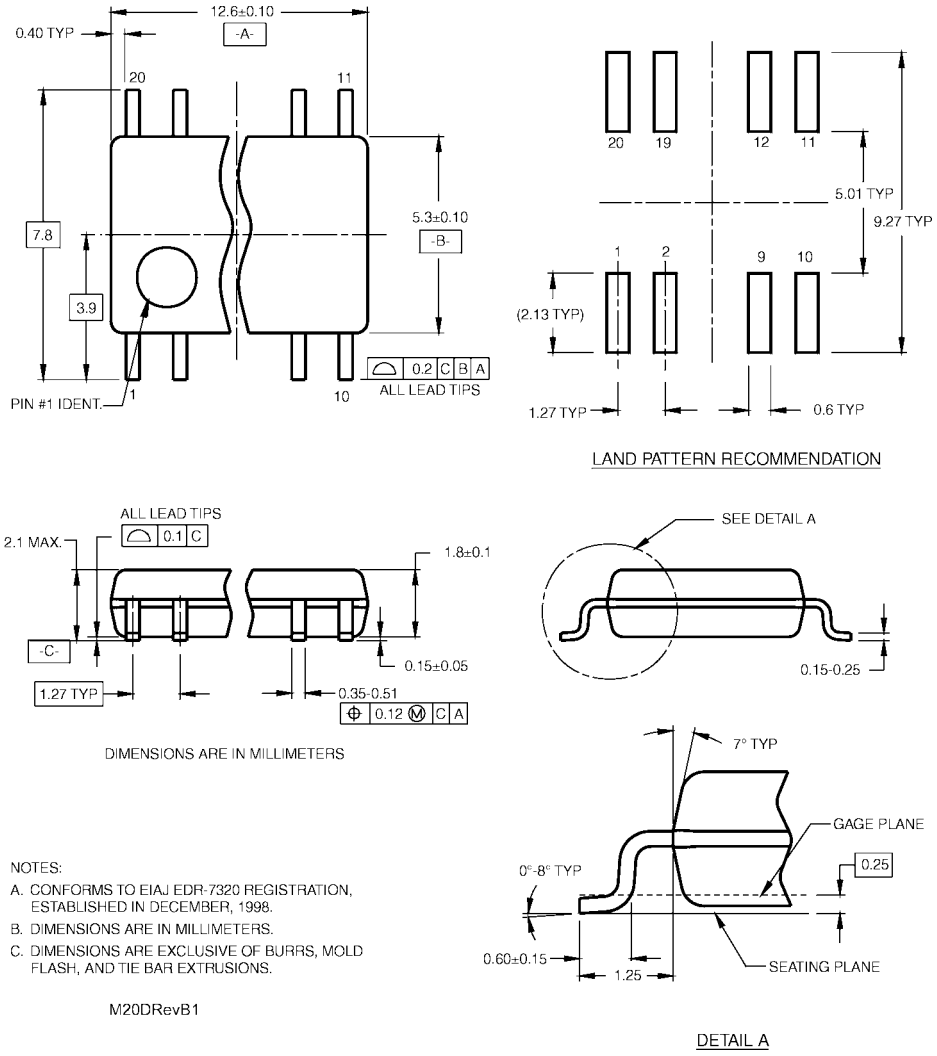
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
$C_{I/O}$	Input/Output Capacitance	15.0	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	45.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

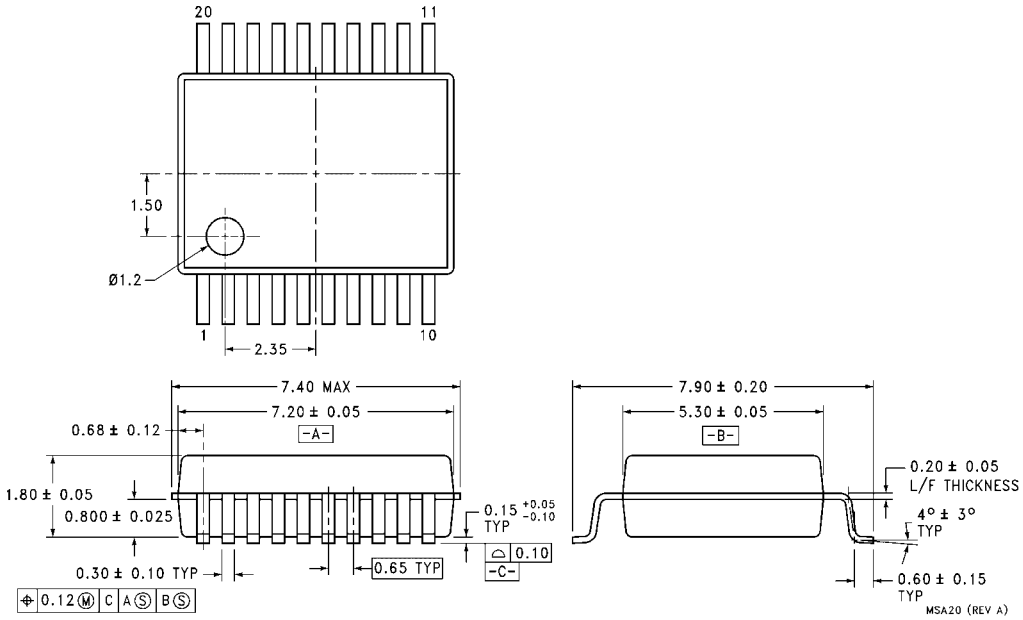
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

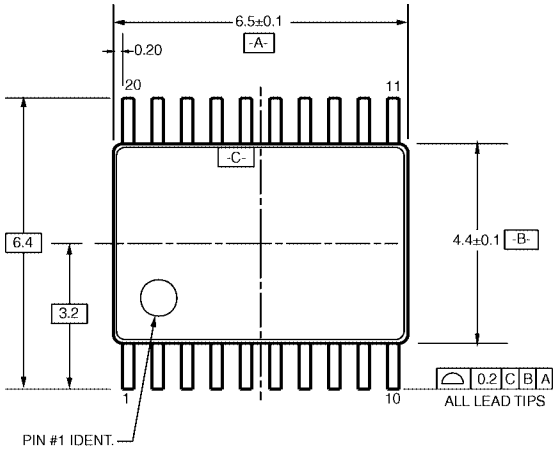
20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

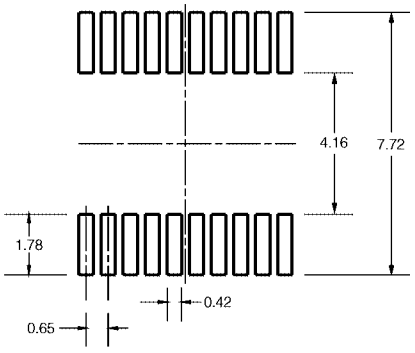
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



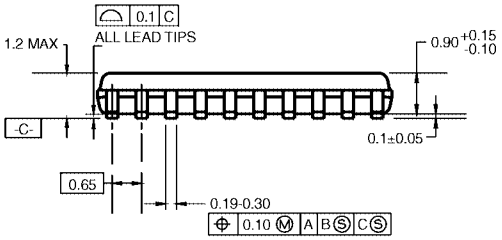
20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

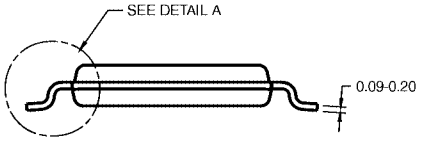
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





LAND PATTERN RECOMMENDATION





DIMENSIONS ARE IN MILLIMETERS

NOTES:

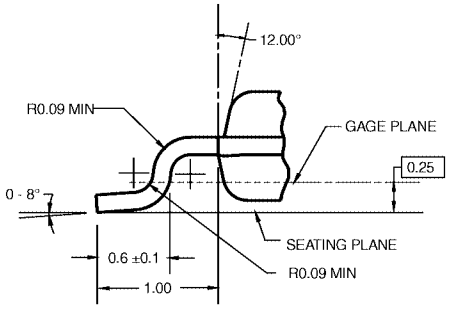
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

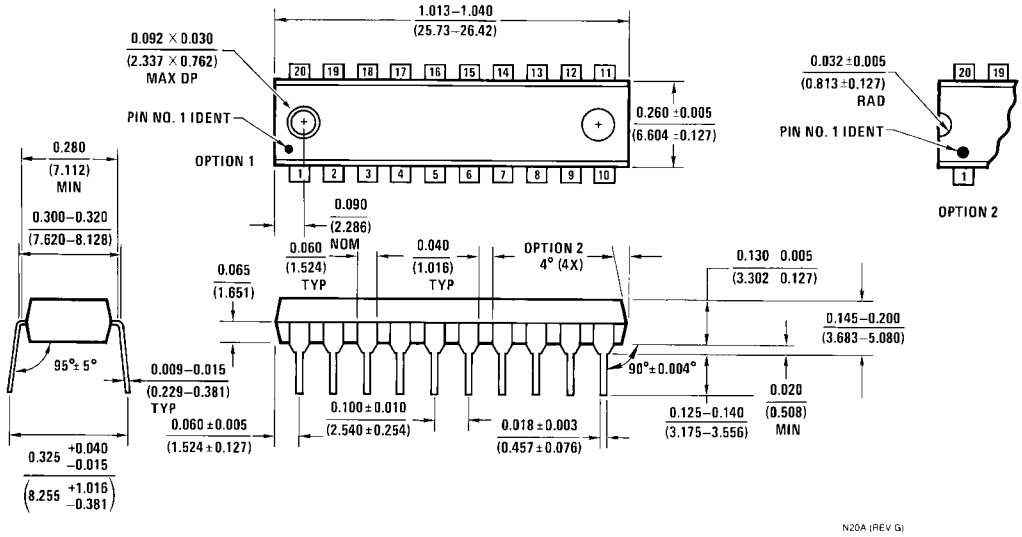
MTC20RevD1



DETAIL A

20-Lead Thin Shrink Small Outline Package, (TSSOP) JEDEC
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

4.5 AN1095

Design of Isolated Converters Using Simple Switchers

National Semiconductor
Application Note 1095
Ravindra Ambatipudi
August 1998

INTRODUCTION

Isolated converters are required to provide electrical isolation between two interrelated systems. Isolation between the power source and the load is required in certain applications in order to meet safety specifications such as UL1459, which necessitates 500V of isolation for telecom applications.

Isolation must be provided between all the input and output stages of the power converter. Thus, isolation must be provided in the power stage and the control loop. Power stage isolation is generally provided using transformer. Isolation in the feedback/control loop is often provided through an opto-coupler (also known as opto-isolator).

Transformers are well suited for power stage isolation, since they are known for providing good dielectric barrier between two systems, with the ability to have multiple outputs. Transformers also allow stepping up or stepping down of the input voltage.

In isolated switching power supplies, opto-couplers are very widely used to provide isolation in the feedback loop. Opto-couplers do an excellent job of isolation, minimizing circuit complexity and reducing cost. One of the disadvantages of using an opto-coupler is its low bandwidth. The bandwidth of the converter is reduced by the introduction of an extra pole in the control loop gain of the converter. This is not a problem in conventional low frequency converters. However, in modern high-frequency converters, the opto-coupler imposes severe restrictions on control loop bandwidth/speed.

Another disadvantage of using opto-isolator is the large unit-to-unit variation in the current transfer ratio (CTR). CTR or the coupling efficiency is defined as the ratio of opto-isolator transistor collector current to the diode current. The loop gain is directly proportional to CTR gain. Hence, high variation in CTR imposes constraints on control loop design.

PART I. DESIGN OF OPTO-ISOLATED POWER SUPPLY

Design Approach

With the advent of SIMPLE SWITCHER™, and the associated "Switchers Made Simple" software (SMS4.2.1, SMS3.3), the non-isolated converter design has become very simple. However, the non-isolated converters can be modified to isolated converters very easily. The procedure for design of opto-isolated converter is as follows:

Step 1: Design the power stage components for a flyback converter using SMS4.2.1/3.3. The "Switchers Made Simple" software can be used to design the transformer, input/output capacitors, output rectifier, clamping network, etc.

Step 2: Modify the feedback/control loop by introducing a secondary side controller (such as LM3411) and an opto-isolator for feedback isolation. Also, disable the internal reference in the Simple Switcher.

Design of Power Stage Components

The first step in the design process is to enter the converter specifications (shown in *Table 1*) in the input menu of the "Switchers Made Simple" software. Using these specifications, the software will design the power stage components. The following example will be based on Switchers Made Simple 4.2.1 (SMS4.2.1) and the associated LM258X flyback converters.

If the input specifications are entered as shown in *Figure 1*, SMS4.2 will design a buck converter instead of flyback. In order to design a flyback converter when the output voltage is lower than input voltage levels, it is necessary to enter initially a fictitious output voltage value which is greater than V_{IN}(min). The software will then design a flyback. Now, go to the main menu and change input requirements. Change the fictitious output voltage value to the required value. If the output voltage is greater than the minimum input voltage, these extra steps are not necessary.

TABLE 1. Isolated Power Converter Specifications (Example)

Input Voltage	10V to 30V
Output Voltage	5V
Load (maximum)	2A
Operating Temp. Range	0˚C to 70˚C

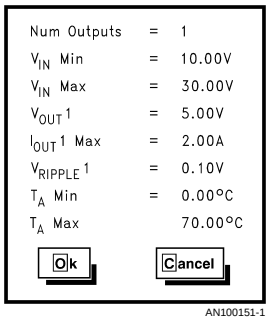


FIGURE 1. Enter the Converter Specifications in the Input Menu of SMS4.2.1

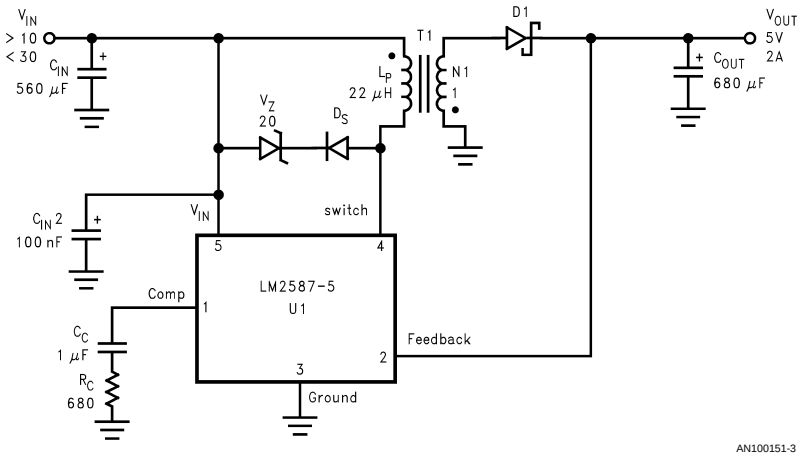
Modify the component values, input specs, etc. to suit the requirements. The software will design all the power stage components and give a list of vendors. In the example shown in *Figure 2*, the component values were entered manually to produce a surface mount design.

The isolation voltage of the transformer is not listed in the software. The isolation voltage is generally mentioned in the transformer manufacturer's catalog. Select a transformer taking into consideration the isolation voltage. Any of the transformers listed in the LM258X Simple Switcher data sheets meet UL1459 spec, and are suitable for telecom applications.

Input Parameters			Operating Values			Component Values		
V_{IN} Min	=	10.00V	Mode	=	Cont	Pri L	=	22.00 µH
V_{IN} Max	=	30.00V	Frequency	=	100.00 kHz	Leakage L	=	470.00 nH
$V_{OUT}1$	=	5.00V	Duty Cycle	=	38.68%	N1 sec/pri	=	1.00
$I_{OUT}1$ Max	=	2.00A	IC I_{PK} Max	=	5.00A	V_Z	=	20.00V
$V_{RIPPLE}1$	=	0.10V	IC I_{PK}	=	4.04A	C_{IN}	=	560.00 µF
T_A Min	=	0.00°C	L I_{PP}	=	1.56A	C_{IN} ESR	=	40.00 mΩ
T_A Max		70.00°C	Efficiency	=	72.88%	C_C	=	1.00 µF
			IC Pd	=	1.71W	R_C	=	1.00 kΩ
			IC T_J	=	106.21°C	IC Heatsnk	=	19.23°C/W
			Diode1 Pd	=	1.00W	Pri DCR	=	35.84 mΩ
			Xformer Pd	=	0.32W	$C_{OUT}1$	=	660.00 µF
			Zener Pd	=	0.49W	$C_{OUT}1$ ESR	=	24.00 mΩ
			I_{IN} Avg	=	1.37A			
			Cross Freq	=	2.40 kHz			
			Phase Marg	=	89.78 Deg			
			$V_{OUT}1$ P-P	=	96.61 mV			

AN100151-2

FIGURE 2. Main Screen of SMS4.2.1 Summarizes the Design



AN100151-3

FIGURE 3. Circuit Designed using SMS4.2.1

The software will also produce a schematic of the non-isolated converter as shown in *Figure 3*. This concludes the first step of the design process.

Modification of Control Loop for Isolated Design

The second step in designing an opto-isolated converter is to modify the feedback loop by using a secondary controller such as LM3411 and to use an opto-isolator for feedback isolation. To do this, connect an opto-coupler between the secondary controller and the compensation pin for feedback isolation. Power stage isolation is provided by the transformer.

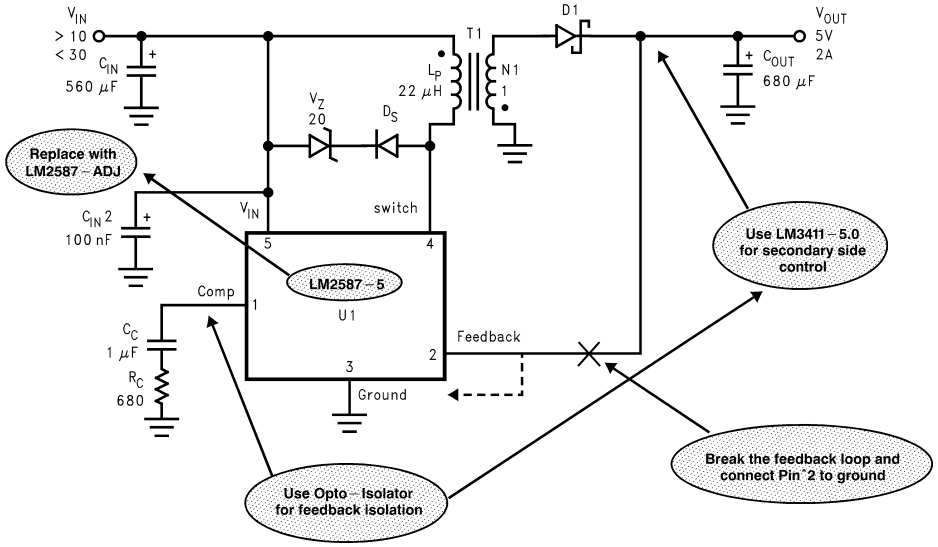


FIGURE 4. Modification of Non-Isolated Flyback to Isolated Flyback

The reference and the error amplifier internal to LM2587 have to be disabled in order to avoid interaction with the reference in secondary controller and to avoid excessive gain in the feedback loop. *Figure 5* shows the internal block diagram of LM2587. By connecting the feedback pin to ground and by connecting the opto-coupler output to the compensation pin, the error-amp is by-passed. For this reason, any voltage option of the LM2587 can be used. This completes the design of the isolated converter.

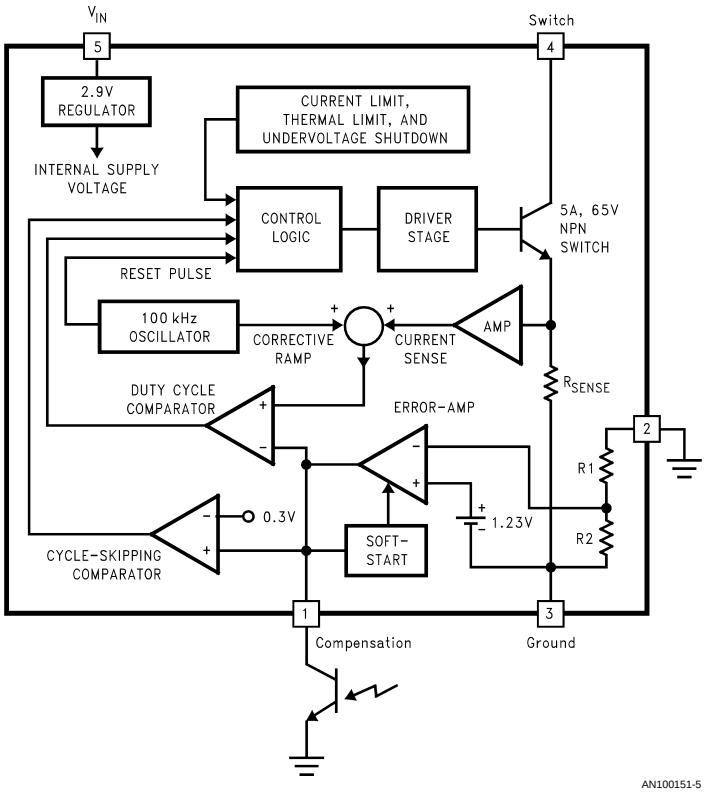


FIGURE 5. LM2587 Block Diagram; Grounding Feedback Pin Disables Error Amplifier, Opto-Coupler Delivers Feedback to Compensation Pin Instead

Figure 6 shows the circuit diagram of an LM2587 based opto-isolated flyback power supply. With the LM2587 error amplifier disabled, the feedback control now consists of LM3411-5.0 secondary side controller and the opto-isolator. Resistors R_o and R_d are required for biasing the opto-isolator. Capacitor C_s is required for soft-start.

Note: Short Circuit Protection. In LM258X switchers, the soft-start comparator and the short-circuit protection are both controlled by the feedback pin voltage. At start-up, when the output voltage is zero, the soft-start comparator is activated and the output gradually increases to the nominal value. After this, the soft-start comparator gets disabled and the short-circuit protection is enabled. Now if the output is shorted, the frequency will change to 25% of normal operating frequency.

The short-circuit protection is activated only after the soft-start is disabled. In the isolated converter, the feedback pin is grounded. The converter never comes out of soft-start mode. So the short-circuit protection (which changes the frequency to 25 kHz under short circuit conditions) never gets activated. Hence, an external circuit is required for short-circuit protection.

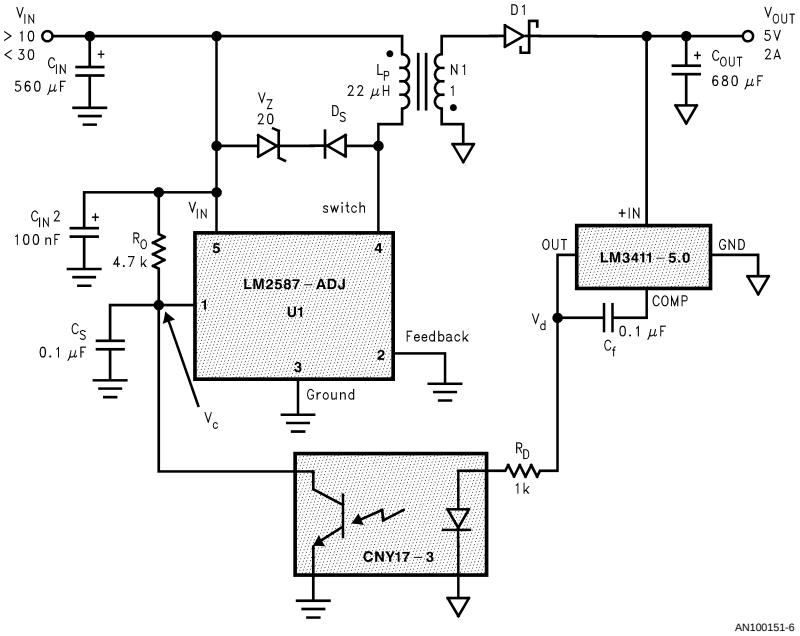


FIGURE 6. 10 Watt Opto-Isolated Flyback Converter

Selection of Compensation Components

The compensation circuit design involves selection of the opto-coupler output resistance, R_o, the opto-coupler input resistance, R_d, and the feedback capacitance, C_f. The compensator transfer function is the small-signal transfer function from the output voltage, V_O to the control voltage, V_c. The transfer function, A(s) is given by:

$$A(s) = \frac{CTR \times R_o}{R_d}\left(1 + \frac{1}{sC_fR_f}\right)$$

Thus, the compensator is a two pole, one zero compensator. In the above equation, *CTR* is the opto-coupler current transfer ratio or coupling-efficiency. The power stage transfer function is a one pole, one zero (esr) compensator (in the frequency range of interest). Choose R_o and R_d such that voltage V_c is always more than 0.3V. Also, the maximum voltage on the compensation pin should be no more than 2V.

Choose C_f to place a zero to cancel the power stage pole, as shown in *Figure 7*. If the compensator is designed as shown above, the loop gain should have very good phase margin and gain margin. In *Figure 7*,

$$f_z = \frac{1}{2\pi C_f 94K}, \quad f_{p1} = \frac{1}{2\pi C_o R_L}$$

$$f_{esr} = \frac{1}{2\pi C_o R_{esr}}$$

where f_{p1} is the frequency of the power stage pole in current mode converter, f_z is the compensator zero, and f_{esr} is the esr zero. f_c is the loop cross over frequency. f_{p2} is the pole(s) created due to current mode control (located at high frequencies close to half the switching frequency).

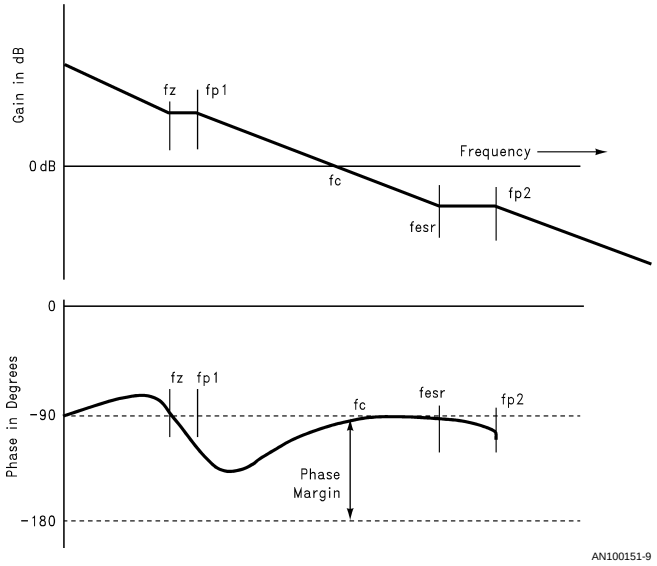


FIGURE 7. The Estimated Loop Response

The loop gain measured on the experimental converter shown in *Figure 6*, is shown in *Figure 8*. The bandwidth and phase margin are very much lower than expected.

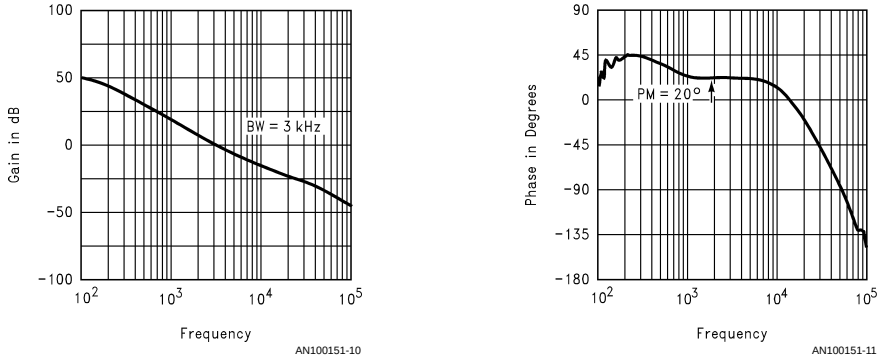


FIGURE 8. Measured Loop Gain of the Experimental Converter (Bandwidth = 3 kHz and Phase Margin = 20˚)

Since the bandwidth and phase margin are very low, a transient step of 0 to 1A produces a very poor transient response, as shown in *Figure 9*. This also indicates poor stability in the control loop.

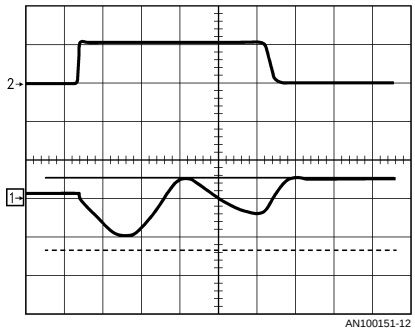


FIGURE 9. Transient Response for a Step Change in Load from 0 to 1A

PART II. IMPROVING TRANSIENT RESPONSE OF OPTO-ISOLATED CONVERTERS

What Causes the Divergence Between Estimated and Measured Results?

The converter shown in *Figure 6* uses an opto-isolator CNY17-3 for feedback isolation and LM3411 for secondary side control. Since this converter is operated at 100 kHz switching frequency, then it is desired to have its loop cross-over at around 10 kHz–20 kHz for superior transient performance. However, the opto-coupler CNY17-3 used in this configuration has a −3 dB frequency of 5 kHz–10 kHz depending on the resistance R_o shown in *Figure 6*. The opto-coupler pole will introduce a phase-shift of more than 45˚ at around 10 kHz as shown in *Figure 10*. Because this fact was not taken into consideration while designing the compensator or loop gain, the measured phase margin and the bandwidth are lower than what was estimated.

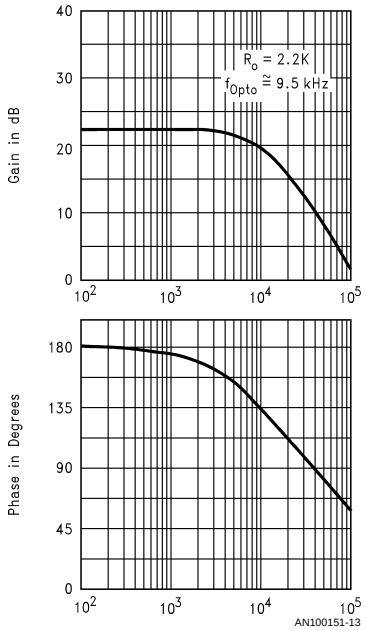


FIGURE 10. Opto-Coupler CNY17-3 Adds More Than 45˚ of Phase Shift at the Desired Loop Bandwidth of 10 kHz

What Limits the Bandwidth of the Opto-Coupler?

The severe bandwidth limitations of the opto-coupler is due entirely to the characteristics of the opto-coupler photo-transistor. When forward current is passed through the opto-coupler diode, it emits infra-red radiation. This radiant energy is transmitted through an optical coupling medium and falls on the surface of the photo-transistor. In order to make the photo-transistor base region sensitive to light, and to minimize the losses in radiant energy transfer, the photo-transistors are designed to have a very large base-collector junction area and a very thick base region. This results in a very large base capacitance, Cob. This capacitance is typically in the order of several pico farads. However, this gets effectively multiplied due to the Miller effect, resulting in a very large Miller capacitance Com. The Miller capacitance is in the order of several nana farads.

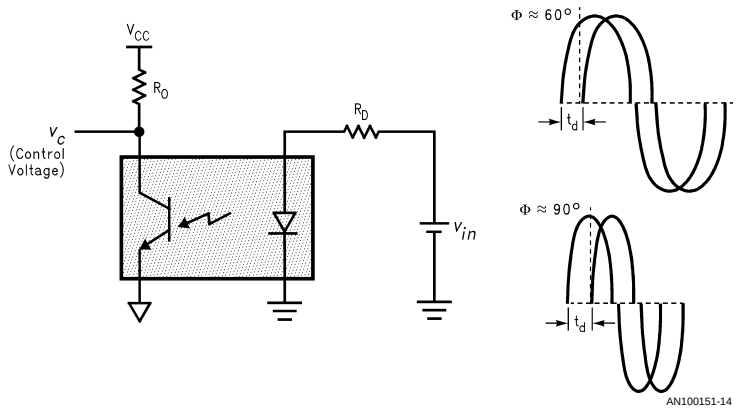


FIGURE 11. Opto-Coupler Transmission Delay Adds Phase Change at High Frequencies (as the frequency of the input sinusoid increases, the phase shift between the input and output increases linearly)

The Miller capacitance Com, coupled with the resistance R_o, will produce a pole in its transfer function. This pole should be taken into consideration while designing the compensation circuit.

It can also be observed from the opto-isolator characteristics that the phase changes very dramatically at very high frequencies. This is due to the inherent delay in transmission of radiant energy through the optical medium. If the input signal to the opto-coupler, as shown in *Figure 11*, is a sinusoid, the output signal is also a sinusoid, but phase shifted due to the delay. As the frequency of this sinusoid increases, the phase shift increases, almost linearly. The phase shift will increase linearly only if this shift is due to time delay.

How To Solve The Opto-Coupler Bandwidth Problems?

The control loop bandwidth can be improved in three ways:

1. The phase margin can be improved by reducing the system cross-over frequency. However, the transient performance of the converter is sacrificed.
2. Opto-isolators with better frequency characteristics (such as MOC8101) can be used. However, these opto-couplers are more expensive.
3. The opto-isolator pole can be compensated by introducing an additional zero in the control loop. This requires proper prediction of opto-coupler pole.

Estimation of The Opto-Coupler Pole

The opto-coupler pole can be estimated in a number of ways. One method is to characterize the pole by actual bench measurements. *Figure 12* shows the bench measurement setup for characterization of an opto-coupler using a network analyzer. A signal is injected at the opto-coupler input and frequency of this signal is swept over the frequency range of interest. The input signal is measured with probe A and the output signal with probe B. By taking the ratio of the input signal to the output signal, the frequency characteristics are obtained.

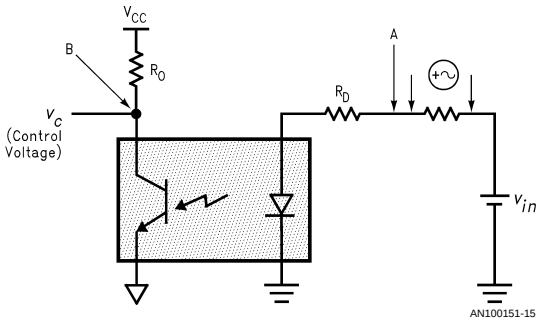


FIGURE 12. Bench Measurement Setup for Frequency Characterization of Opto-Coupler Pole Using a Network Analyzer

Figure 13 shows the typical performance curve obtained by actual measurements for the opto-coupler CNY17-3. In this figure, the opto-coupler bandwidth (pole) has been plotted versus the resistance R_o. The opto-coupler pole can be very easily predicted from this curve. As an example, let us predict the pole for CNY17-3 when the resistance, R_o = 5 kΩ. Draw a line parallel to Y-axis at R_o = 5 kΩ. From the point of intersection on the curve, read the corresponding value on Y-axis. The opto-coupler pole would be at 4 kHz.

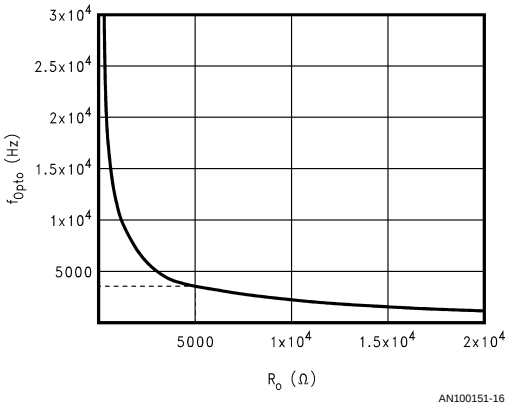


FIGURE 13. Opto-Coupler CNY17-3 Bandwidth versus Resistance R_o

From the results of Part I, it is very obvious that the opto-isolator pole imposes severe restrictions on the control loop bandwidth. This pole can be compensated in two ways:

- If the base connection is available, then by connecting a large resistor between the base and emitter of the opto-coupler photo-transistor, the bandwidth can be improved. However, the opto-coupler gain will reduce by doing so.
- The bandwidth can also be improved by introducing an additional zero in the compensation circuit.

Implementation of the Opto-Coupler Pole Compensation

For the circuit shown in *Figure 6*, the opto-coupler pole can be estimated as discussed in previous sections. However, the soft-start capacitor appears in parallel with opto-coupler device capacitances and influences the position of the opto-coupler pole. The additional zero required to compensate the opto-coupler pole can be obtained by connecting a capacitor in parallel with R_{d1} as shown in *Figure 14*. In the process, this creates an additional pole due to R_{d2} and C_d. To obtain sufficient gain margin and attenuation of high frequency switching noise, this pole can be placed at a high frequency above the cross-over frequency.

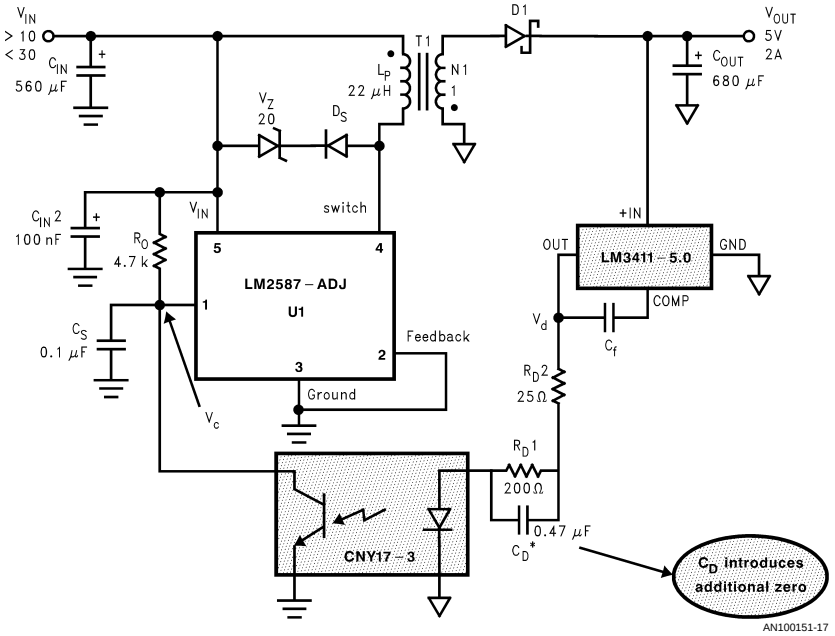


FIGURE 14. Compensating the Opto-Coupler Pole to Improve the Bandwidth Limitations

The modified compensator transfer function is:

$$A_{(S)} = \frac{CTR \times R_o}{R_{d1} + R_{d2}} \left(\frac{sC_cR_f + 1}{sC_cR_f}\right)\left(\frac{sC_dR_{d1} + 1}{sC_dR_{d2} + 1}\right) \text{ (assuming } R_{d2} >> R_{d1})$$

where:

CTR = Opto-coupler current transfer ratio or coupling efficiency

R_f = feedback resistor internal to LM3411 (92k for LM3411-5.0)

C_c = Compensation capacitor

An additional zero can also be obtained by connecting a resistor in series with capacitor C_s, the additional zero required to compensate the opto-coupler pole can be placed at a frequency equal to f_z.

$$f_z = \frac{1}{2\pi R_o C_s}$$

(Assuming C_s is very much larger than the opto-coupler Miller capacitance).

Notice that the compensator transfer function is directly dependent on the opto-coupler CTR, which varies from unit-to-unit, so it is important to take this factor into consideration. This means that an opto-coupler with low CTR variation and guaranteed limits should be used.

Figure 15 shows the loop gain with modified compensator. Significant improvement in bandwidth and phase margin are observed. The loop gain is as expected and shows excellent stability. As expected, the transient response is also improved, as shown in *Figure 16*.

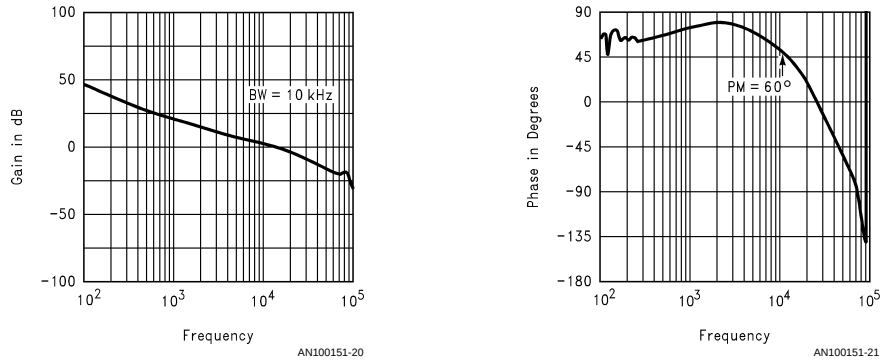


FIGURE 15. Significant Improvement in Bandwidth and Phase Margin is Observed with Opto-Coupler Pole Compensation (Bandwidth = 10 kHz and Phase Margin = 60°)

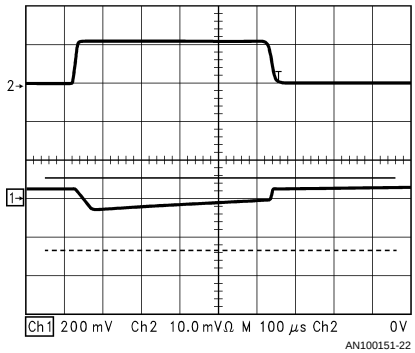


FIGURE 16. Transient Response with Opto-Coupler Pole Compensation (0 to 1A Step-Change in Load)

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

4.6 CNY17

FAIRCHILD
SEMICONDUCTOR®

PHOTOTRANSISTOR OPTOCOUPLERS

DESCRIPTION

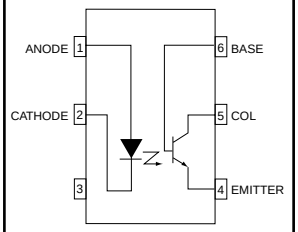
The CNY17 series consists of a Gallium Arsenide IRED coupled with an NPN phototransistor.

CNY17-1 CNY17-3
CNY17-2 CNY17-4

FEATURES

- CNY17-1/2/3 are also available in white package by specifying -M suffix (eg. CNY17-2-M)
- UL recognized (File # E90700)
- VDE recognized
  - -102497 for white package
  - -File #102497
  - -File #94766
  - -Add option V for white package (e.g., CNY17-2V-M)
  - -Add option '300' for black package (e.g., CNY17-2.300)
- Current transfer ratio in select groups
- High BV_{CEO}—70V minimum

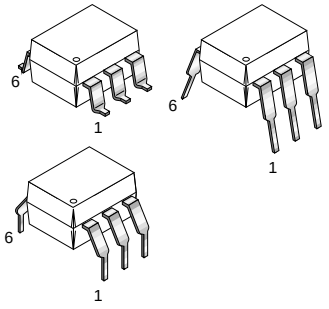
SCHEMATIC



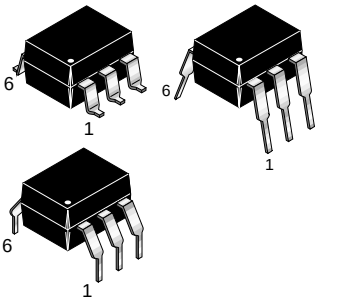
APPLICATIONS

- Power supply regulators
- Microprocessor inputs
- Industrial controls
- Digital logic inputs
- Appliance sensor systems

WHITE PACKAGE (-M SUFFIX)



BLACK PACKAGE (NO -M SUFFIX)



Parameters	Symbol	Device	Value	Units
TOTAL DEVICE Storage Temperature	T_{STG}	All	-55 to +150	°C
Operating Temperature	T_{OPR}	All	-55 to +100	°C
Lead Solder Temperature	T_{SOL}	All	260 for 10 sec	°C
Total Device Power Dissipation @ 25°C (LED plus detector)	P_D	-M	250	mW
		non -M	260	
Derate Linearly From 25°C		-M	2.94	mW/°C
		non -M	3.50	
EMITTER Continuous Forward Current	I_F	-M	60	mA
		non -M	90	
Reverse Voltage	V_R	All	6	V
Forward Current - Peak (1 µs pulse, 300 pps)	I_F(pk)	-M	1.5	A
		non -M	3.0	
LED Power Dissipation 25°C Ambient	P_D	-M	120	mW
		non -M	135	
Derate Linearly From 25°C		-M	1.41	mW/°C
		non -M	1.8	
DETECTOR Detector Power Dissipation @ 25°C	P_D	-M	150	mW
		non -M	200	
Derate Linearly from 25°C		-M	1.76	mW/°C
		non -M	2.67	

ELECTRICAL CHARACTERISTICS (T_A = 25°C Unless otherwise specified.)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameters	Test Conditions	Symbol	Device	Min	Typ	Max	Units
EMITTER	I_F = 60 mA	V_F	-M		1.35	1.65	V
Input Forward Voltage	I_F = 10 mA		non -M		1.15	1.50	
Capacitance	V_F = 0 V, f = 1.0 MHz	C_J	non -M		50		pF
			-M		18		
Reverse Leakage Current	V_R = 6 V	I_R	All		0.001	10	µA
DETECTOR							
Breakdown Voltage Collector to Emitter	I_C = 1.0 mA, I_F = 0	BV_{CEO}	All	70	100		V
Collector to Base	I_C = 10 µA, I_F = 0	BV_{CBO}	All	70	120		V
Emitter to Collector	I_E = 100 µA, I_F = 0	BV_{ECO}	All	7	10		V
Leakage Current Collector to Emitter	V_{CE} = 10 V, I_F = 0	I_{CEO}	All		1	50	nA
Collector to Base	V_{CB} = 10 V, I_F = 0	I_{CBO}	All			20	nA
Capacitance Collector to Emitter	V_{CE} = 0, f = 1 MHz	C_{CE}	All		8		pF
Collector to Base	V_{CB} = 0, f = 1 MHz	C_{CB}	All		20		pF
Emitter to Base	V_{EB} = 0, f = 1 MHz	C_{EB}	All		10		pF

ISOLATION CHARACTERISTICS

Characteristic	Test Conditions	Symbol	Device	Min	Typ**	Max	Units
Input-Output Isolation Voltage	f = 60 Hz, t = 1 min.	V_{ISO}	Black Package	5300			Vac(rms)*
			'-M' White Package	7500			Vac(pk)
Isolation Resistance	V_{I-O} = 500 VDC	R_{ISO}	All	10^{11}			Ω
Isolation Capacitance	V_{I-O} = ∅, f = 1 MHz	C_{ISO}	Black Package		0.5		pF
			'-M' White Package		0.2		

Note
* 5300 Vac(rms) for 1 minute equates to approximately 9000 Vac (pk) for 1 second
** Typical values at T_A = 25°C

TRANSFER CHARACTERISTICS (T_A = 25°C Unless otherwise specified.)

DC Characteristics	Test Conditions	Symbol	Device	Min	Typ	Max	Units
Current Transfer Ratio, Collector to Emitter	I_F = 10 mA, V_{CE} = 5 V	CTR	CNY17-1/-1-M	40		80	%
			CNY17-2/-2-M	63		125	
			CNY17-3/-3-M	100		200	
			CNY17-4	160		320	
Saturation Voltage	I_F = 10 mA, I_C = 2.5 mA	$V_{CE(SAT)}$	All			.40	V
AC Characteristics	**Test Conditions**	**Symbol**	**Device**	**Min**	**Typ**	**Max**	**Units**
Non-Saturated Switching Times Turn-On Time (Fig.19 and Fig.20)	R_L = 100 Ω, I_C = 2 mA, V_{CC} = 10 V	t_{on}	non -M			10	µs
Turn-Off Time (Fig.19 and Fig.20)	R_L = 100 Ω, I_C = 2 mA, V_{CC} = 10 V	t_{off}	non -M			10	µs
Delay Time (Fig.19 and Fig.20)	I_F = 10 mA, V_{CC} = 5 V, R_L = 75 Ω	t_d	-M			5.6	µs
Rise Time (Fig.19 and Fig.20)	I_F = 10 mA, V_{CC} = 5 V, R_L = 75 Ω	t_r	-M			4.0	µs
Storage Time (Fig.19 and Fig.20)	I_F = 10 mA, V_{CC} = 5 V, R_L = 75 Ω	t_s	-M			4.1	µs
Fall Time (Fig.19 and Fig.20)	I_F = 10 mA, V_{CC} = 5 V, R_L = 75 Ω	t_f	-M			3.5	µs
Saturated Switching Times Turn-On Time (Fig.19 and Fig.20)	I_F = 20 mA, V_{CE} = 0.4 V	t_{on}	CNY17-1			5.5	µs
	I_F = 10 mA, V_{CE} = 0.4 V		CNY17-2, CNY17-3, CNY17-4			8.0	
Rise-Time (Fig.19 and Fig.20)	I_F = 20 mA, V_{CE} = 0.4 V	t_r	CNY17-1			4.0	µs
	I_F = 10 mA, V_{CE} = 0.4 V		CNY17-2, CNY17-3, CNY17-4			6.0	
	I_F = 20 mA, V_{CC} = 5 V, R_L = 1 KΩ		CNY17-1-M			4.0	
	I_F = 10 mA, V_{CC} = 5 V, R_L = 1 KΩ		CNY17-2-M,CNY17-3-M			6.0	
Delay Time (Fig.19 and Fig.20)	I_F = 20 mA, V_{CC} = 5 V, R_L =1 KΩ	t_d	CNY17-1-M			5.5	µs
	I_F = 10 mA, V_{CC} = 5 V, R_L =1 KΩ		CNY17-2, CNY17-3			8.0	
Turn-Off Time (Fig.19 and Fig.20)	I_F = 20 mA, V_{CE} = 0.4 V	t_{off}	CNY17-1			34.0	µs
	I_F = 10 mA, V_{CE} = 0.4 V		CNY17-2, CNY17-3, CNY17-4			39.0	
Fall-Time (Fig.19 and Fig.20)	I_F = 20 mA, V_{CE} = 0.4 V	t_f	CNY17-1			20.0	µs
	I_F = 10 mA, V_{CE} = 0.4 V		CNY17-2, CNY17-3, CNY17-4			24.0	
	I_F = 20 mA, V_{CC} = 5 V, R_L =1 KΩ		CNY17-1-M			20.0	
	I_F = 10 mA, V_{CC} = 5 V, R_L = 1 KΩ		CNY17-2-M,CNY17-3-M			24.0	
Storage Time (Fig.19 and Fig.20)	I_F = 20 mA, V_{CC} = 5 V, R_L =1 KΩ	t_s	CNY17-1-M			34.0	µs
	I_F = 10 mA, V_{CC} = 5 V, R_L =1 KΩ		CNY17-2-M,CNY17-3-M			39.0	

Fig.1 Normalized CTR vs. Forward Current (Black Package)

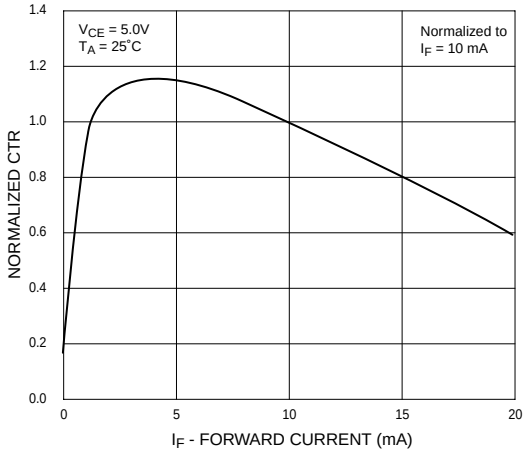


Fig.2 Normalized CTR vs. Forward Current (White Package)

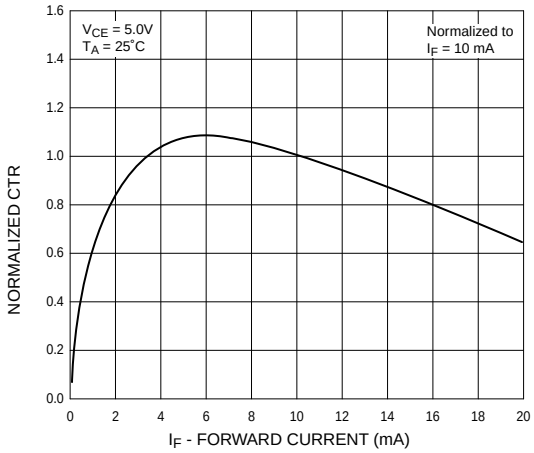


Fig. 3 Normalized CTR vs. Ambient Temperature (Black Package)

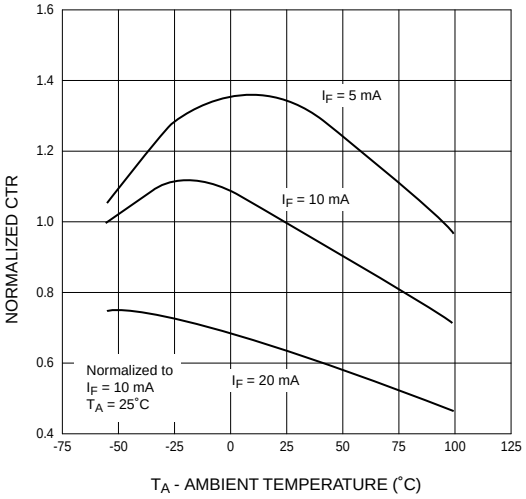


Fig. 4 Normalized CTR vs. Ambient Temperature (White Package)

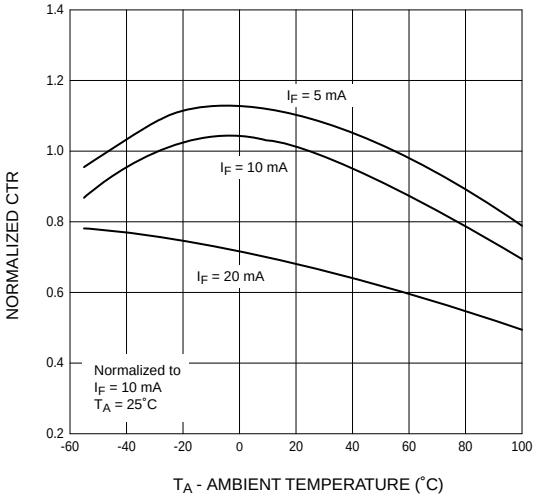


Fig. 5 CTR vs. RBE (Unsaturated) (Black Package)

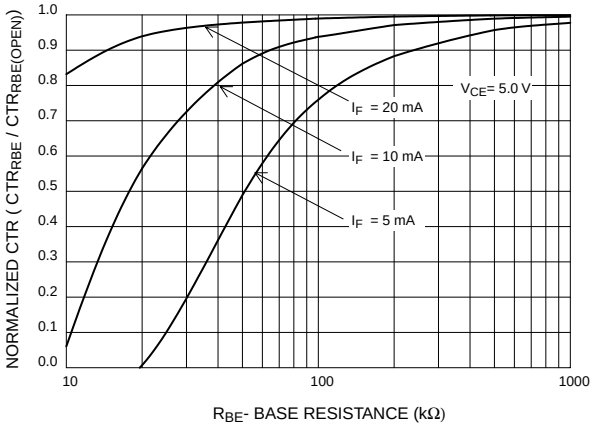


Fig. 6 CTR vs. RBE (Unsaturated) (White Package)

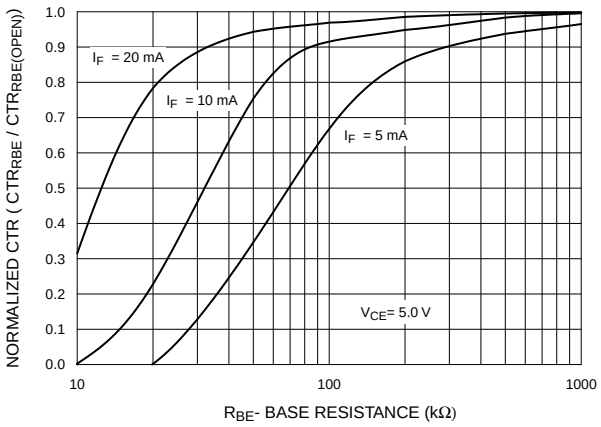


Fig. 7 CTR vs. RBE (Saturated) (Black Package)

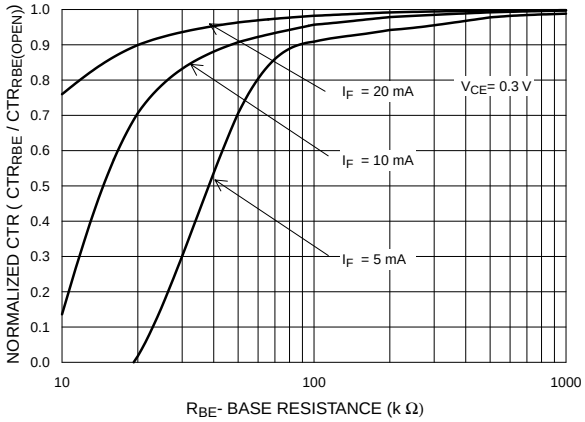


Fig. 8 CTR vs. RBE (Saturated) (White Package)

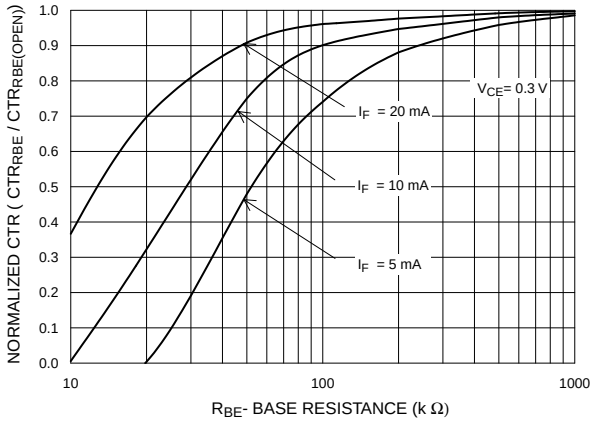


Fig. 9 Switching Speed vs. Load Resistor (Black Package)

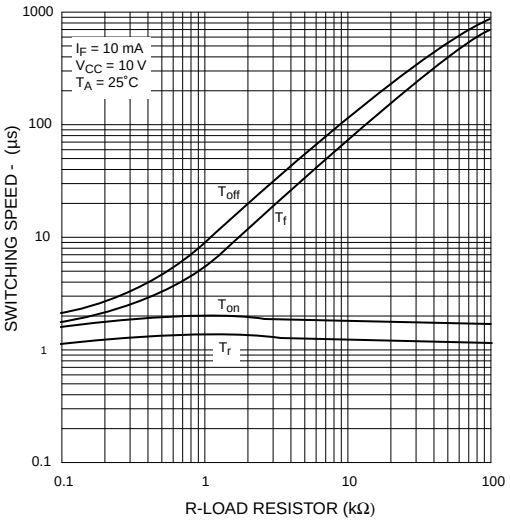


Fig. 10 Switching Speed vs. Load Resistor (White Package)

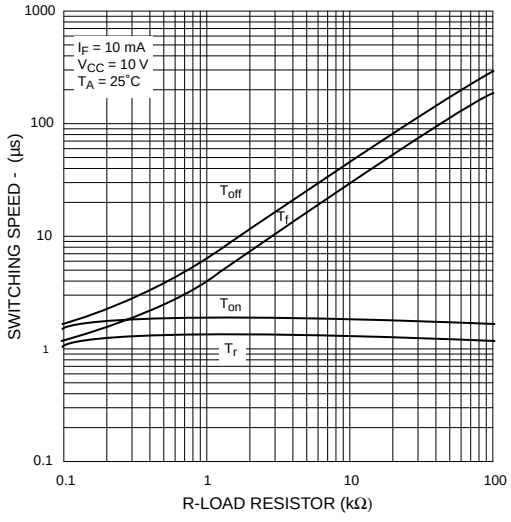


Fig. 11 Normalized t_{on} vs. R_{BE} (Black Package)

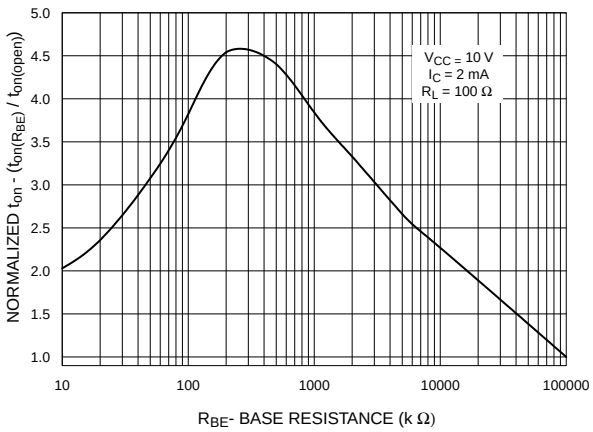


Fig. 12 Normalized t_{on} vs. R_{BE} (White Package)

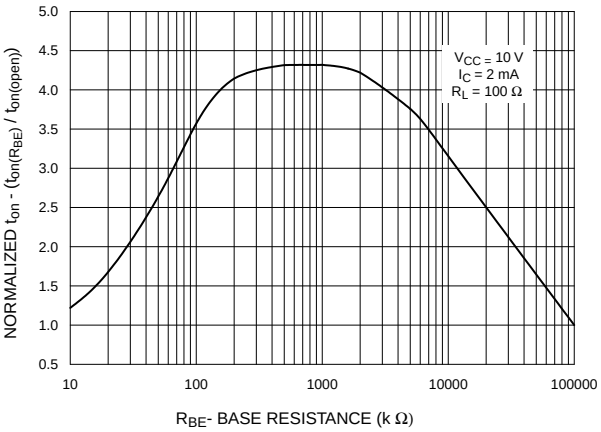


Fig. 13 Normalized t_{off} vs. R_{BE} (Black Package)

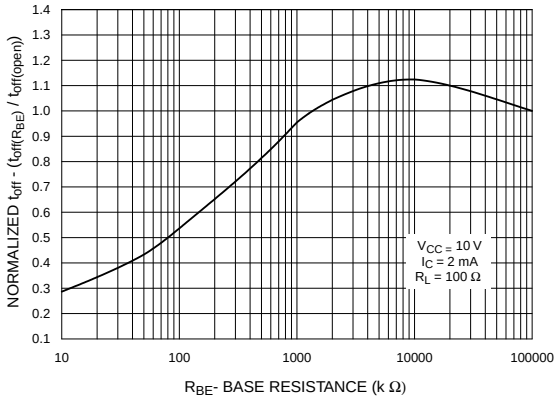


Fig. 14 Normalized t_{off} vs. R_{BE} (White Package)

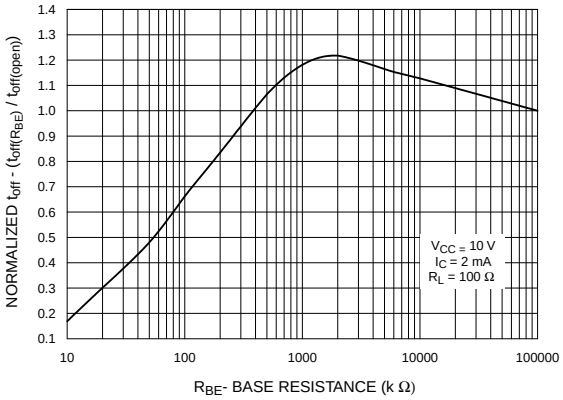


Fig. 15 LED Forward Voltage vs. Forward Current (Black Package)

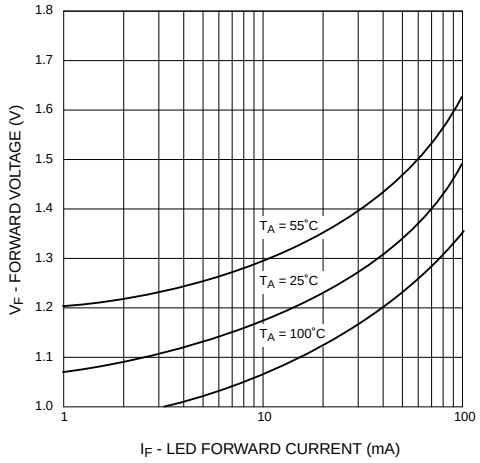


Fig. 16 LED Forward Voltage vs. Forward Current (White Package)

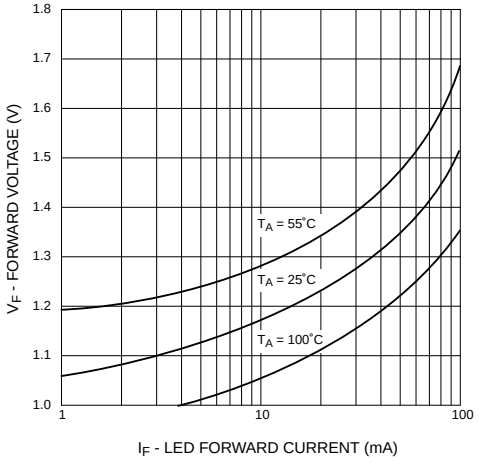


Fig. 17 Collector Current vs. Collector-Emitter Saturation Voltage

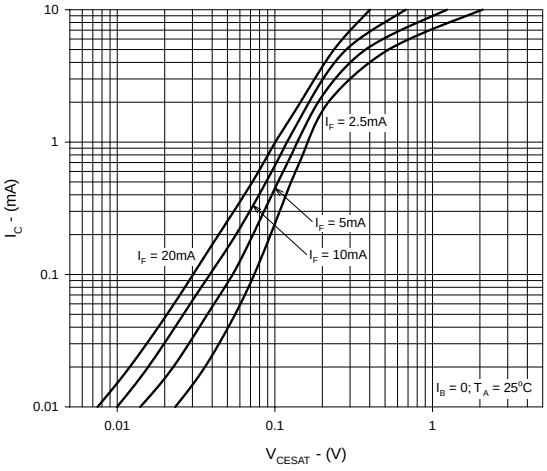
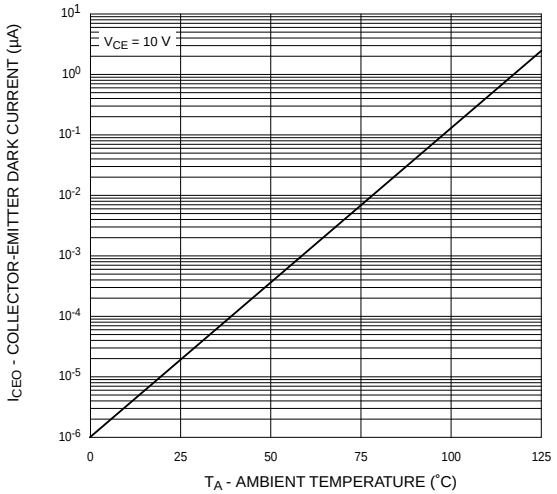


Fig. 18 Dark Current vs. Ambient Temperature (Black Package)



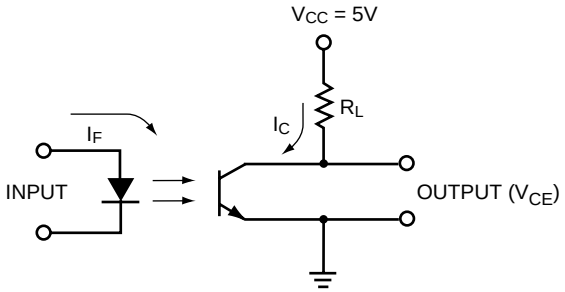


Figure 19. Switching Time Test Circuit

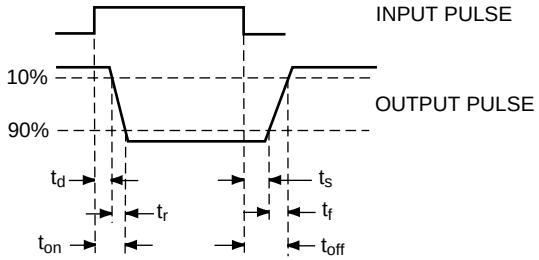
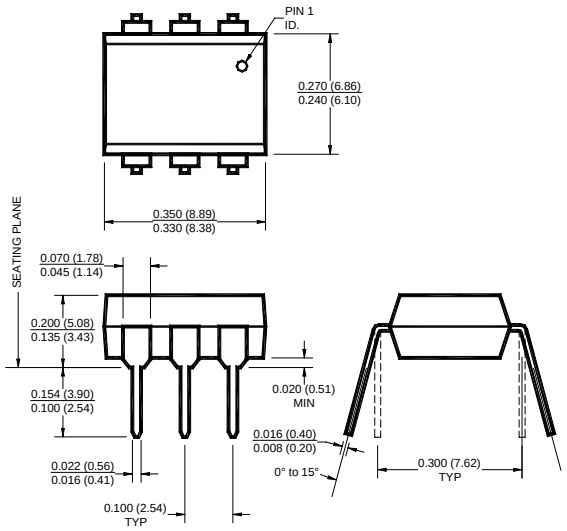


Figure 20. Switching Time Waveforms

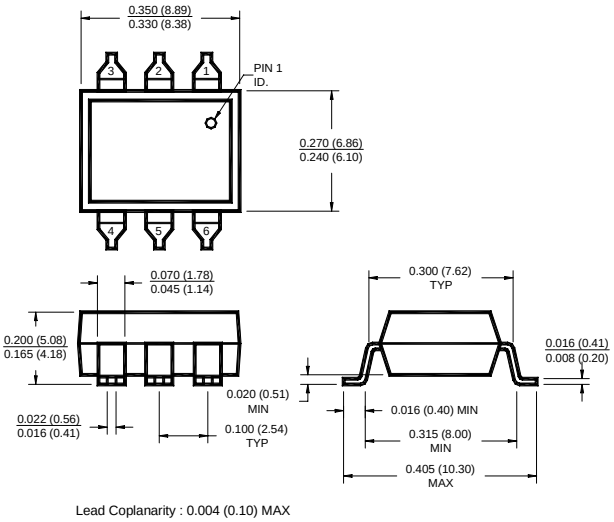
Black Package (No -M Suffix)

CNY17-1	CNY17-3
CNY17-2	CNY17-4

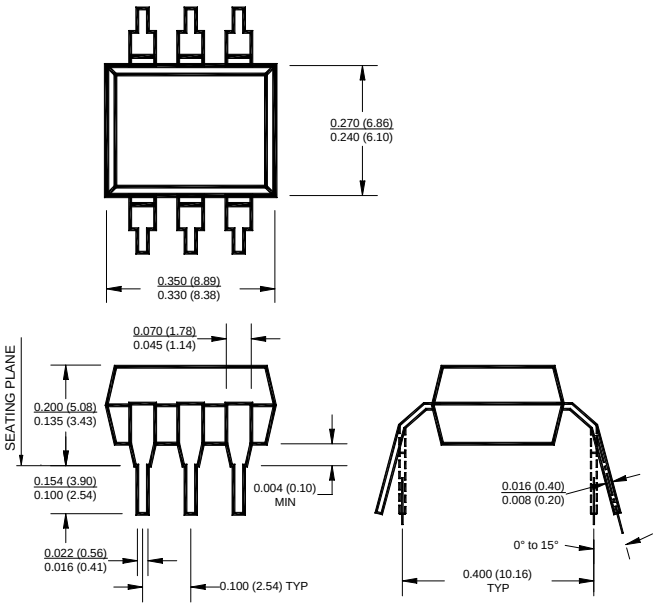
Package Dimensions (Through Hole)



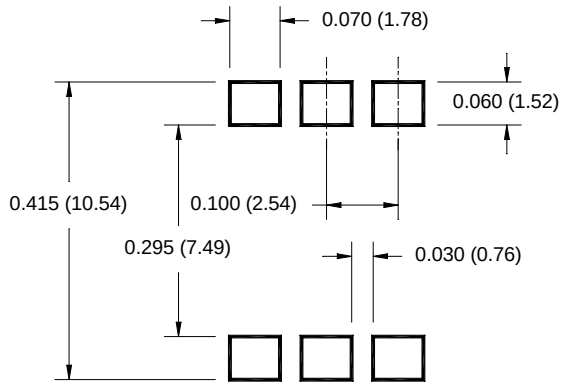
Package Dimensions (Surface Mount)



Package Dimensions (0.4”Lead Spacing)



Recommended Pad Layout for Surface Mount Leadform (Black Package Only)



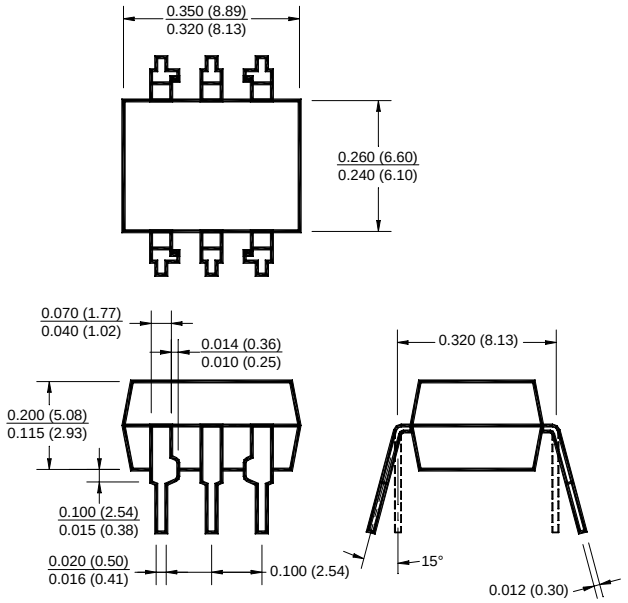
NOTE

All dimensions are in inches (millimeters)

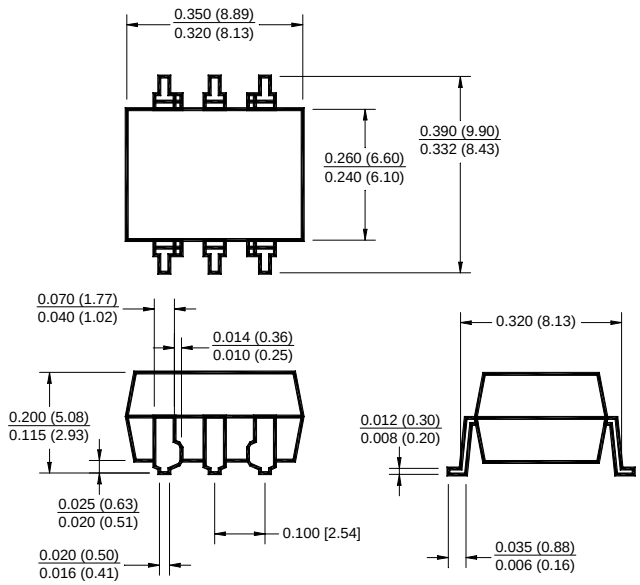
CNY17-1	CNY17-3
CNY17-2	CNY17-4

White Package (-M Suffix)

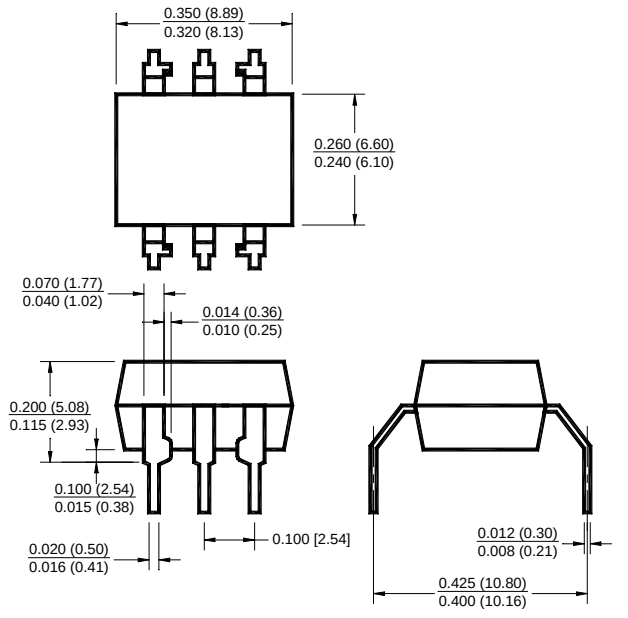
Package Dimensions (Through Hole)



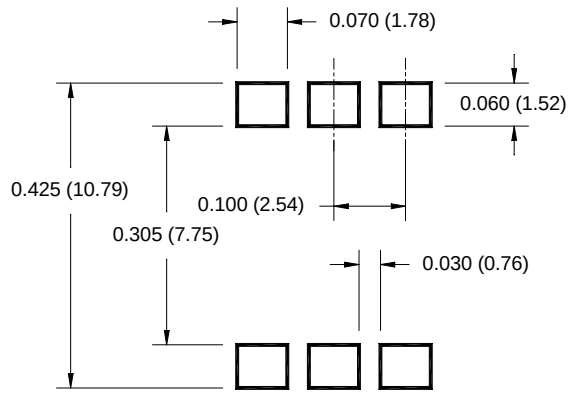
Package Dimensions (Surface Mount)



Package Dimensions (0.4”Lead Spacing)



Recommended Pad Layout for Surface Mount Leadform (White Package Only)



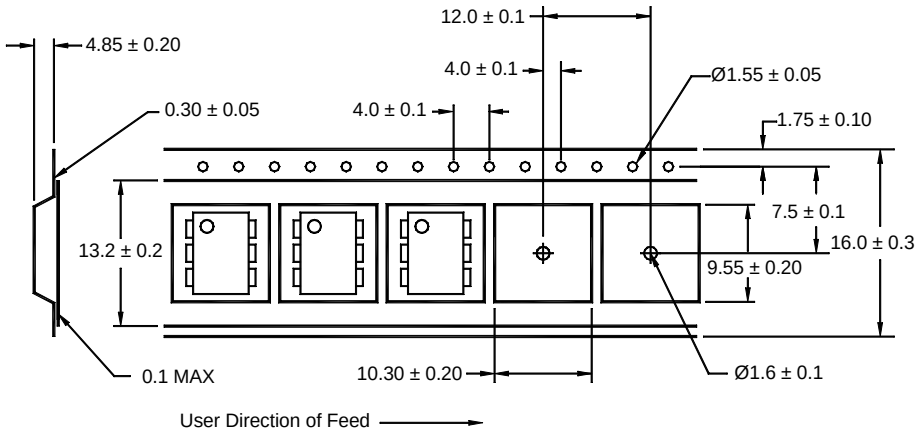
NOTE

All dimensions are in inches (millimeters)

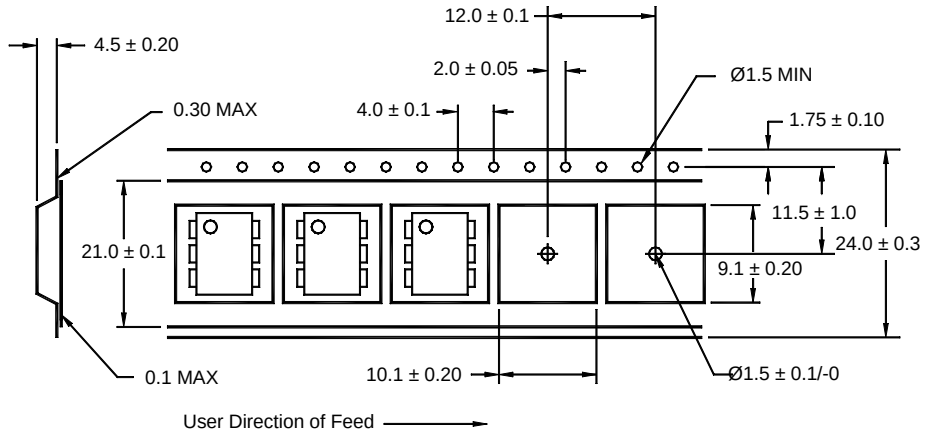
ORDERING INFORMATION

Option	Black Package (No Suffix)	White Package (-m Suffix)	Description
	Order Entry Idenifier		
S	.S	S	Surface Mount Lead Bend
SD	.SD	SR2	Surface Mount; Tape and reel
W	.W	T	0.4” Lead Spacing
300	.300	V	VDE 0884
300W	.300W	TV	VDE 0884, 0.4” Lead Spacing
3S	.3S	SV	VDE 0884, Surface Mount
3SD	.3SD	SR2V	VDE 0884, Surface Mount, Tape & Reel

Carrier Tape Specifications (Black Package, No Suffix)



Carrier Tape Specifications (White Package, -M Suffix)



NOTE

All dimensions are in inches (millimeters)

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body,or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

4.7 CY37256

5V, 3.3V, ISR™ High-Performance CPLDs

Features

- **In-System Reprogrammable™ (ISR™) CMOS CPLDs**
  - **JTAG interface for reconfigurability**
  - **Design changes don't cause pinout changes**
  - **Design changes don't cause timing changes**
- **High density**
  - **32 to 512 macrocells**
  - **32 to 264 I/O pins**
  - **5 dedicated inputs including 4 clock pins**
- **Simple timing model**
  - **No fanout delays**
  - **No expander delays**
  - **No dedicated vs. I/O pin delays**
  - **No additional delay through PIM**
  - **No penalty for using full 16 product terms**
  - **No delay for steering or sharing product terms**
- **3.3V and 5V versions**
- **PCI Compatible**[1]
- **Programmable Bus-Hold capabilities on all I/Os**
- **Intelligent product term allocator provides:**
  - **0 to 16 product terms to any macrocell**
  - **Product term steering on an individual basis**
  - **Product term sharing among local macrocells**
- **Flexible clocking**
  - **4 synchronous clocks per device**
  - **Product Term clocking**
  - **Clock polarity control per logic block**
- **Consistent package/pinout offering across all densities**
  - **Simplifies design migration**
  - **Same pinout for 3.3V and 5.0V devices**
- **Packages**
  - **44 to 400 Leads in PLCC, CLCC, PQFP, TQFP, CQFP, BGA, and Fine-Pitch BGA packages**

General Description

The Ultra37000™ family of CMOS CPLDs provides a range of high-density programmable logic solutions with unparalleled system performance. The Ultra37000 family is designed to bring the flexibility, ease of use, and performance of the 22V10 to high-density CPLDs. The architecture is based on a number of logic blocks that are connected by a Programmable Interconnect Matrix (PIM). Each logic block features its own product term array, product term allocator, and 16 macrocells. The PIM distributes signals from the logic block outputs and all input pins to the logic block inputs.

All of the Ultra37000 devices are electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows, thereby reducing costs. The ISR feature provides the ability to reconfigure the devices without having design changes cause pinout or timing changes. The Cypress ISR function is implemented through a JTAG-compliant serial interface. Data is shifted in and out through the TDI and TDO pins, respectively. Because of the superior routability and simple timing model of the Ultra37000 devices, ISR allows users to change existing logic designs while simultaneously fixing pinout assignments and maintaining system performance.

The entire family features JTAG for ISR and boundary scan, and is compatible with the PCI Local Bus specification, meeting the electrical and timing requirements. The Ultra37000 family features user programmable bus-hold capabilities on all I/Os.

Ultra37000 5.0V Devices

The Ultra37000 devices operate with a 5V supply and can support 5V or 3.3V I/O levels. V_{CCO} connections provide the capability of interfacing to either a 5V or 3.3V bus. By connecting the V_{CCO} pins to 5V the user insures 5V TTL levels on the outputs. If V_{CCO} is connected to 3.3V the output levels meet 3.3V JEDEC standard CMOS levels and are 5V tolerant. These devices require 5V ISR programming.

Ultra37000V 3.3V Devices

Devices operating with a 3.3V supply require 3.3V on all V_{CCO} pins, reducing the device's power consumption. These devices support 3.3V JEDEC standard CMOS output levels, and are 5V tolerant. These devices allow 3.3V ISR programming.

Note:
1. Due to the 5V-tolerant nature of 3.3V device I/Os, the I/Os are not clamped to V_{CC}, PCI V_{IH}=2V.

Selection Guide

5.0V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032	32	5	32	6	200
CY37064	64	5	32/64	6	200
CY37128	128	5	64/128	6.5	167
CY37192	192	5	120	7.5	154
CY37256	256	5	128/160/192	7.5	154
CY37384	384	5	160/192	10	118
CY37512	512	5	160/192/264	10	118

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032	X		X		X			
CY37064	X		X		X			
CY37128		X			X	X		
CY37192			X		X		X	
CY37256			X		X		X	
CY37384					X		X	
CY37512					X	X	X	

Device-Package Offering & I/O Count

Device	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	256-Lead BGA	352-Lead BGA
CY37032	37	37										
CY37064	37	37	37	69		69						
CY37128				69	69	69	133					
CY37192							125					
CY37256							133	133	165		197	
CY37384									165		197	
CY37512									165	165	197	269

3.3V Selection Guide

General Information

Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032V	32	5	32	8.5	143
CY37064V	64	5	32/64	8.5	143
CY37128V	128	5	64/80/128	10	125
CY37192V	192	5	120	12	100
CY37256V	256	5	128/160/192	12	100
CY37384V	384	5	160/192	15	83
CY37512V	512	5	160/192/264	15	83

Speed Bins

Device	200	167	154	143	125	100	83	66
CY37032V				X		X		
CY37064V				X		X		
CY37128V				X	X		X	
CY37192V						X		X
CY37256V				X		X		X
CY37384V							X	X
CY37512V					X		X	X

Shaded areas indicate preliminary speed bins.

Device-Package Offering & I/O Count

Device	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	48-Lead FBGA	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	100-Lead FBGA	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	256-Lead BGA	256-Lead FBGA	352-Lead BGA	400-Lead FBGA
CY37032V	37	37		37												
CY37064V	37	37	37	37	69		69	69								
CY37128V					69	69	69	85	133							
CY37192V									125							
CY37256V									133	133	165		197	197		
CY37384V											165		197			
CY37512V											165	165	197		269	269

Architecture Overview of Ultra37000 Family

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) consists of a completely global routing matrix for signals from I/O pins and feedbacks from the logic blocks. The PIM provides extremely robust interconnection to avoid fitting and density limitations.

The inputs to the PIM consist of all I/O and dedicated input pins and all macrocell feedbacks from within the logic blocks. The number of PIM inputs increases with pin count and the number of logic blocks. The outputs from the PIM are signals routed to the appropriate logic blocks. Each logic block receives 36 inputs from the PIM and their complements, allowing for 32-bit operations to be implemented in a single pass through the device. The wide number of inputs to the logic block also improves the routing capacity of the Ultra37000 family.

An important feature of the PIM is its simple timing. The propagation delay through the PIM is accounted for in the timing specifications for each device. There is no additional delay for traveling through the PIM. In fact, all inputs travel through the PIM. As a result, there are no route-dependent timing parameters on the Ultra37000 devices. The worst-case PIM delays are incorporated in all appropriate Ultra37000 specifications.

Routing signals through the PIM is completely invisible to the user. All routing is accomplished by software—no hand routing is necessary. *Warp*™ and third-party development packages automatically route designs for the Ultra37000 family in a matter of minutes. Finally, the rich routing resources of the Ultra37000 family accommodate last minute logic changes while maintaining fixed pin assignments.

Logic Block

The logic block is the basic building block of the Ultra37000 architecture. It consists of a product term array, an intelligent product-term allocator, 16 macrocells, and a number of I/O cells. The number of I/O cells varies depending on the device used. Refer to *Figure 1* for the block diagram.

Product Term Array

Each logic block features a 72 x 87 programmable product term array. This array accepts 36 inputs from the PIM, which originate from macrocell feedbacks and device pins. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 87 product terms in the array can be created from any of the 72 inputs.

Of the 87 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Four of the remaining seven product terms in the logic block are output enable (OE) product terms. Each of the OE product terms controls up to eight of the 16 macrocells and is selectable on an individual macrocell basis. In other words, each I/O cell can select between one of two OE product terms to control the output buffer. The first two of these four OE product terms are available to the upper half of the I/O macrocells in a logic block. The other two OE product terms are available to the lower half of the I/O macrocells in a logic block.

The next two product terms in each logic block are dedicated asynchronous set and asynchronous reset product terms. The final product term is the product term clock. The set, reset, OE and product term clock have polarity control to realize OR functions in a single pass through the array.

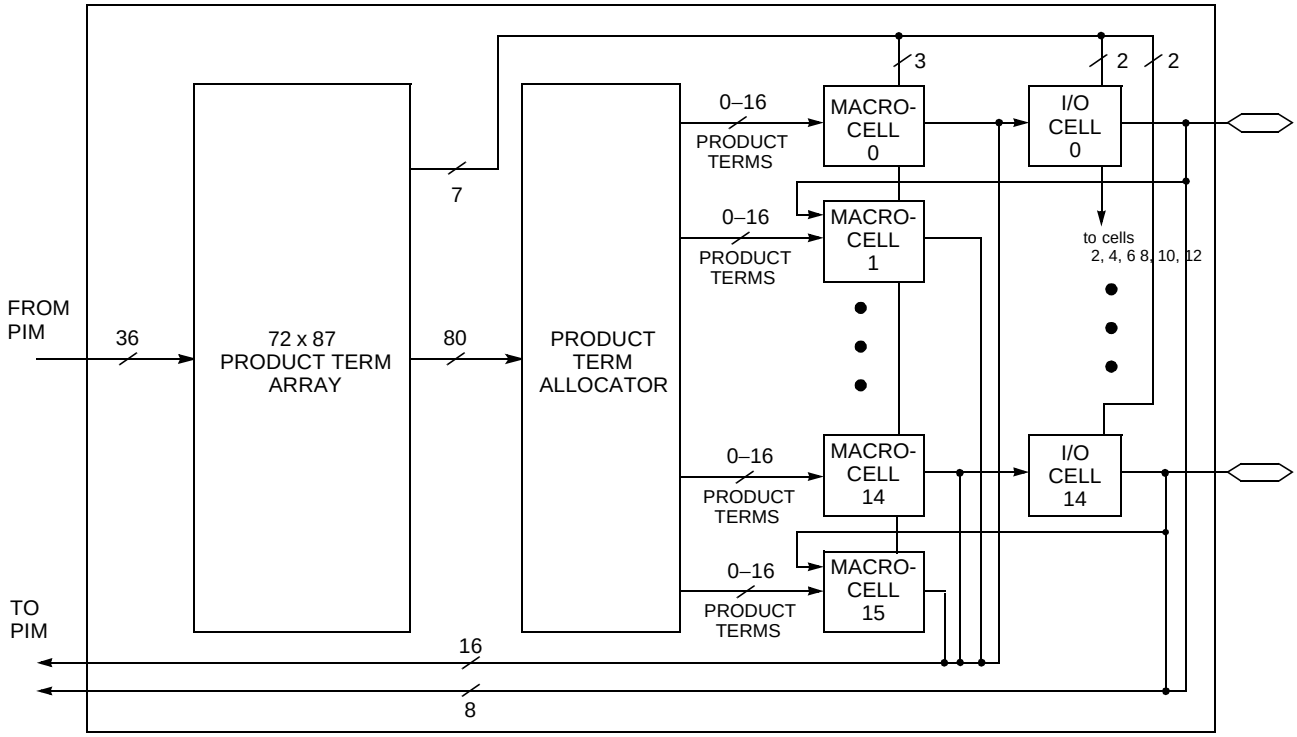


Figure 1. Logic Block with 50% Buried Macrocells

Low-Power Option

Each logic block can operate in high-speed mode for critical path performance, or in low-power mode for power conservation. The logic block mode is set by the user on a logic block by logic block basis.

Product Term Allocator

Through the product term allocator, software automatically distributes product terms among the 16 macrocells in the logic block as needed. A total of 80 product terms are available from the local product term array. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will "steer" ten product terms to one macrocell and three to the other. On Ultra37000 devices, product terms are steered on an individual basis. Any number between 0 and 16 product terms can be steered to any macrocell. Note that 0 product terms is useful in cases where a particular macrocell is unused or used as an input register.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms are only programmed once. The Ultra37000 product term allocator allows sharing across groups of four output macrocells in a variable fashion. The software automatically takes advantage of this capability—the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All worst-case steering and sharing configurations have been incorporated in the timing specifications for the Ultra37000 devices.

Ultra37000 Macrocell

Within each logic block there are 16 macrocells. Macrocells can either be I/O Macrocells, which include an I/O Cell which is associated with an I/O pin, or buried Macrocells, which do not connect to an I/O. The combination of I/O Macrocells and buried Macrocells varies from device to device.

Buried Macrocell

Figure 2 displays the architecture of buried macrocells. The buried macrocell features a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a level-triggered latch.

The register can be asynchronously set or asynchronously reset at the logic block level with the separate set and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be set or reset based on an AND expression or an OR expression.

Clocking of the register is very flexible. Four global synchronous clocks and a product term clock are available to clock the register. Furthermore, each clock features programmable polarity so that registers can be triggered on falling as well as rising edges (see the Clocking section). Clock polarity is chosen at the logic block level.

The buried macrocell also supports input register capability. The buried macrocell can be configured to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

I/O Macrocell

Figure 2 illustrates the architecture of the I/O macrocell. The I/O macrocell supports the same functions as the buried macrocell with the addition of I/O capability. At the output of the macrocell, a polarity control mux is available to select active LOW or active HIGH signals. This has the added advantage of allowing significant logic reduction to occur in many applications.

The Ultra37000 macrocell features a feedback path to the PIM separate from the I/O pin input path. This means that if the macrocell is buried (fed back internally only), the associated I/O pin can still be used as an input.

Bus Hold Capabilities on all I/Os

Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND. For more information, see the application note "Understanding Bus-Hold – A Feature of Cypress CPLDs."

Programmable Slew Rate Control

Each output has a programmable configuration bit, which sets the output slew rate to fast or slow. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.

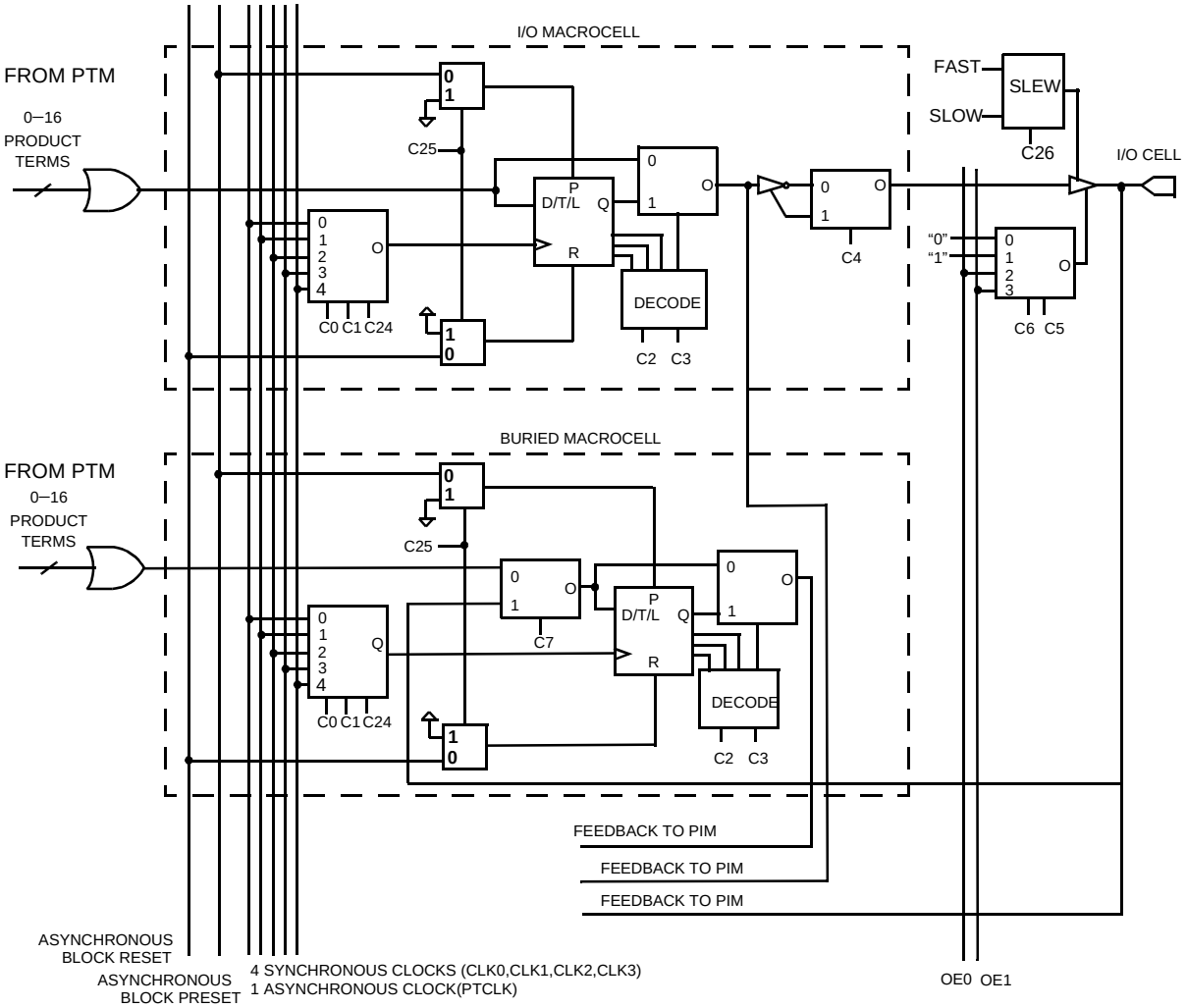


Figure 2. I/O and Buried Macrocells

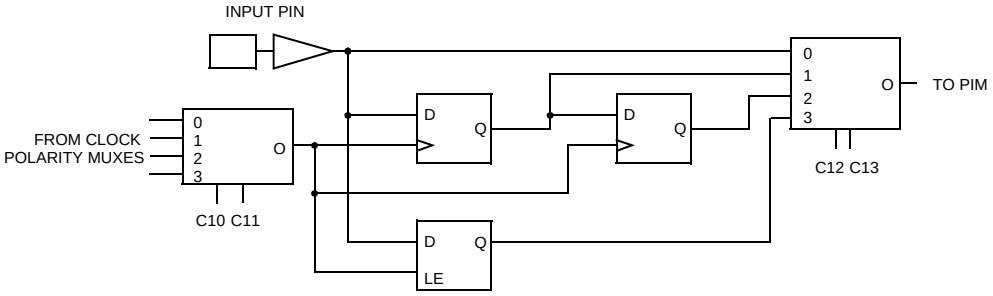


Figure 3. Input Macrocell

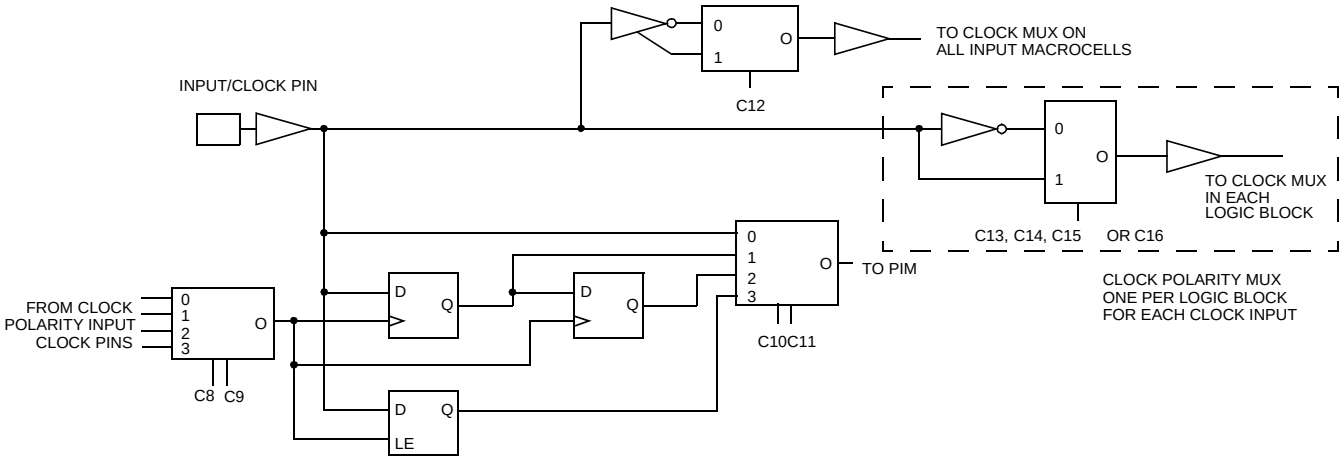


Figure 4. Input/Clock Macrocell

Clocking

Each I/O and buried macrocell has access to four synchronous clocks (CLK0, CLK1, CLK2 and CLK3) as well as an asynchronous product term clock PTCLK. Each input macrocell has access to all four synchronous clocks.

Dedicated Inputs/Clocks

Five pins on each member of the Ultra37000 family are designated as input-only. There are two types of dedicated inputs on Ultra37000 devices: input pins and input/clock pins. *Figure 3* illustrates the architecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control.

Figure 4 illustrates the architecture for the input/clock pins. Like the input pins, input/clock pins can be combinatorial, registered, double-registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input has user-configurable polarity.

Product Term Clocking

In addition to the four synchronous clocks, the Ultra37000 family also has a product term clock for asynchronous clocking. Each logic block has an independent product term clock which is available to all 16 macrocells. Each product term clock also supports user configurable polarity selection.

Timing Model

One of the most important features of the Ultra37000 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used. *Figure 5* illustrates the true timing model for the 167-MHz devices in high speed mode. For combinatorial paths, any input to any output incurs a 6.5-ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input set-up time to the output macrocells for any input is 3.5 ns and the clock to output time is also 4.0 ns. These measurements are for any output and synchronous clock, regardless of the logic used.

The Ultra37000 features:

- No fanout delays
- No expander delays
- No dedicated vs. I/O pin delays
- No additional delay through PIM
- No penalty for using 0–16 product terms
- No added delay for steering product terms
- No added delay for sharing product terms
- No routing delays
- No output bypass delays

The simple timing model of the Ultra37000 family eliminates unexpected performance penalties.

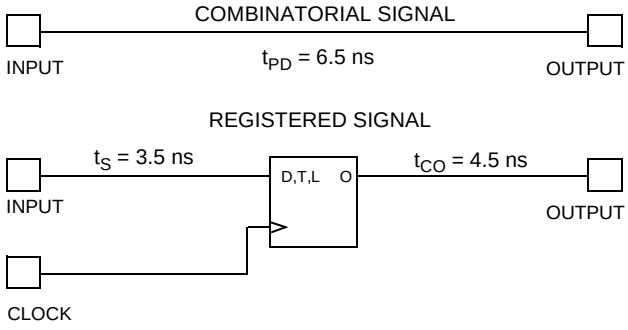


Figure 5. Timing Model for CY37128

JTAG and PCI Standards

PCI Compliance

5V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3V products meet all PCI requirements except for the output 3.3V clamp, which is in direct conflict with 5V tolerance. The Ultra37000 family's simple and predictable timing model ensures compliance with the PCI AC specifications independent of the design.

IEEE 1149.1 Compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode, and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 6*.

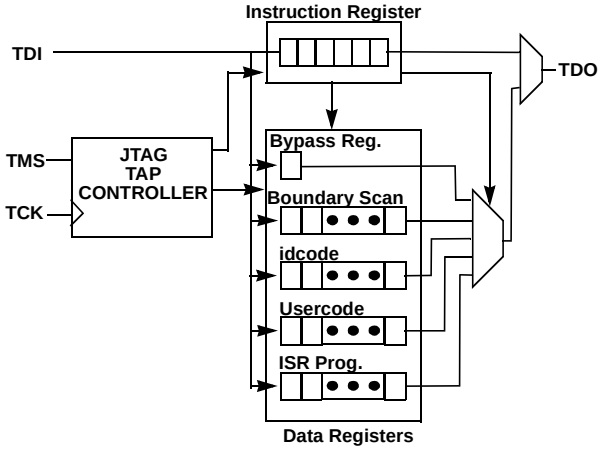


Figure 6. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing resources for pinout flexibility, and a simple timing model for consistent system performance.

Development Software Support

Warp™

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, *Warp* provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor, and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. To facilitate design and debugging, *Warp* provides graphical timing simulation and analysis.

Warp Professional™

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparison of waveforms before and after design changes.

Warp Enterprise™

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the *Warp* for PC, *Warp* for UNIX, *Warp* Professional and *Warp* Enterprise data sheets on Cypress's web site (www.cypress.com).

Third-Party Software

Although *Warp* is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the Ultra37000 family of devices. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third-party vendors.

Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the 37000 UltraISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The 37000 UltraISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on the Cypress ISR Interface, see the ISR Programming Kit data sheet (CY3700i).

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). This is accomplished through a file created by the ISR software. Check the Cypress website for the latest ISR software download information.

The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the system. The Ultra37000 ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of Ultra37000 devices to complete the desired reconfiguring or diagnostic operations. Contact your local sales office for information on availability of this option.

The fourth method for programming Ultra37000 devices is to use the same programmer that is currently being used to program FLASH370i devices.

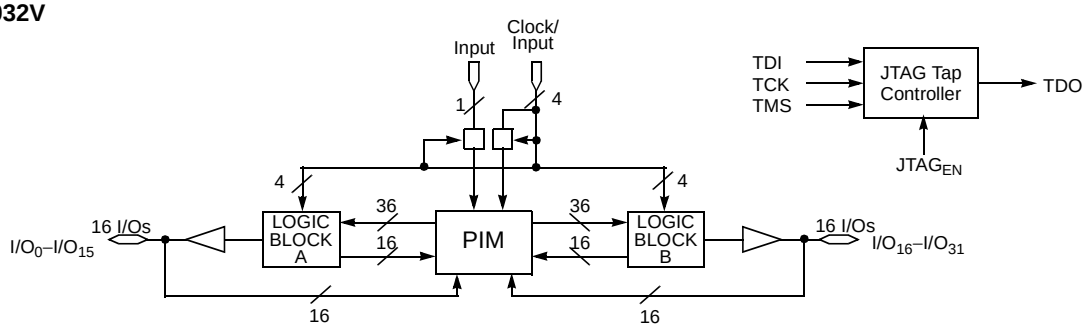
For all pinout, electrical, and timing requirements, refer to device data sheets. For ISR cable and software specifications, refer to the UltraISR kit data sheet (CY3700i).

Third-Party Programmers

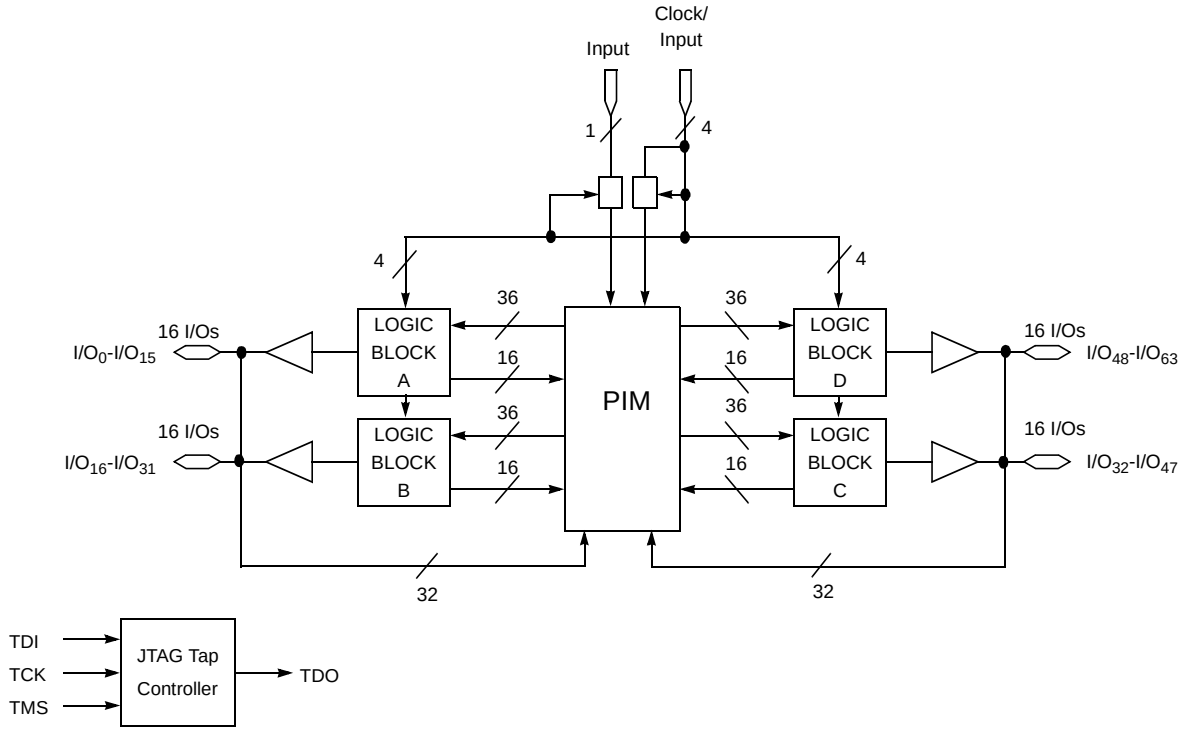
As with development software, Cypress support is available on a wide variety of third-party programmers. All major third-party programmers (including BP Micro, Data I/O, and SMS) support the Ultra37000 family.

Logic Block Diagrams

CY37032 / CY37032V

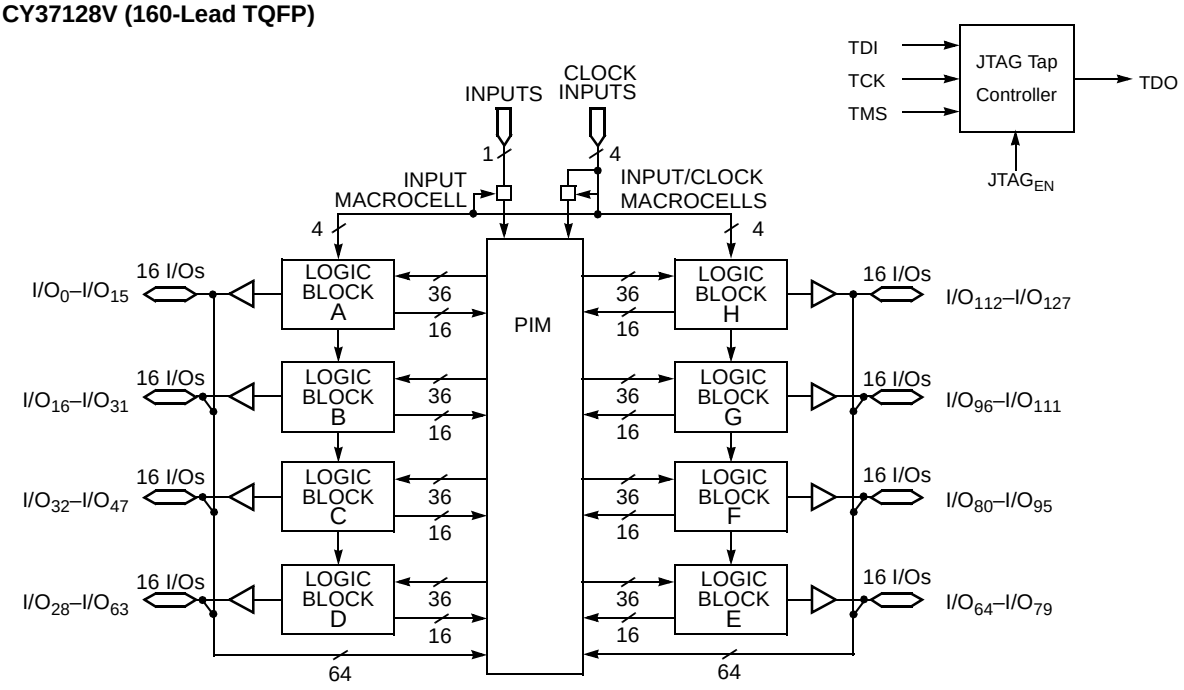


CY37064 / CY37064V (100-Lead TQFP)

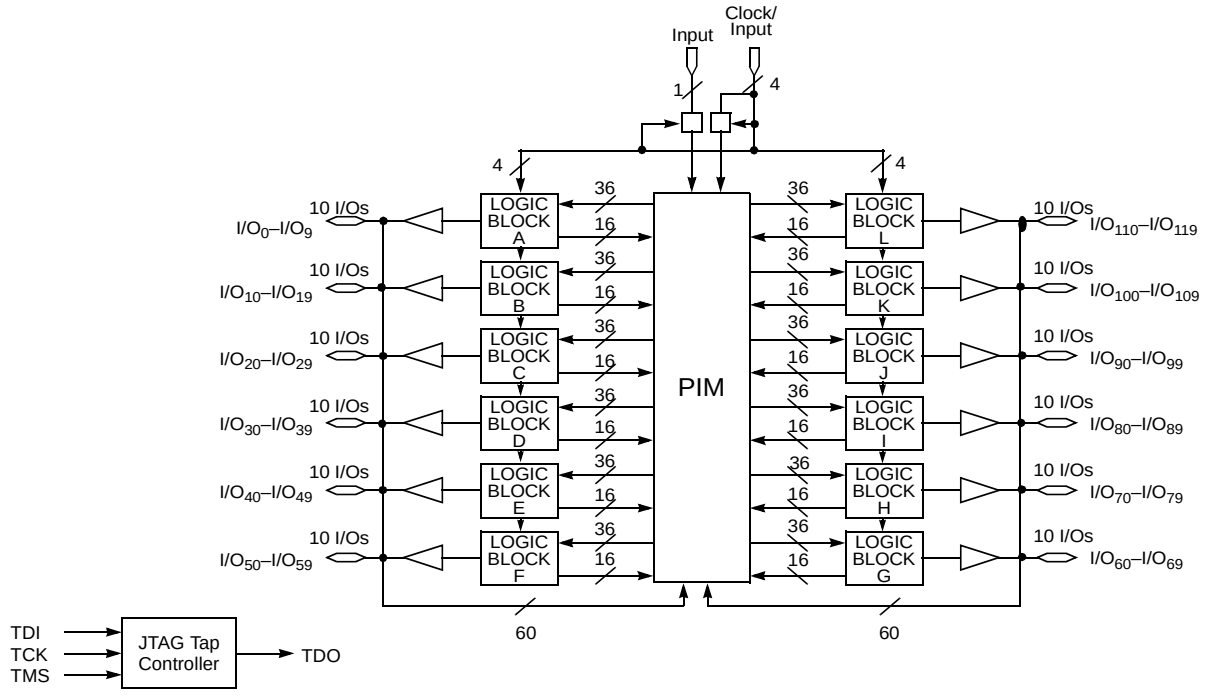


Logic Block Diagrams (continued)

CY37128 / CY37128V (160-Lead TQFP)

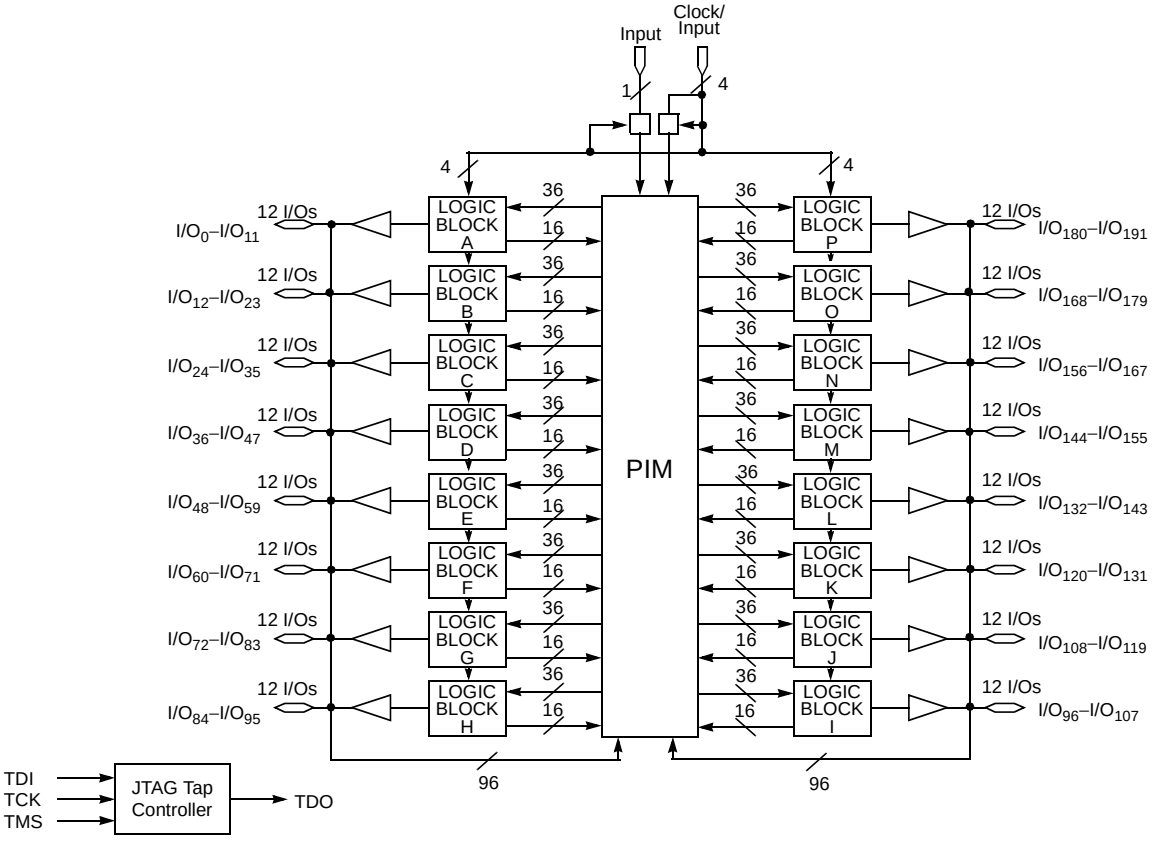


CY37192 / CY37192V (160-Lead TQFP)



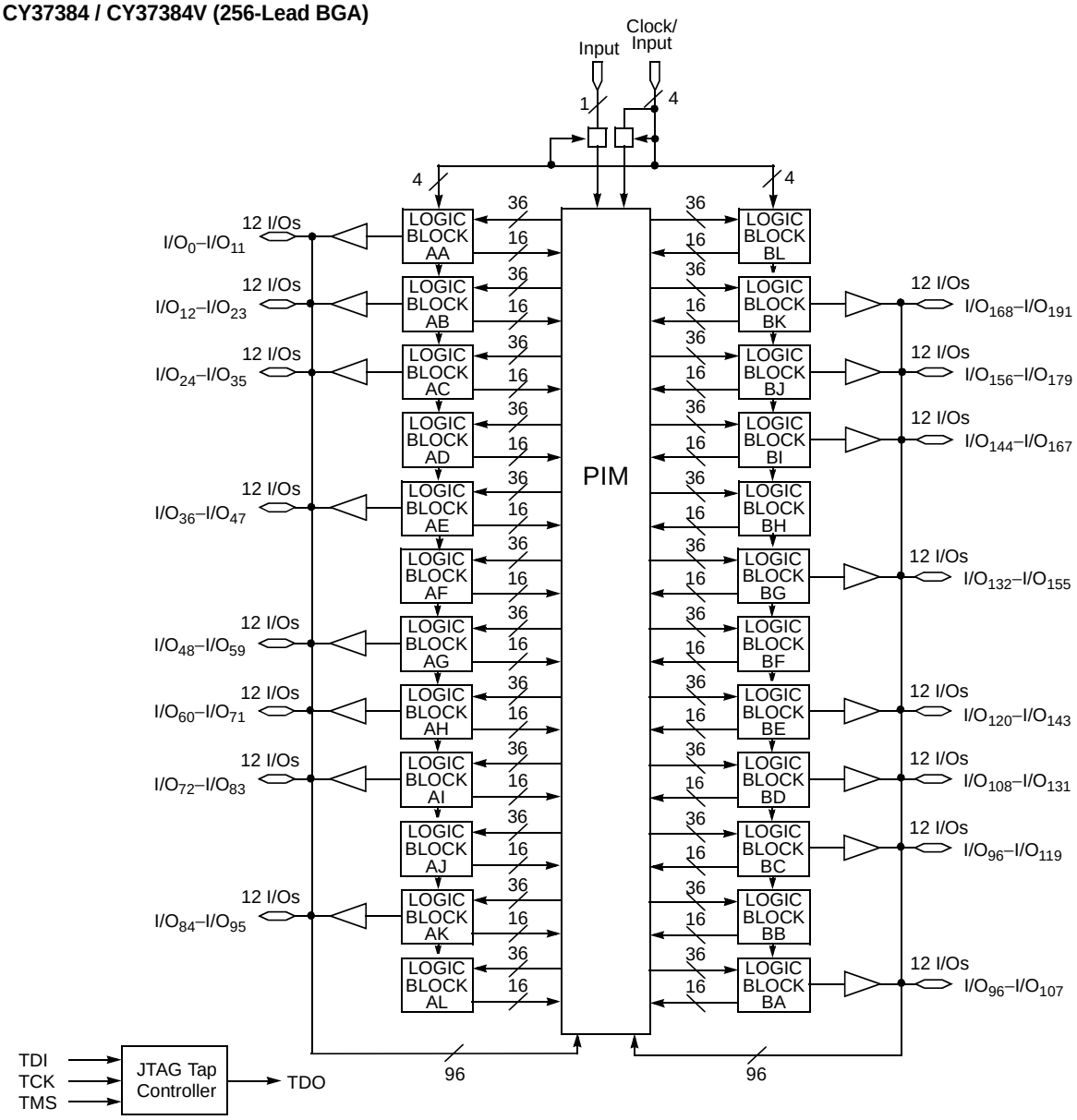
Logic Block Diagrams (continued)

CY37256 / CY37256V (256-Lead BGA)



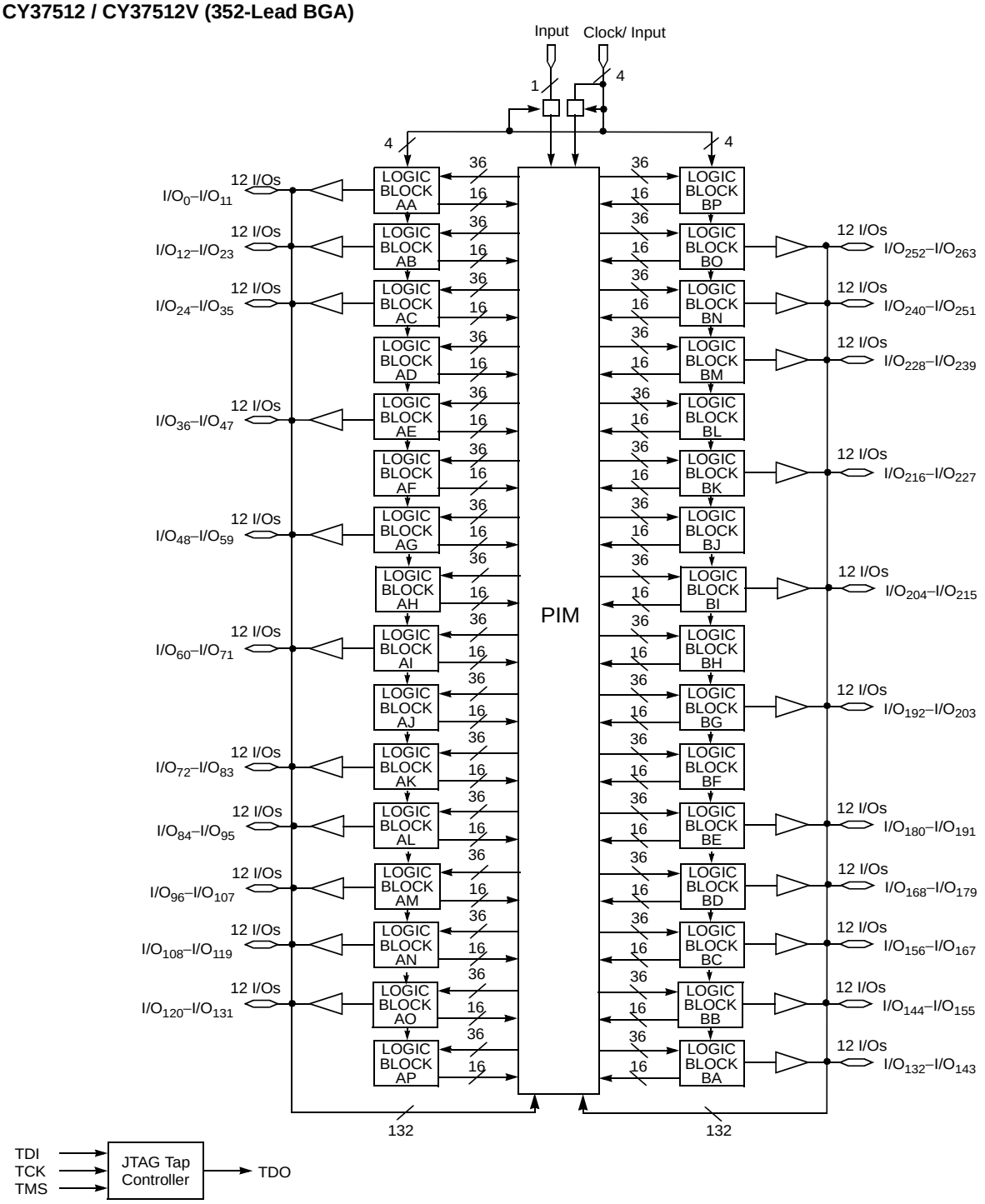
Logic Block Diagrams (continued)

CY37384 / CY37384V (256-Lead BGA)



Logic Block Diagrams (continued)

CY37512 / CY37512V (352-Lead BGA)



5.0V Device Characteristics

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage ..... 4.5 to 5.5V

Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	Output Condition	V_{CC}	V_{CCO}
Commercial	0°C to +70°C	0°C to +90°C	5V	5V ± 0.25V	5V ± 0.25V
			3.3V	5V ± 0.25V	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	5V	5V ± 0.5V	5V ± 0.5V
			3.3V	5V ± 0.5V	3.3V ± 0.3V

Notes:

2. Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 Family devices, please refer to the Application Note titled “An Introduction to In System Reprogramming with the Ultra37000.”
3. T_A is the “Instant On” case temperature.

5.0V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3.2 mA (Com'l/Ind)[4]	2.4			V
			I_{OH} = –2.0 mA (Mil)[4]	2.4			V
V_{OHZ}	Output HIGH Voltage with Output Disabled[5]	V_{CC} = Max.	I_{OH} = 0 µA (Com'l)[6]			4.2	V
			I_{OH} = 0 µA (Ind/Mil)[6]			4.5	V
			I_{OH} = –100 µA (Com'l)[6]			3.6	V
			I_{OH} = –150 µA (Ind/Mil)[6]			3.6	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)[4]			0.5	V
			I_{OL} = 12 mA (Mil)[4]			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0		V_{CCmax}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5		0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10		10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50		50	µA
I_{OS}	Output Short Circuit Current[8, 5]	V_{CC} = Max., V_{OUT} = 0.5V		–30		–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75			µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75			µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.				+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.				–500	µA

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	10	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual Function Pins[9]	V_{IN} = 5.0V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

Notes:

4. I_{OH} = –2 mA, I_{OL} = 2 mA for TDO.
5. Tested initially and after any design or process changes that may affect these parameters.
6. When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to above 3.6V if no leakage current is allowed. Note that all I/Os are output disabled during ISR programming. Refer to the application note "Understanding Bus-Hold" for additional information.
7. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
8. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
9. Dual pins are I/O with JTAG pins.

3.3V Device Characteristics

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Program Voltage ..... 3.0 to 3.6V

Current into Outputs ..... 8 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Junction Temperature	V_{CC}
Commercial	0°C to +70°C	0°C to +90°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	–40°C to +105°C	3.3V ± 0.3V
Military[3]	–55°C to +125°C	–55°C to +130°C	3.3V ± 0.3V

3.3V Device Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –4 mA (Com'l)[4]	2.4		V
			I_{OH} = –3 mA (Mil)[4]			
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8 mA (Com'l)[4]		0.5	V
			I_{OL} = 6 mA (Mil)[4]			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[7]		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs[7]		–0.5	0.8	V
I_{IX}	Input Load Current	V_I = GND OR V_{CC}, Bus-Hold Disabled		–10	10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}, Output Disabled, Bus-Hold Disabled		–50	50	µA
I_{OS}	Output Short Circuit Current[8, 5]	V_{CC} = Max., V_{OUT} = 0.5V		–30	–160	mA
I_{BHL}	Input Bus-Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75		µA
I_{BHH}	Input Bus-Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75		µA
I_{BHLO}	Input Bus-Hold LOW Overdrive Current	V_{CC} = Max.			+500	µA
I_{BHHO}	Input Bus-Hold HIGH Overdrive Current	V_{CC} = Max.			–500	µA

Inductance[5]

Parameter	Description	Test Conditions	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	208-Lead PQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 3.3V at f = 1 MHz	2	5	2	8	5	8	9	11	nH

Capacitance[5]

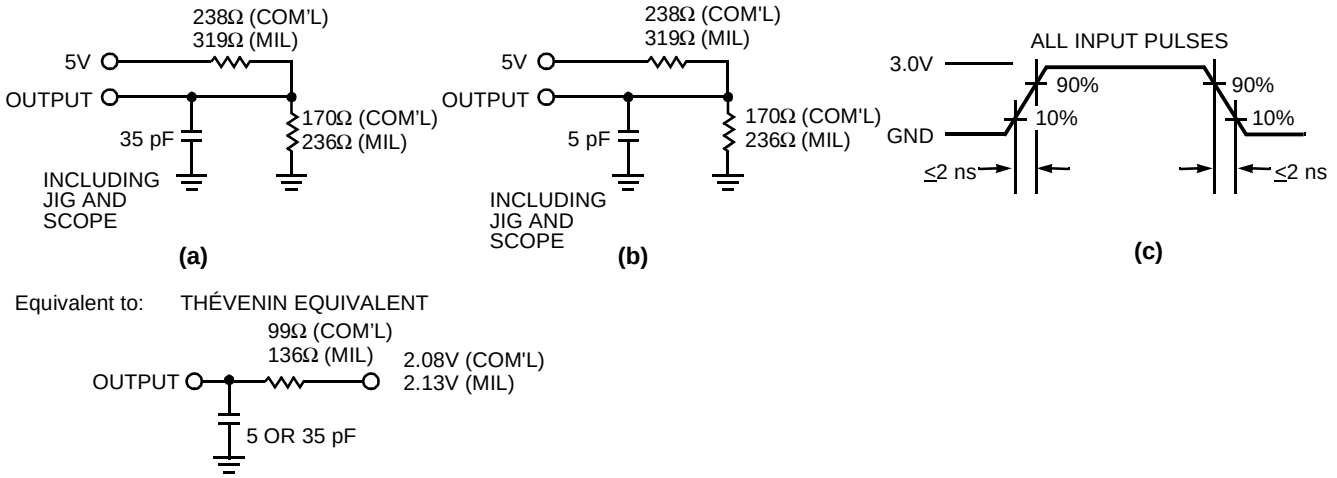
Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	12	pF
C_{DP}	Dual Functional Pins[9]	V_{IN} = 3.3V at f = 1 MHz at T_A = 25°C	16	pF

Endurance Characteristics[5]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

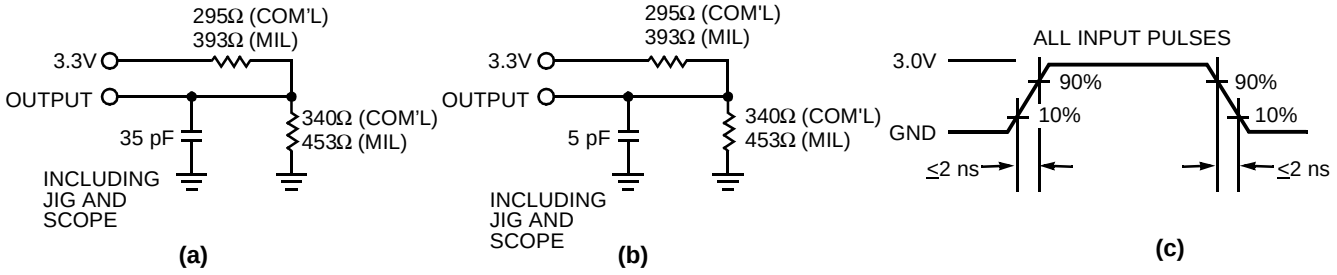
AC Characteristics.

5.0V AC Test Loads and Waveforms

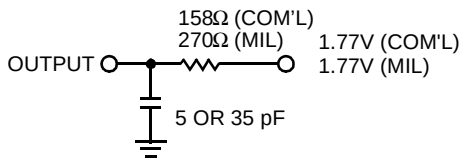


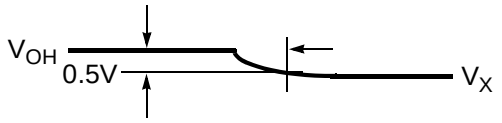
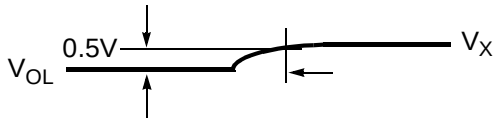
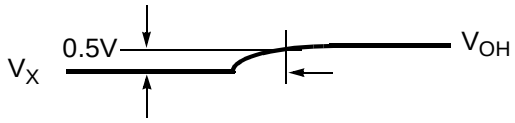
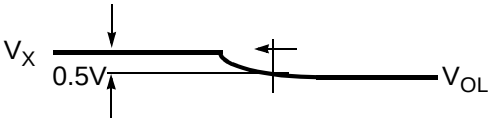
Equivalent to: THÉVENIN EQUIVALENT

3.3V AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameter[10]	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{the}	

(d) Test Waveforms

Note:
10. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.

Switching Characteristics Over the Operating Range[11]

Parameter	Description	Unit
Combinatorial Mode Parameters		
t_{PD}[12, 13, 14]	Input to Combinatorial Output	ns
t_{PDL}[12, 13, 14]	Input to Output Through Transparent Input or Output Latch	ns
t_{PDLL}[12, 13, 14]	Input to Output Through Transparent Input and Output Latches	ns
t_{EA}[12, 13, 14]	Input to Output Enable	ns
t_{ER}[10, 12]	Input to Output Disable	ns
Input Register Parameters		
t_{WL}	Clock or Latch Enable Input LOW Time[8]	ns
t_{WH}	Clock or Latch Enable Input HIGH Time[8]	ns
t_{IS}	Input Register or Latch Set-Up Time	ns
t_{IH}	Input Register or Latch Hold Time	ns
t_{ICO}[12, 13, 14]	Input Register Clock or Latch Enable to Combinatorial Output	ns
t_{ICOL}[12, 13, 14]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch	ns
Synchronous Clocking Parameters		
t_{CO}[13, 14]	Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output	ns
t_{S}[12]	Set-Up Time from Input to Sync. Clk (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_{H}	Register or Latch Data Hold Time	ns
t_{CO2}[12, 13, 14]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Combinatorial Output Delay (Through Logic Array)	ns
t_{SCS}[12]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable (Through Logic Array)	ns
t_{SL}[12]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK_0 CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	ns
Product Term Clocking Parameters		
t_{COPT}[12, 13, 14]	Product Term Clock or Latch Enable (PTCLK) to Output	ns
t_{SPT}	Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK)	ns
t_{HPT}	Register or Latch Data Hold Time	ns
t_{ISPT}[12]	Set-Up Time for Buried Register used as an Input Register from Input to Product Term Clock or Latch Enable (PTCLK)	ns
t_{IHPT}	Buried Register Used as an Input Register or Latch Data Hold Time	ns
t_{CO2PT}[12, 13, 14]	Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array)	ns
Pipelined Mode Parameters		
t_{ICS}[12]	Input Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) to Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3)	ns

Notes:
11. All AC parameters are measured with two outputs switching and 35-pF AC Test Load.
12. Logic Blocks operating in Low-Power Mode, add t_{LP} to this spec.
13. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.
14. When V_{CCO}= 3.3V, add $t_{3.3IO}$ to this spec.

Switching Characteristics Over the Operating Range[11] (continued)

Parameter	Description	Unit
Operating Frequency Parameters		
f_{MAX1}	Maximum Frequency with Internal Feedback (Lesser of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)[5]	MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$[5]	MHz
f_{MAX4}	Maximum Frequency in Pipelined Mode (Lesser of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)[5]	MHz
Reset/Preset Parameters		
t_{RW}	Asynchronous Reset Width[5]	ns
t_{RR}[12]	Asynchronous Reset Recovery Time[5]	ns
t_{RO}[12, 13, 14]	Asynchronous Reset to Output	ns
t_{PW}	Asynchronous Preset Width[5]	ns
t_{PR}[12]	Asynchronous Preset Recovery Time[5]	ns
t_{PO}[12, 13, 14]	Asynchronous Preset to Output	ns
User Option Parameters		
t_{LP}	Low Power Adder	ns
t_{SLEW}	Slow Output Slew Rate Adder	ns
$t_{3.3IO}$	3.3V I/O Mode Timing Adder[5]	ns
JTAG Timing Parameters		
$t_{S\ JTAG}$	Set-Up Time from TDI and TMS to TCK[5]	ns
$t_{H\ JTAG}$	Hold Time on TDI and TMS[5]	ns
$t_{CO\ JTAG}$	Falling Edge of TCK to TDO[5]	ns
f_{JTAG}	Maximum JTAG Tap Controller Frequency[5]	ns

Switching Characteristics Over the Operating Range[11]

Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters																	
t_{PD}[12, 13, 14]		6		6.5		7.5		8.5		10		12		15		20	ns
t_{PDL}[12, 13, 14]		11		12.5		14.5		16		16.5		17		19		22	ns
t_{PDLL}[12, 13, 14]		12		13.5		15.5		17		17.5		18		20		24	ns
t_{EA}[12, 13, 14]		8		8.5		11		13		14		16		19		24	ns
t_{ER}[10, 12]		8		8.5		11		13		14		16		19		24	ns
Input Register Parameters																	
t_{WL}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t_{WH}	2.5		2.5		2.5		2.5		3		3		4		5		ns
t_{IS}	2		2		2		2		2		2.5		3		4		ns
t_{IH}	2		2		2		2		2		2.5		3		4		ns
t_{ICO}[12, 13, 14]		11		11		11		12.5		12.5		16		19		24	ns
t_{ICOL}[12, 13, 14]		12		12		12		14		16		18		21		26	ns
Synchronous Clocking Parameters																	
t_{CO}[13, 14]		4		4		4.5		6		6.5[15]		6.5[16]		8[17]		10	ns
t_{S}[12]	4		4		5		5		5.5[15]		6[16]		8[17]		10		ns
t_{H}	0		0		0		0		0		0		0		0		ns
t_{CO2}[12, 13, 14]		9.5		10		11		12		14		16		19		24	ns
t_{SCS}[12]	5		6		6.5		7		8[15]		10		12		15		ns
t_{SL}[12]	7.5		7.5		8.5		9		10		12		15		15		ns
t_{HL}	0		0		0		0		0		0		0		0		ns
Product Term Clocking Parameters																	
t_{COPT}[12, 13, 14]		7		10		10		13		13		13		15		20	ns
t_{SPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t_{HPT}	2.5		2.5		2.5		3		5		5.5		6		7		ns
t_{ISPT}[12]	0		0		0		0		0		0		0		0		ns
t_{IHPT}	6		6.5		6.5		7.5		9		11		14		19		ns
t_{CO2PT}[12, 13, 14]		12		14		15		19		19		21		24		30	ns
Pipelined Mode Parameters																	
t_{ICS}[12]	5		6		6		7		8[15]		10		12		15		ns
Operating Frequency Parameters																	
f_{MAX1}	200		167		154		143		125[15]		100		83		66		MHz
f_{MAX2}	200		200		200		167		154		153[16]		125[17]		100		MHz
f_{MAX3}	125		125		105		91		83		80[16]		62.5		50		MHz
f_{MAX4}	167		167		154		125		118		100		83		66		MHz

Notes:

15. The following values correspond to the CY37512 and CY37384 devices: t_{CO} = 5 ns, t_S = 6.5 ns, t_{SCS} = 8.5 ns, t_{ICS} = 8.5 ns, f_{MAX1} = 118 MHz.
16. The following values correspond to the CY37192V and CY37256V devices: t_{CO} = 6 ns, t_S = 7 ns, f_{MAX2} = 143 MHz, f_{MAX3} = 77 MHz, and f_{MAX4} = 100 MHz; and for the CY37512 devices: t_S = 7 ns.
17. The following values correspond to the CY37512V and CY37384V devices: t_{CO} = 6.5 ns, t_S = 9.5 ns, and f_{MAX2} = 105 MHz.

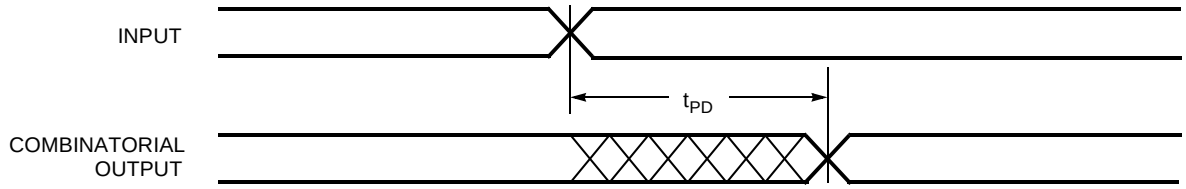
Switching Characteristics Over the Operating Range[11] (continued)

Parameter	200 MHz		167 MHz		154 MHz		143 MHz		125 MHz		100 MHz		83 MHz		66 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters																	
t_{RW}	8		8		8		8		10		12		15		20		ns
t_{RR}[12]	10		10		10		10		12		14		17		22		ns
t_{RO}[12, 13, 14]		12		13		13		14		15		18		21		26	ns
t_{PW}	8		8		8		8		10		12		15		20		ns
t_{PR}[12]	10		10		10		10		12		14		17		22		ns
t_{PO}[12, 13, 14]		12		13		13		14		15		18		21		26	ns
User Option Parameters																	
t_{LP}		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{SLEW}		3		3		3		3		3		3		3		3	ns
$t_{3.3IO}$[18]		0.3		0.3		0.3		0.3		0.3		0.3		0.3		0.3	ns
JTAG Timing Parameters																	
$t_{S\ JTAG}$	0		0		0		0		0		0		0		0		ns
$t_{H\ JTAG}$	20		20		20		20		20		20		20		20		ns
$t_{CO\ JTAG}$		20		20		20		20		20		20		20		20	ns
f_{JTAG}		20		20		20		20		20		20		20		20	MHz

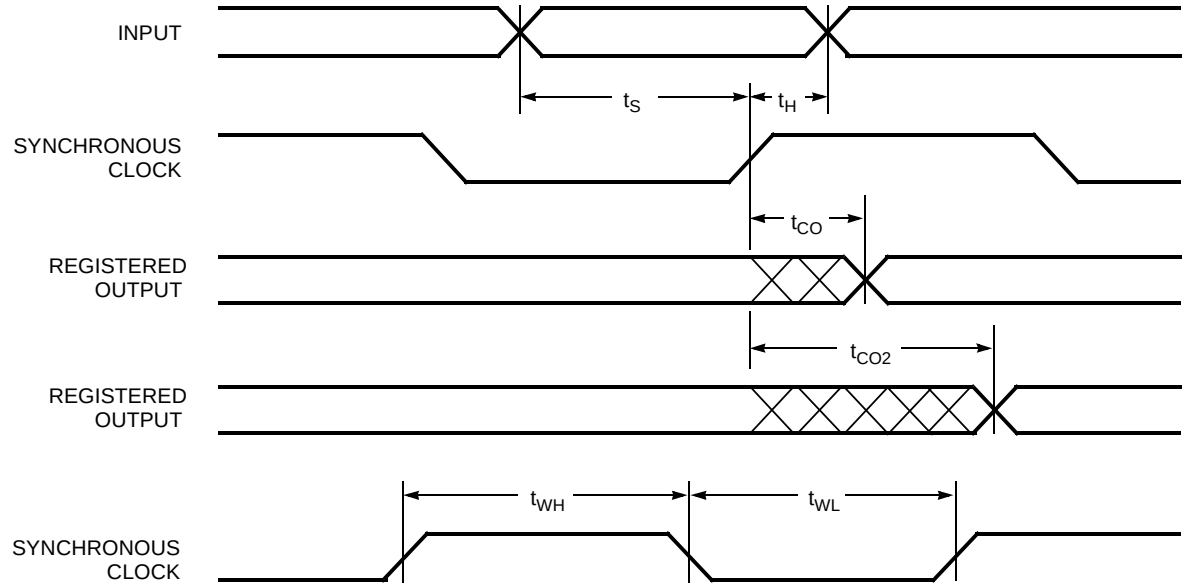
Note:
18. Only applicable to the 5V devices.

Switching Waveforms

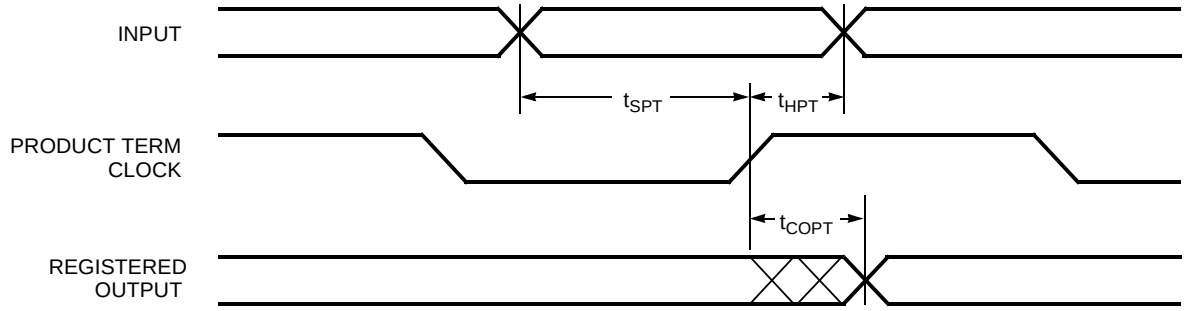
Combinatorial Output



Registered Output with Synchronous Clocking

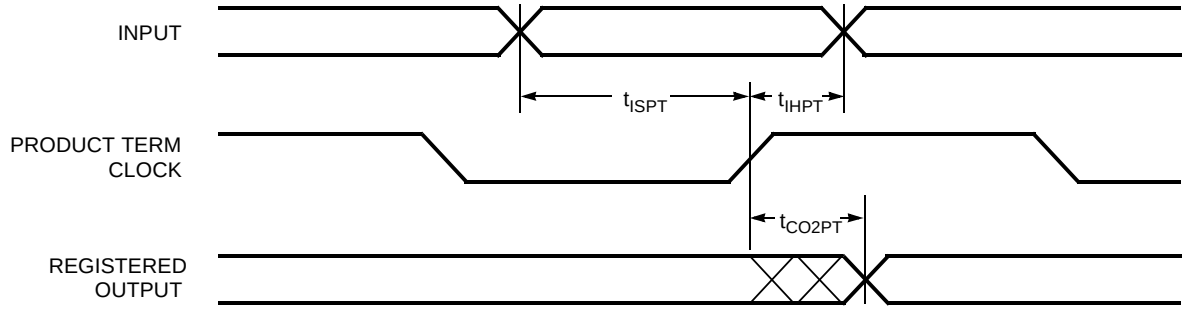


Registered Output with Product Term Clocking Input Going Through the Array

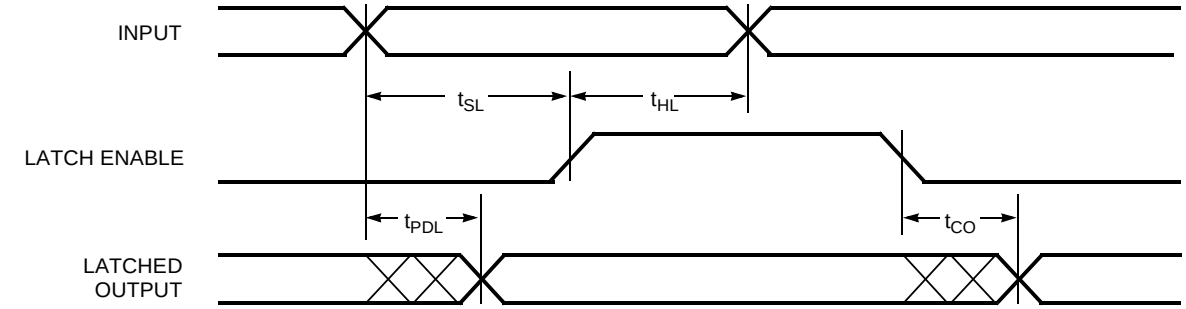


Switching Waveforms (continued)

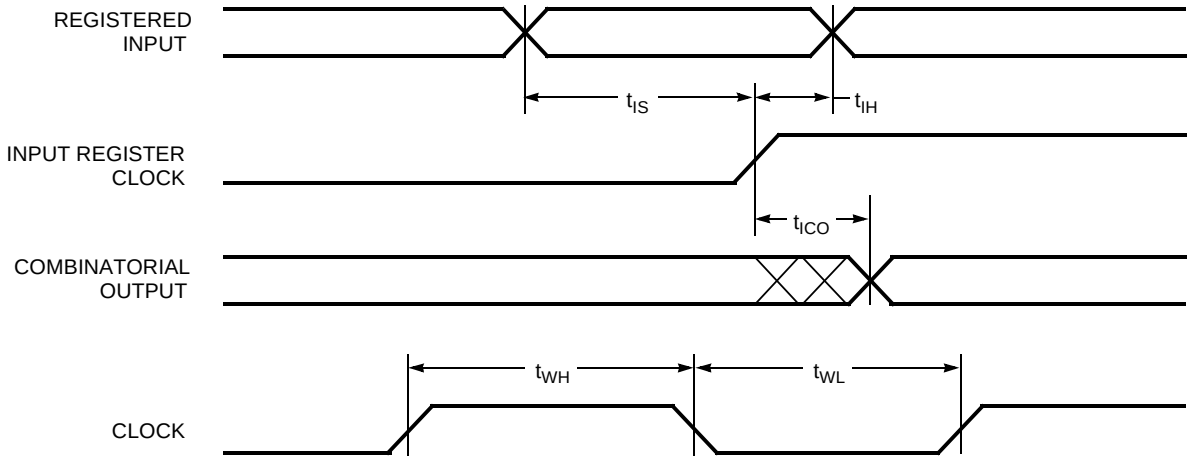
Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register



Latched Output

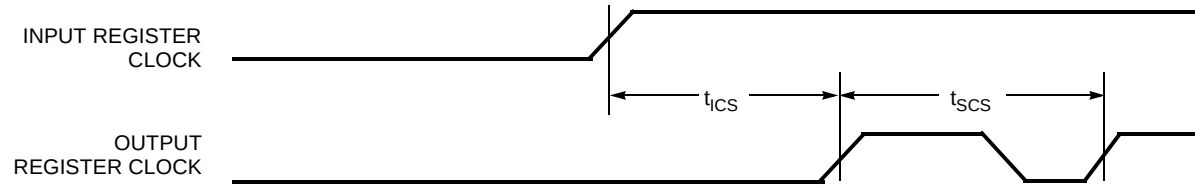


Registered Input

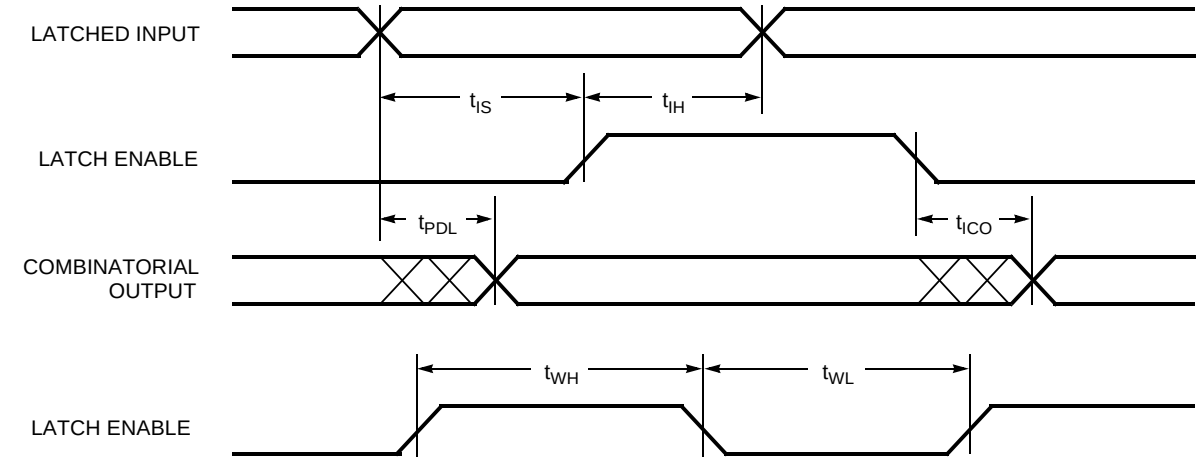


Switching Waveforms (continued)

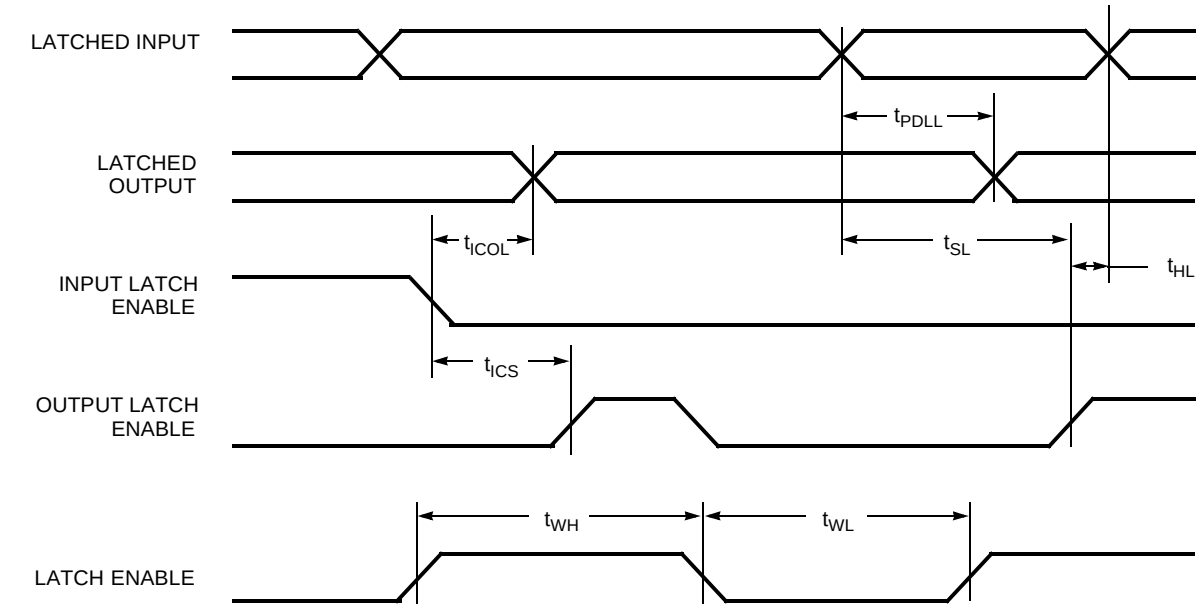
Clock to Clock



Latched Input

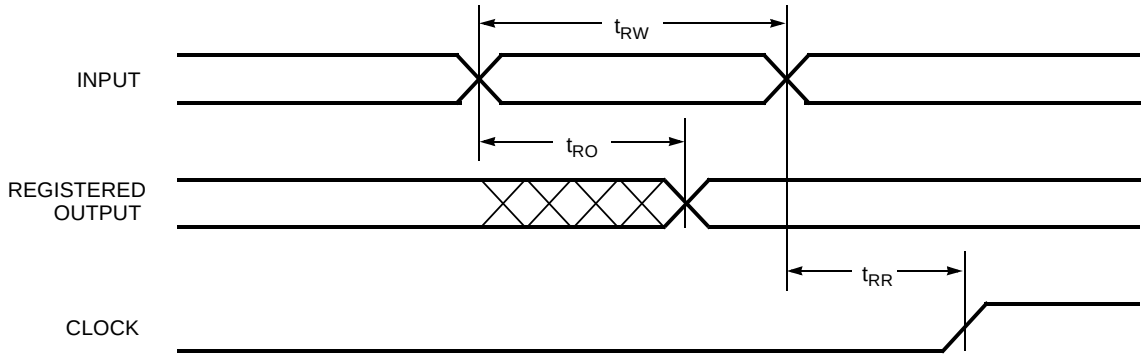


Latched Input and Output

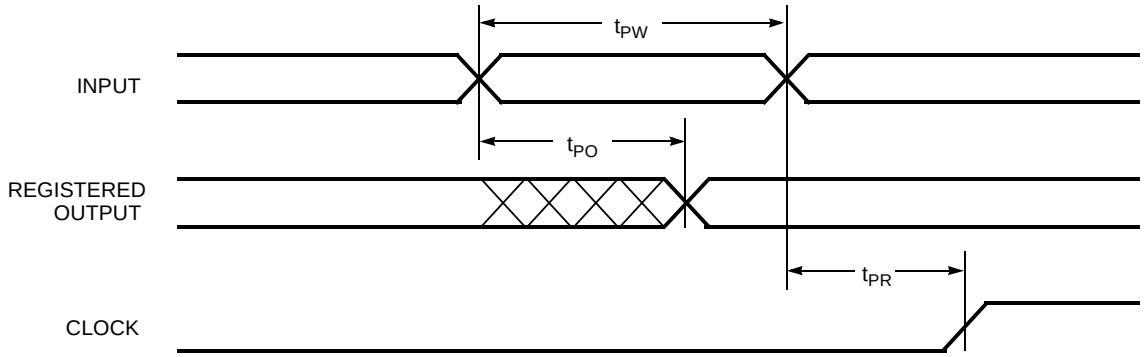


Switching Waveforms (continued)

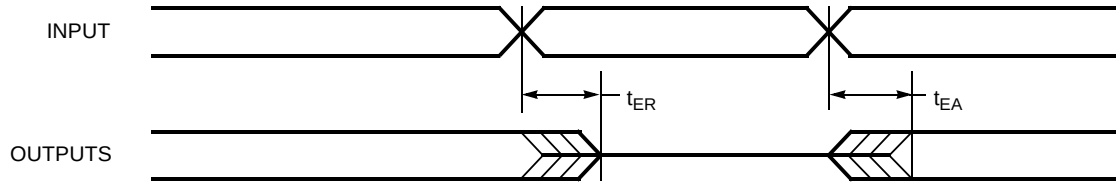
Asynchronous Reset



Asynchronous Preset



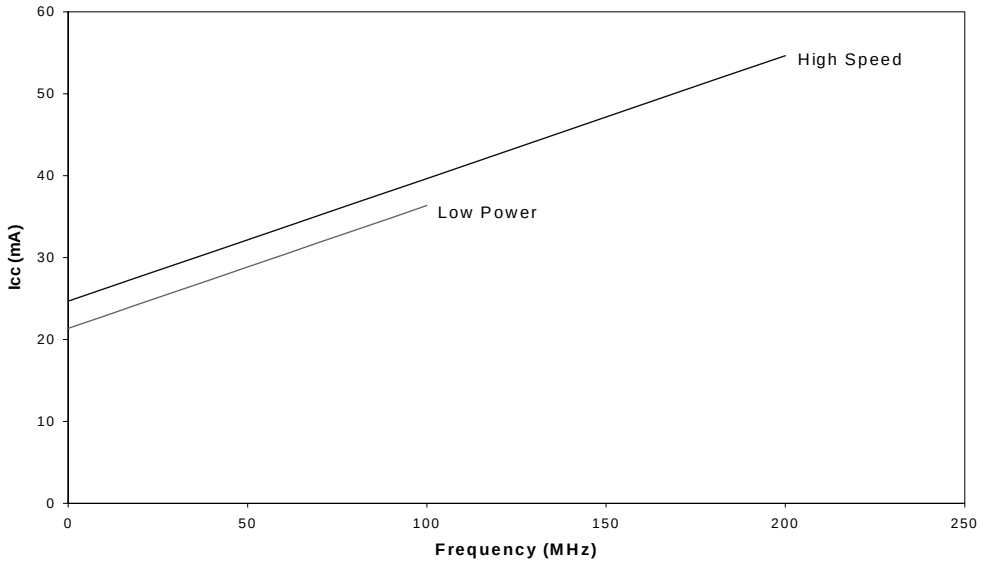
Output Enable/Disable



Power Consumption

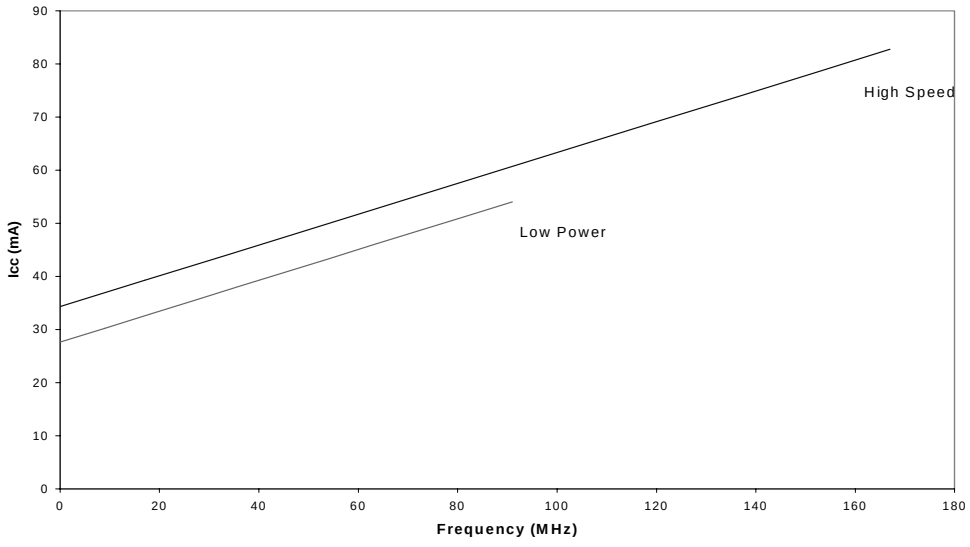
Typical 5.0V Power Consumption

CY37032



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

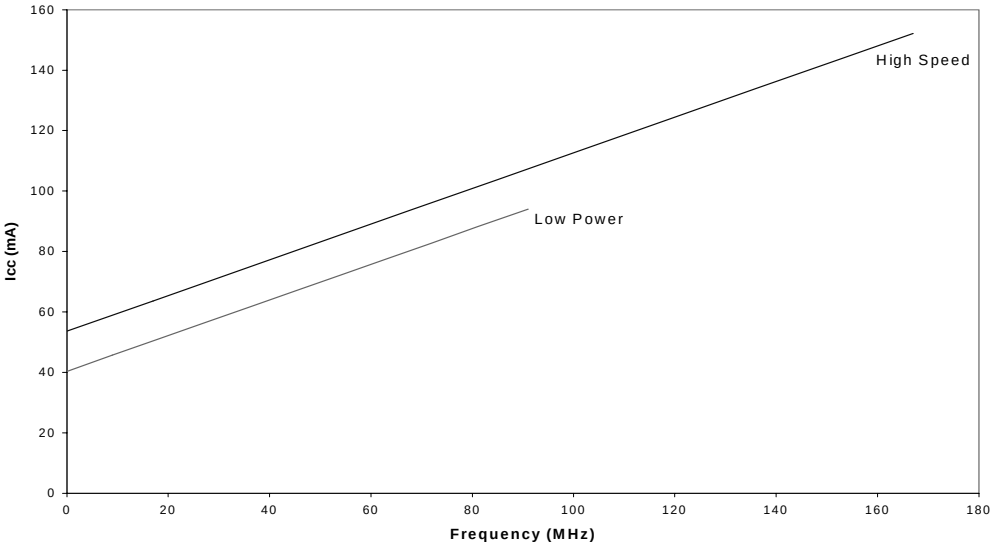
CY37064



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

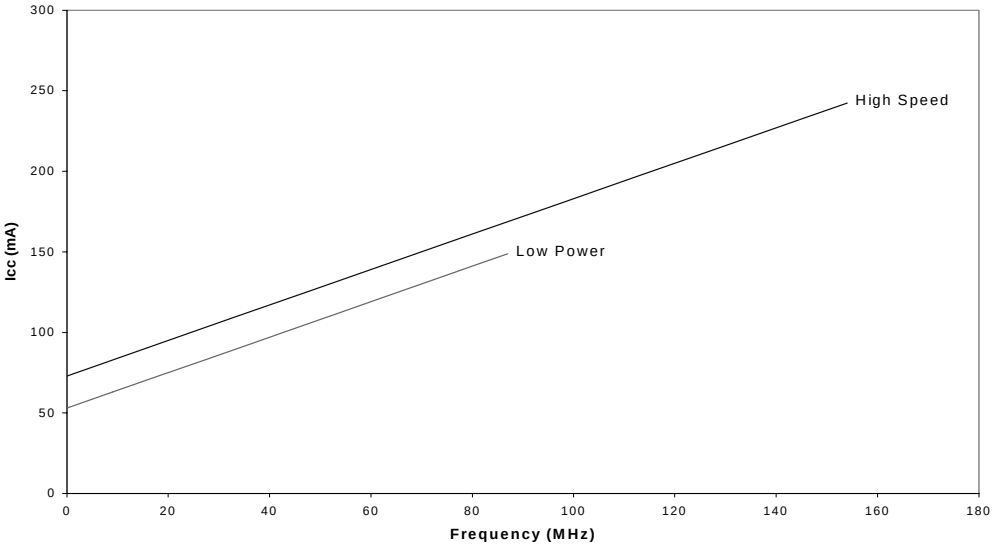
Typical 5.0V Power Consumption (continued)

CY37128



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

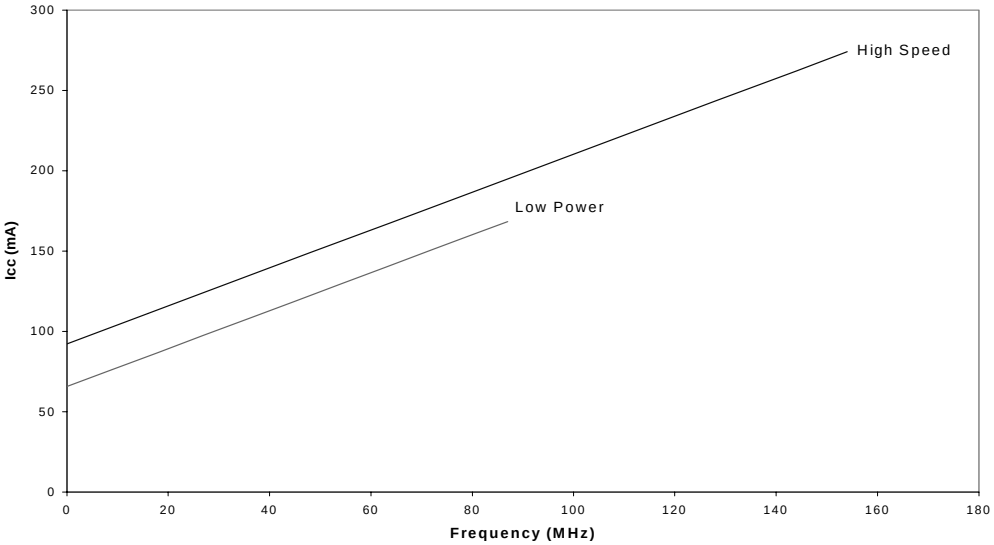
CY37192



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

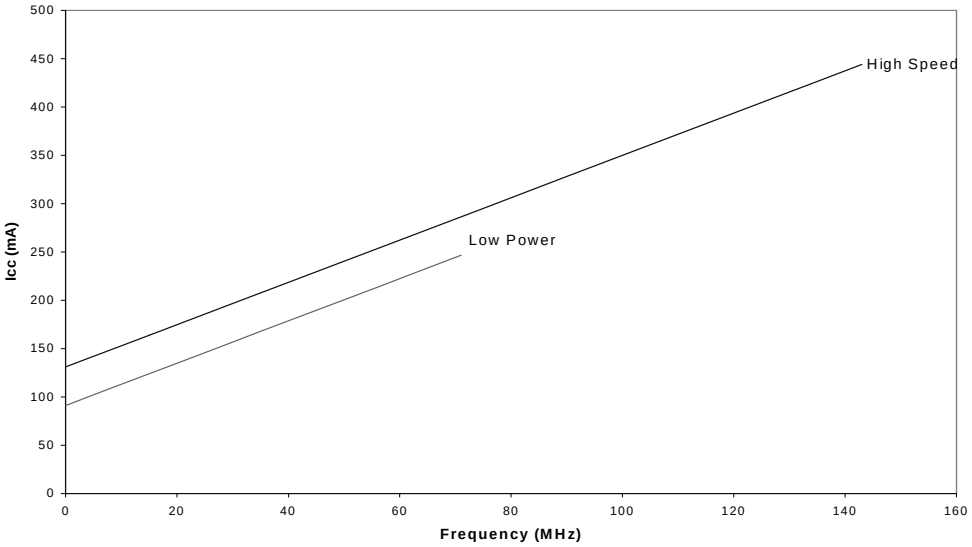
Typical 5.0V Power Consumption (continued)

CY37256



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

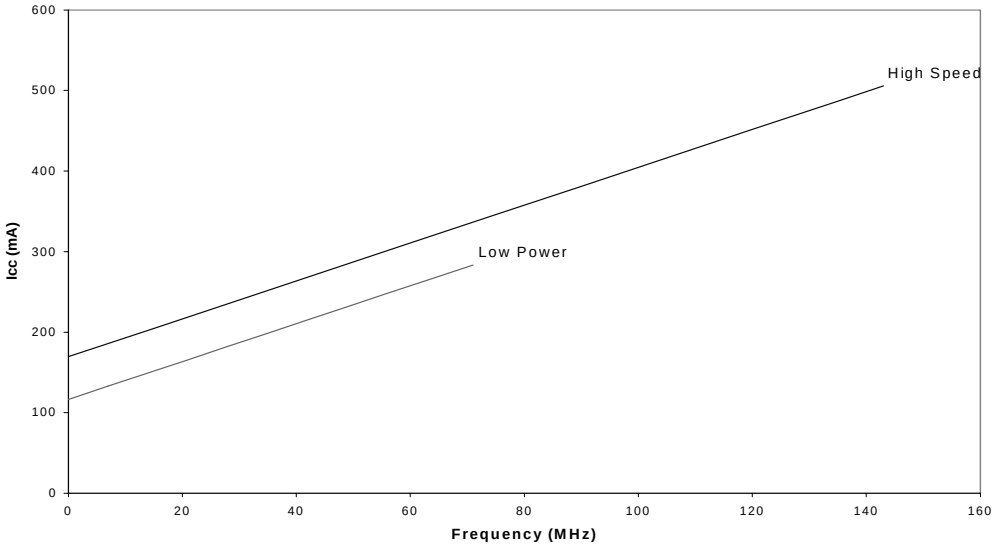
CY37384



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Typical 5.0V Power Consumption (continued)

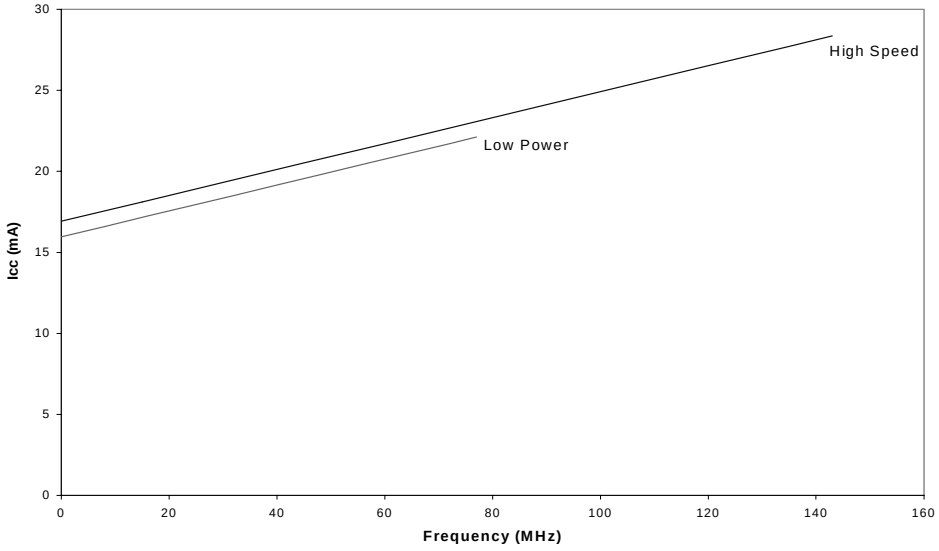
CY37512



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 5.0V, T_A = Room Temperature

Typical 3.3V Power Consumption

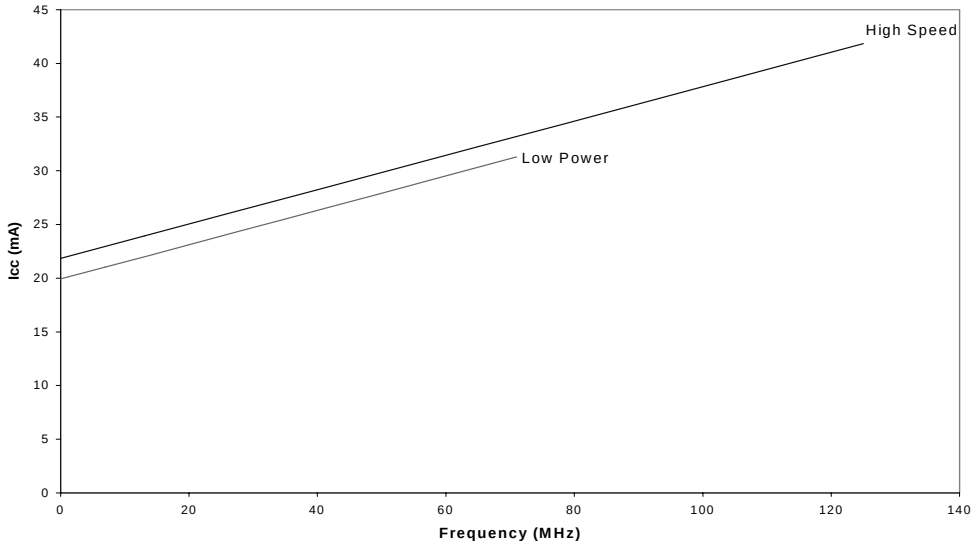
CY37032V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

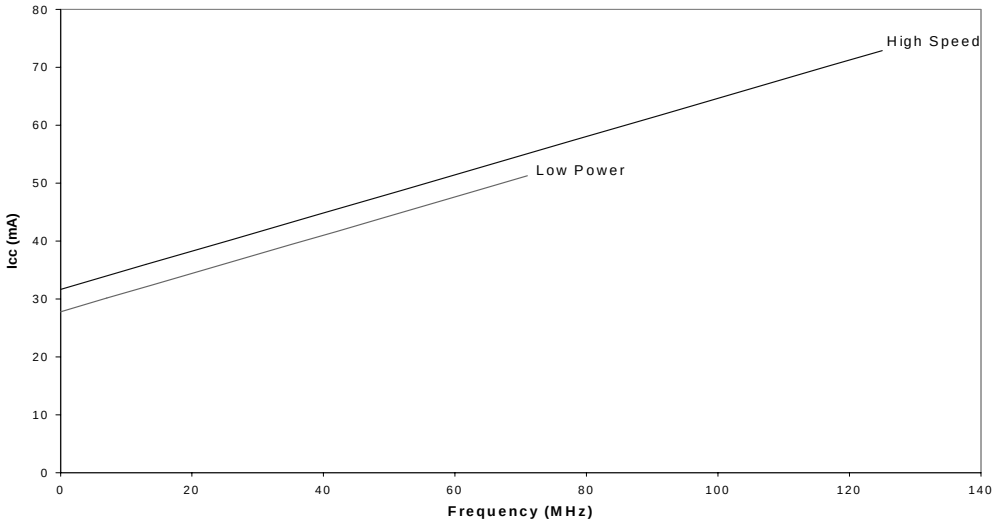
Typical 3.3V Power Consumption (continued)

CY37064V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

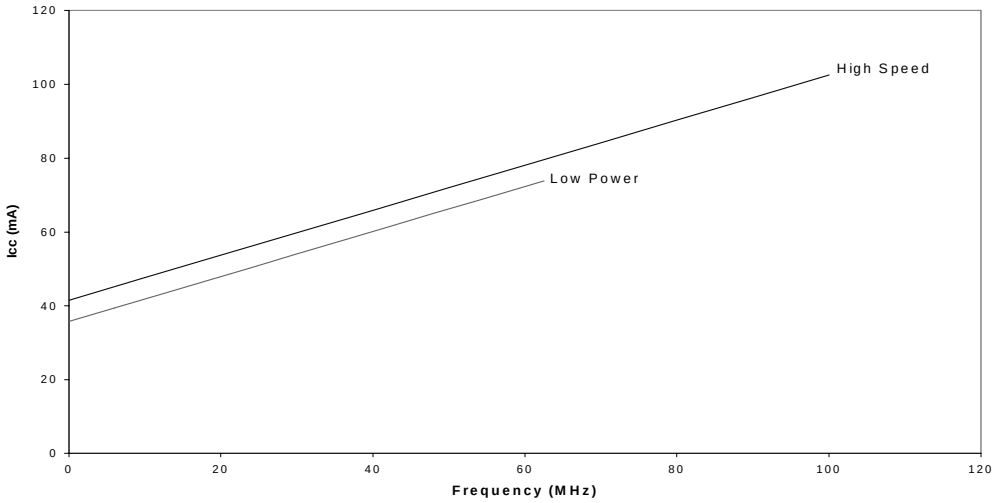
CY37128V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

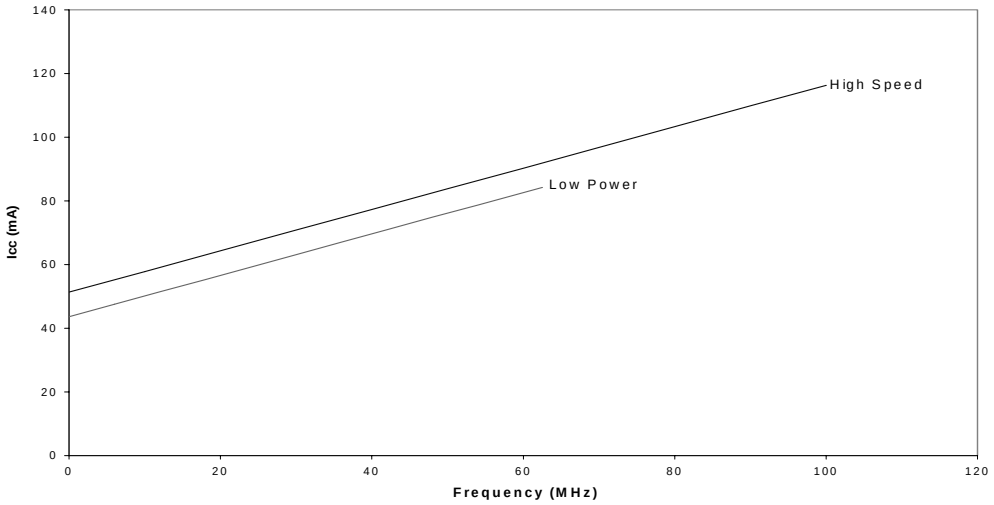
Typical 3.3V Power Consumption (continued)

CY37192V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

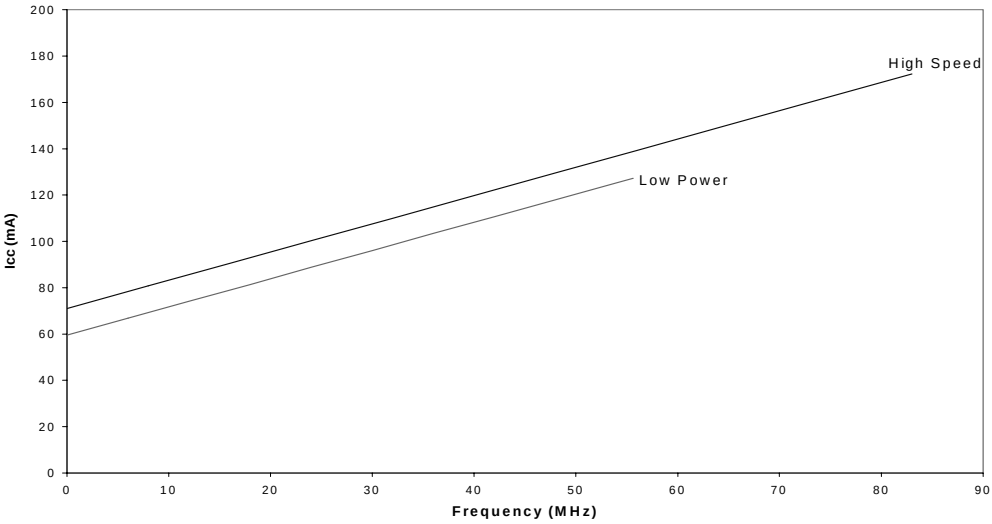
CY37256V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

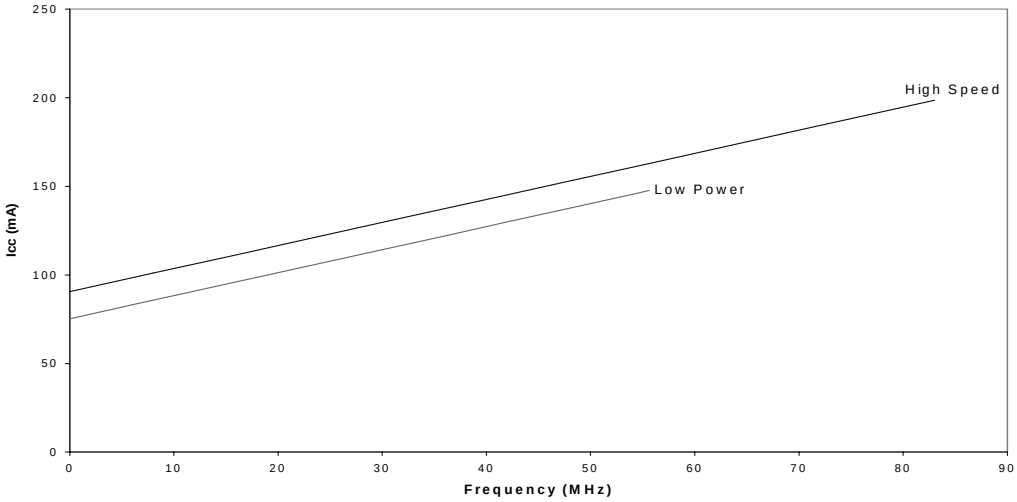
Typical 3.3V Power Consumption (continued)

CY37384V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

CY37512V

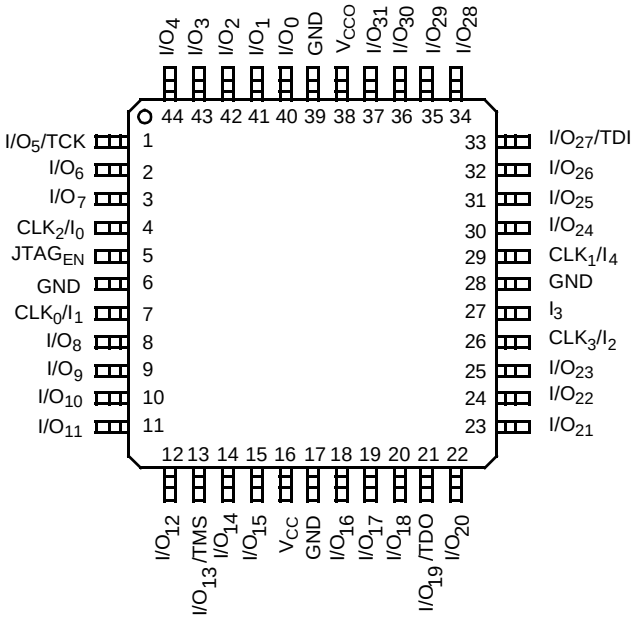


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.
V_{CC} = 3.3V, T_A = Room Temperature

Pin Configurations[19]

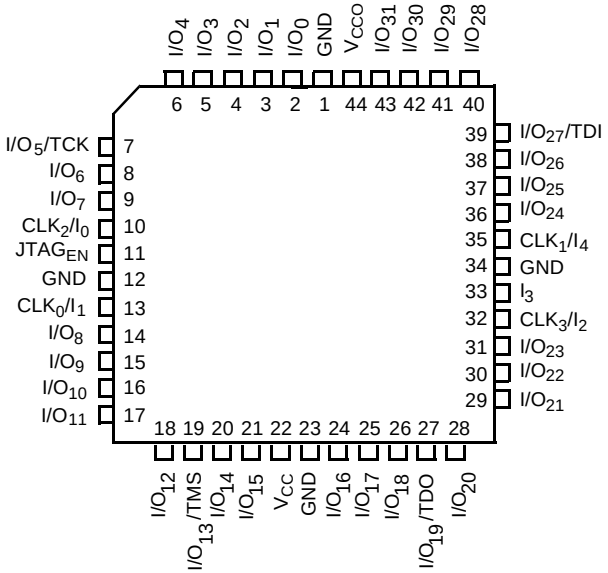
44-Pin TQFP (A44)

Top View



44-Pin PLCC (J67) / CLCC (Y67)

Top View



Note:
19. For 3.3V versions (Ultra37000V), $V_{CCO} = V_{CC}$.

Pin Configurations[19] (continued)

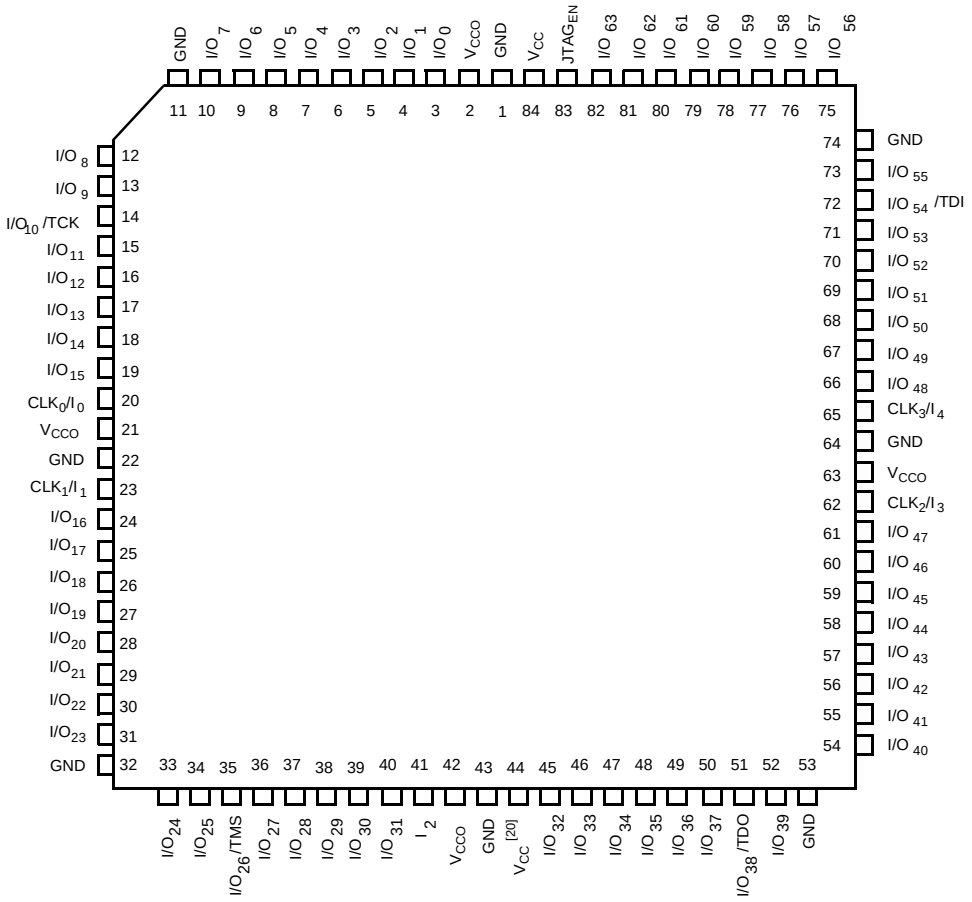
48-Ball Fine-Pitch BGA (BA50)
Top View

	1	2	3	4	5	6	7	8
A	I/O_5 TCK	V_{CC}	I/O_3	I/O_1	I/O_{31}	I/O_{30}	V_{CC}	I/O_{27} TDI
B	V_{CC}	I/O_4	I/O_2	I/O_0	I/O_{29}	I/O_{28}	I/O_{26}	CLK_1/ I_4
C	CLK_2/ I_0	I/O_7	I/O_6	GND	GND	I/O_{25}	I/O_{24}	I_3
D	$JTAG_{EN}$	I/O_8	I/O_9	GND	GND	I/O_{22}	I/O_{23}	CLK_3/ I_2
E	CLK_0/ I_1	I/O_{12}	I/O_{11}	I/O_{10}	I/O_{16}	I/O_{20}	I/O_{21}	V_{CC}
F	I/O_{13} TMS	V_{CC}	I/O_{14}	I/O_{15}	I/O_{17}	I/O_{18}	V_{CC}	I/O_{19} TDO

Pin Configurations[19] (continued)

84-Lead PLCC (J83) / CLCC (Y84)

Top View

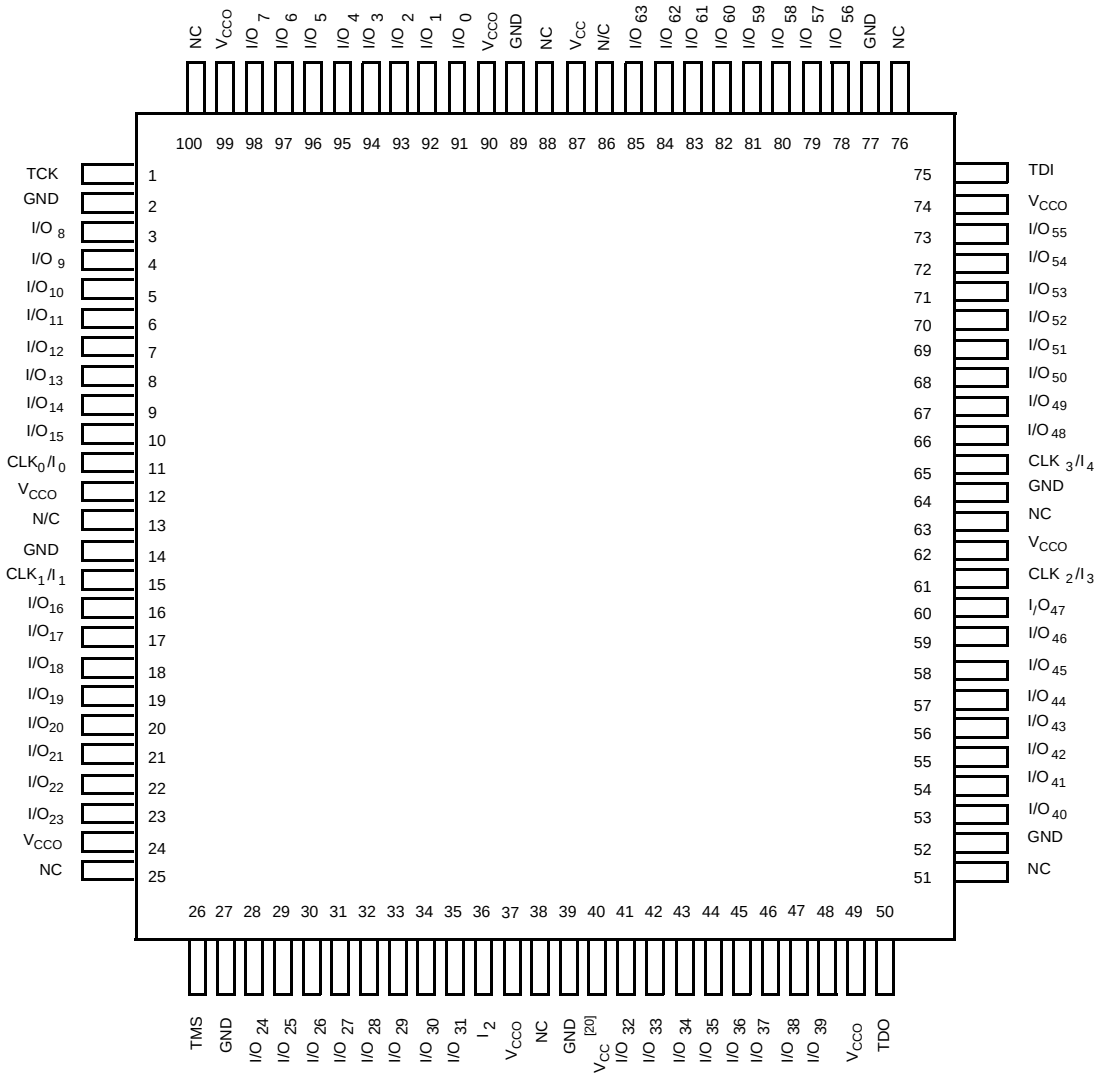


Note:

20. This pin is a N/C, but Cypress recommends that you connect it to V_{CC} to ensure future compatibility.

Pin Configurations[19] (continued)

100-Lead TQFP (A100)
Top View



Pin Configurations[19] (continued)

100-Ball Fine-Pitch BGA (BB100)
for CY37064V
Top View

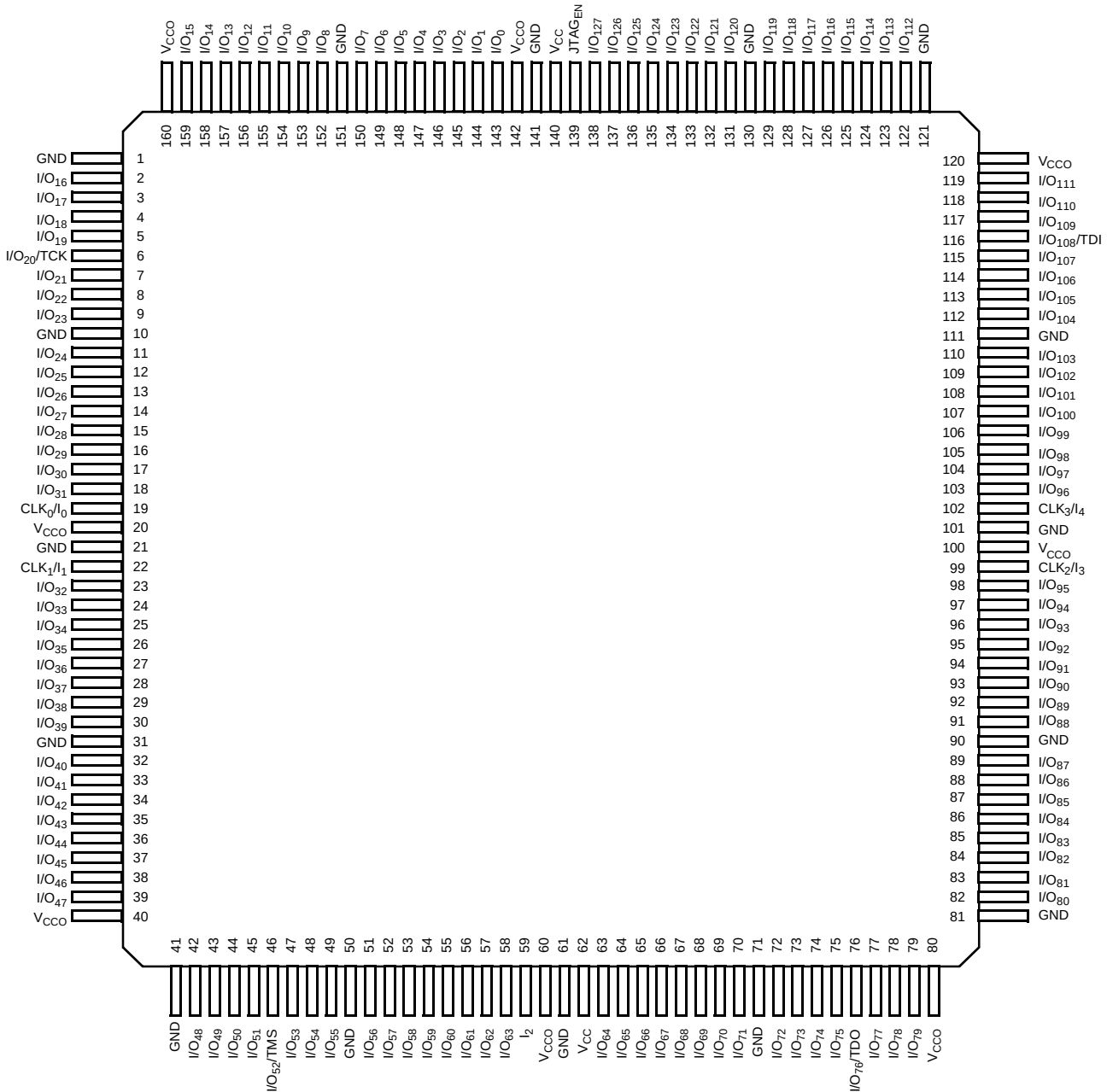
	1	2	3	4	5	6	7	8	9	10
A	NC	NC	I/O_7	I/O_5	I/O_2	I/O_{62}	I/O_{60}	I/O_{58}	I/O_{57}	I/O_{56}
B	I/O_9	I/O_8	I/O_6	I/O_4	I/O_1	I/O_{63}	V_{CC}	I/O_{59}	I/O_{55}	NC
C	I/O_{10}	TCK	V_{CC}	I/O_3	NC	NC	I/O_{61}	V_{CC}	TDI	I/O_{54}
D	I/O_{11}	NC	I/O_{12}	I/O_{13}	I/O_0	NC	I/O_{51}	I/O_{52}	CLK_3/I_4	I/O_{53}
E	I/O_{14}	CLK_0/I_0	I/O_{15}	NC	GND	GND	I/O_{48}	I/O_{49}	CLK_2/I_3	I/O_{50}
F	I/O_{17}	NC	NC	I/O_{16}	GND	GND	NC	NC	I_2	I/O_{47}
G	I/O_{22}	CLK_1/I_1	I/O_{21}	I/O_{19}	I/O_{18}	I/O_{46}	I/O_{45}	I/O_{44}	NC	I/O_{43}
H	I/O_{23}	TMS	V_{CC}	I/O_{20}	NC	I/O_{32}	I/O_{42}	V_{CC}	TDO	I/O_{41}
J	NC	I/O_{26}	I/O_{28}	NC	I/O_{31}	I/O_{33}	I/O_{35}	I/O_{37}	I/O_{39}	I/O_{40}
K	I/O_{24}	I/O_{25}	I/O_{27}	I/O_{29}	I/O_{30}	I/O_{34}	I/O_{36}	I/O_{38}	NC	NC

100-Ball Fine-Pitch BGA (BB100)
for CY37128V
Top View

	1	2	3	4	5	6	7	8	9	10
A	NC	I/O_9	I/O_8	I/O_6	I/O_3	I/O_{76}	I/O_{74}	I/O_{72}	I/O_{71}	I/O_{70}
B	I/O_{11}	I/O_{10}	I/O_7	I/O_5	I/O_2	I/O_{77}	V_{CC}	I/O_{73}	I/O_{68}	I/O_{69}
C	I/O_{12}	I/O_{13} TCK	V_{CC}	I/O_4	I/O_1	I/O_{78}	I/O_{75}	V_{CC}	I/O_{67} TDI	I/O_{66}
D	I/O_{14}	V_{CC}	I/O_{15}	I/O_{16}	I/O_0	I/O_{79}	I/O_{63}	I/O_{64}	CLK_3/I_4	I/O_{65}
E	I/O_{17}	CLK_0/I_0	I/O_{18}	I/O_{19}	GND	GND	I/O_{60}	I/O_{61}	CLK_2/I_3	I/O_{62}
F	I/O_{22}	$JTAG_{EN}$	I/O_{21}	I/O_{20}	GND	GND	I/O_{59}	I/O_{58}	I_2	I/O_{57}
G	I/O_{27}	CLK_1/I_1	I/O_{26}	I/O_{24}	I/O_{23}	I/O_{56}	I/O_{55}	I/O_{54}	V_{CC}	I/O_{53}
H	I/O_{28}	I/O_{33} TMS	V_{CC}	I/O_{25}	I/O_{39}	I/O_{40}	I/O_{52}	V_{CC}	I/O_{47} TDO	I/O_{51}
J	I/O_{29}	I/O_{32}	I/O_{35}	V_{CC}	I/O_{38}	I/O_{41}	I/O_{43}	I/O_{45}	I/O_{48}	I/O_{50}
K	I/O_{30}	I/O_{31}	I/O_{34}	I/O_{36}	I/O_{37}	I/O_{42}	I/O_{44}	I/O_{46}	I/O_{49}	NC

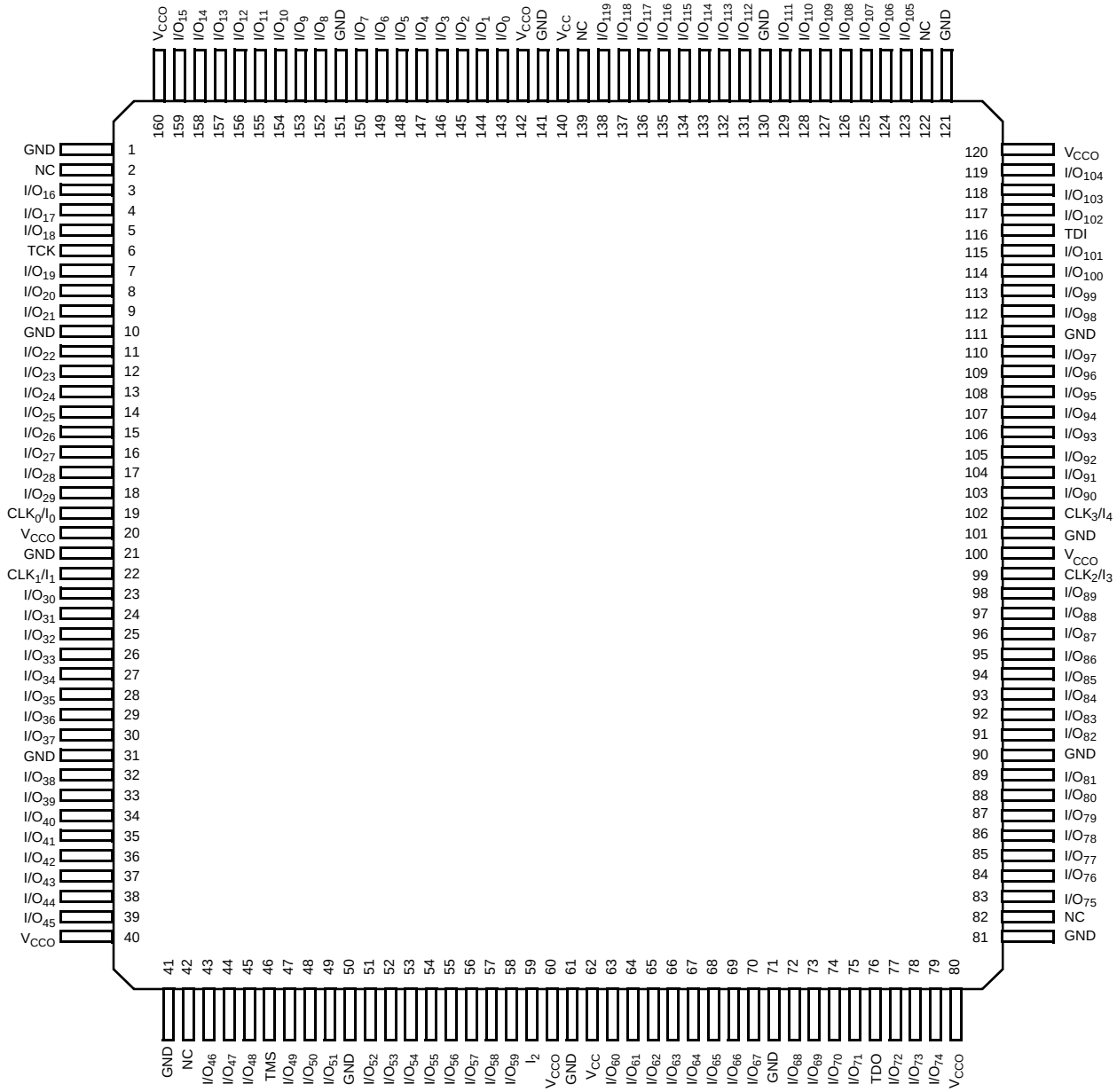
Pin Configurations[19] (continued)

160-Lead TQFP (A160) / CQFP (U162)
for CY37128(V) and CY256(V)
Top View



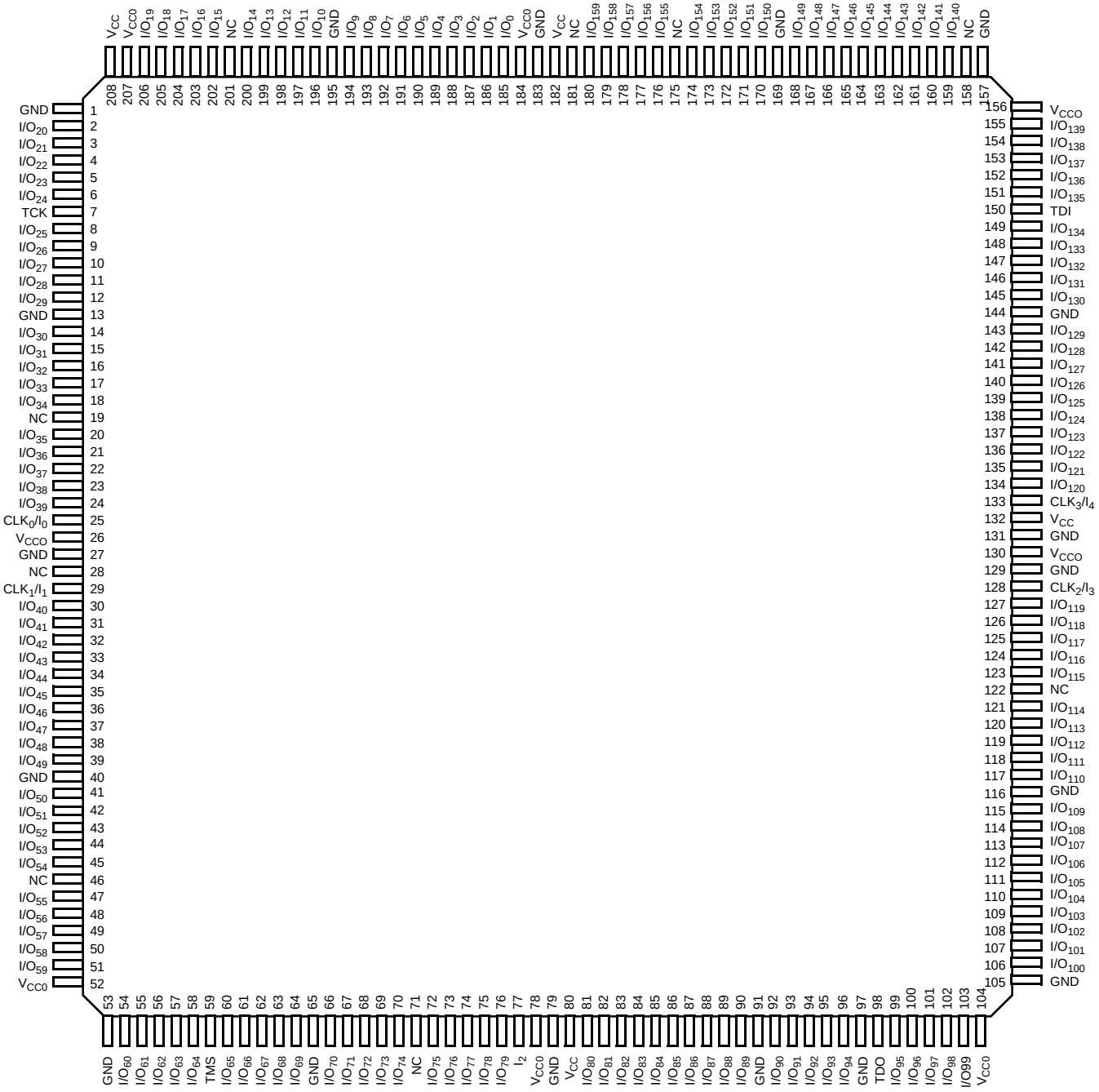
Pin Configurations[19] (continued)

160-Lead TQFP (A160) for CY37192(V)
Top View



Pin Configurations[19] (continued)

208-Lead PQFP (N208) / CQFP (U208)
Top View



Pin Configurations[19] (continued)

256-Ball PBGA (BG256)
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	I/O_{21}	NC	I/O_{16}	I/O_{12}	I/O_{9}	I/O_{7}	I/O_{4}	I/O_{0}	I/O_{190}	I/O_{189}	I/O_{186}	I/O_{182}	NC	I/O_{178}	I/O_{175}	NC	NC	I/O_{169}	I/O_{168}	A
B	I/O_{23}	I/O_{20}	I/O_{19}	I/O_{18}	I/O_{15}	I/O_{11}	I/O_{8}	I/O_{5}	I/O_{1}	I/O_{191}	I/O_{187}	I/O_{185}	I/O_{181}	NC	NC	I/O_{174}	I/O_{171}	I/O_{170}	NC	I/O_{166}	B
C	NC	NC	I/O_{22}	NC	I/O_{17}	I/O_{14}	I/O_{10}	I/O_{6}	I/O_{2}	NC	I/O_{188}	I/O_{184}	I/O_{180}	I/O_{179}	I/O_{176}	I/O_{173}	I/O_{172}	I/O_{167}	I/O_{165}	I/O_{162}	C
D	I/O_{24}	NC	NC	GND	NC	V_{CCO}	I/O_{13}	GND	I/O_{3}	NC	V_{CC}	I/O_{183}	GND	I/O_{177}	V_{CCO}	NC	GND	I/O_{164}	TDI	I/O_{160}	D
E	I/O_{27}	I/O_{26}	I/O_{25}	NC													I/O_{163}	I/O_{161}	I/O_{159}	I/O_{156}	E
F	I/O_{30}	TCK	I/O_{28}	V_{CCO}													V_{CCO}	I/O_{158}	NC	I/O_{154}	F
G	I/O_{33}	I/O_{32}	I/O_{31}	I/O_{29}													I/O_{157}	I/O_{155}	I/O_{153}	I/O_{152}	G
H	I/O_{35}	NC	I/O_{34}	GND				GND	GND	GND	GND	GND	GND				GND	I/O_{151}	I/O_{150}	I/O_{149}	H
J	I/O_{39}	I/O_{38}	I/O_{37}	I/O_{36}				GND	GND	GND	GND	GND	GND				I/O_{148}	I/O_{147}	I/O_{146}	I/O_{145}	J
K	I/O_{42}	I/O_{40}	I/O_{41}	V_{CC}				GND	GND	GND	GND	GND	GND				I/O_{144}	CLK_3/I_4	NC	NC	K
L	I/O_{43}	I/O_{44}	I/O_{45}	I/O_{46}				GND	GND	GND	GND	GND	GND				V_{CC}	CLK_2/I_3	I/O_{143}	NC	L
M	I/O_{47}	CLK_0/I_0	CLK_1/I_1	I/O_{48}				GND	GND	GND	GND	GND	GND				I/O_{139}	I/O_{140}	I/O_{141}	I/O_{142}	M
N	I/O_{49}	I/O_{50}	I/O_{51}	GND				GND	GND	GND	GND	GND	GND				GND	I/O_{136}	I/O_{137}	I/O_{138}	N
P	I/O_{52}	I/O_{53}	I/O_{55}	I/O_{58}													I/O_{131}	I/O_{133}	I/O_{134}	I/O_{135}	P
R	I/O_{54}	I/O_{56}	I/O_{59}	V_{CCO}													V_{CCO}	I/O_{130}	NC	I/O_{132}	R
T	I/O_{57}	I/O_{60}	I/O_{62}	I/O_{65}													I/O_{124}	I/O_{127}	I/O_{128}	I/O_{129}	T
U	I/O_{61}	I/O_{63}	I/O_{66}	GND	I/O_{76}	V_{CCO}	I/O_{82}	GND	I/O_{91}	V_{CC}	I/O_{98}	I/O_{102}	GND	I/O_{112}	V_{CCO}	NC	GND	I/O_{123}	I/O_{122}	I/O_{126}	U
V	I/O_{64}	I/O_{67}	I/O_{69}	I/O_{75}	I/O_{78}	I/O_{81}	I/O_{85}	I/O_{88}	I/O_{92}	I_2	I/O_{97}	I/O_{101}	I/O_{105}	I/O_{109}	I/O_{113}	TDO	I/O_{114}	I/O_{117}	I/O_{121}	I/O_{125}	V
W	I/O_{68}	I/O_{70}	I/O_{72}	I/O_{74}	I/O_{79}	I/O_{83}	I/O_{86}	I/O_{89}	I/O_{93}	I/O_{95}	I/O_{96}	I/O_{100}	I/O_{104}	I/O_{107}	I/O_{110}	NC	NC	I/O_{115}	I/O_{118}	I/O_{120}	W
Y	I/O_{71}	I/O_{73}	I/O_{77}	TMS	I/O_{80}	I/O_{84}	I/O_{87}	I/O_{90}	I/O_{94}	NC	NC	I/O_{99}	I/O_{103}	I/O_{106}	I/O_{108}	I/O_{111}	NC	NC	I/O_{116}	I/O_{119}	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Pin Configurations[19] (continued)

256-Ball Fine-Pitch BGA (BB256)
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	GND	I/O_{26}	I/O_{24}	I/O_{20}	V_{CC}	I/O_{11}	GND	GND	I/O_{186}	V_{CC}	I/O_{177}	I/O_{172}	I/O_{167}	GND	GND
B	GND	I/O_{27}	I/O_{25}	I/O_{23}	I/O_{19}	I/O_{15}	I/O_{10}	GND	GND	I/O_{185}	I/O_{181}	I/O_{176}	I/O_{171}	I/O_{166}	I/O_{165}	GND
C	I/O_{29}	I/O_{28}	NC	I/O_{22}	I/O_{18}	I/O_{14}	I/O_{9}	I/O_{4}	I/O_{191}	I/O_{184}	I/O_{180}	I/O_{175}	I/O_{170}	NC	I/O_{163}	I/O_{164}
D	I/O_{32}	I/O_{31}	I/O_{30}	NC	I/O_{17}	I/O_{13}	I/O_{8}	I/O_{3}	I/O_{190}	I/O_{183}	I/O_{179}	I/O_{174}	I/O_{169}	I/O_{160}	I/O_{161}	I/O_{162}
E	I/O_{35}	I/O_{34}	I/O_{33}	I/O_{21}	I/O_{16}	I/O_{12}	I/O_{7}	I/O_{2}	I/O_{189}	V_{CC}	I/O_{178}	I/O_{173}	I/O_{168}	I/O_{157}	I/O_{158}	I/O_{159}
F	V_{CC}	I/O_{38}	I/O_{37}	I/O_{36}	TCK	V_{CC}	I/O_{6}	I/O_{1}	I/O_{188}	I/O_{182}	V_{CC}	TDI	I/O_{154}	I/O_{155}	I/O_{156}	V_{CC}
G	I/O_{43}	I/O_{42}	I/O_{41}	I/O_{40}	V_{CC}	I/O_{39}	I/O_{5}	I/O_{0}	I/O_{187}	I/O_{148}	I/O_{149}	CLK_3 /I_4	I/O_{150}	I/O_{151}	I/O_{152}	I/O_{153}
H	GND	GND	I/O_{47}	I/O_{46}	CLK_0 /I_0	I/O_{45}	I/O_{44}	GND	GND	I/O_{144}	I/O_{145}	CLK_2 /I_3	I/O_{146}	I/O_{147}	GND	GND
J	GND	GND	I/O_{51}	I/O_{50}	NC	I/O_{49}	I/O_{48}	GND	GND	I/O_{140}	I/O_{141}	I_2	I/O_{142}	I/O_{143}	GND	GND
K	I/O_{57}	I/O_{56}	I/O_{55}	I/O_{54}	CLK_1 /I_1	I/O_{53}	I/O_{52}	I/O_{91}	I/O_{96}	I/O_{101}	I/O_{135}	V_{CC}	I/O_{136}	I/O_{137}	I/O_{138}	I/O_{139}
L	V_{CC}	I/O_{60}	I/O_{59}	I/O_{58}	TMS	V_{CC}	I/O_{86}	I/O_{92}	I/O_{97}	I/O_{102}	V_{CC}	TDO	I/O_{132}	I/O_{133}	I/O_{134}	V_{CC}
M	I/O_{63}	I/O_{62}	I/O_{61}	I/O_{72}	I/O_{77}	I/O_{82}	V_{CC}	I/O_{93}	I/O_{98}	I/O_{103}	I/O_{108}	I/O_{112}	I/O_{117}	I/O_{129}	I/O_{130}	I/O_{131}
N	I/O_{66}	I/O_{65}	I/O_{64}	I/O_{73}	I/O_{78}	I/O_{83}	I/O_{87}	I/O_{94}	I/O_{99}	I/O_{104}	I/O_{109}	I/O_{113}	NC	I/O_{126}	I/O_{127}	I/O_{128}
P	I/O_{68}	I/O_{67}	NC	I/O_{74}	I/O79	I/O_{84}	I/O_{88}	I/O_{95}	I/O_{100}	I/O_{105}	I/O_{110}	I/O_{114}	I/O_{118}	NC	I/O_{124}	I/O_{125}
R	GND	I/O_{69}	I/O_{70}	I/O_{75}	I/O_{80}	I/O_{85}	I/O_{89}	GND	GND	I/O_{106}	I/O_{111}	I/O_{115}	I/O_{119}	I/O_{121}	I/O_{123}	GND
T	GND	GND	I/O_{71}	I/O_{76}	I/O_{81}	V_{CC}	I/O_{90}	GND	GND	I/O_{107}	V_{CC}	I/O_{116}	I/O_{120}	I/O_{122}	GND	GND

Pin Configurations[19] (continued)

352-Lead BGA (BG352)

Top View

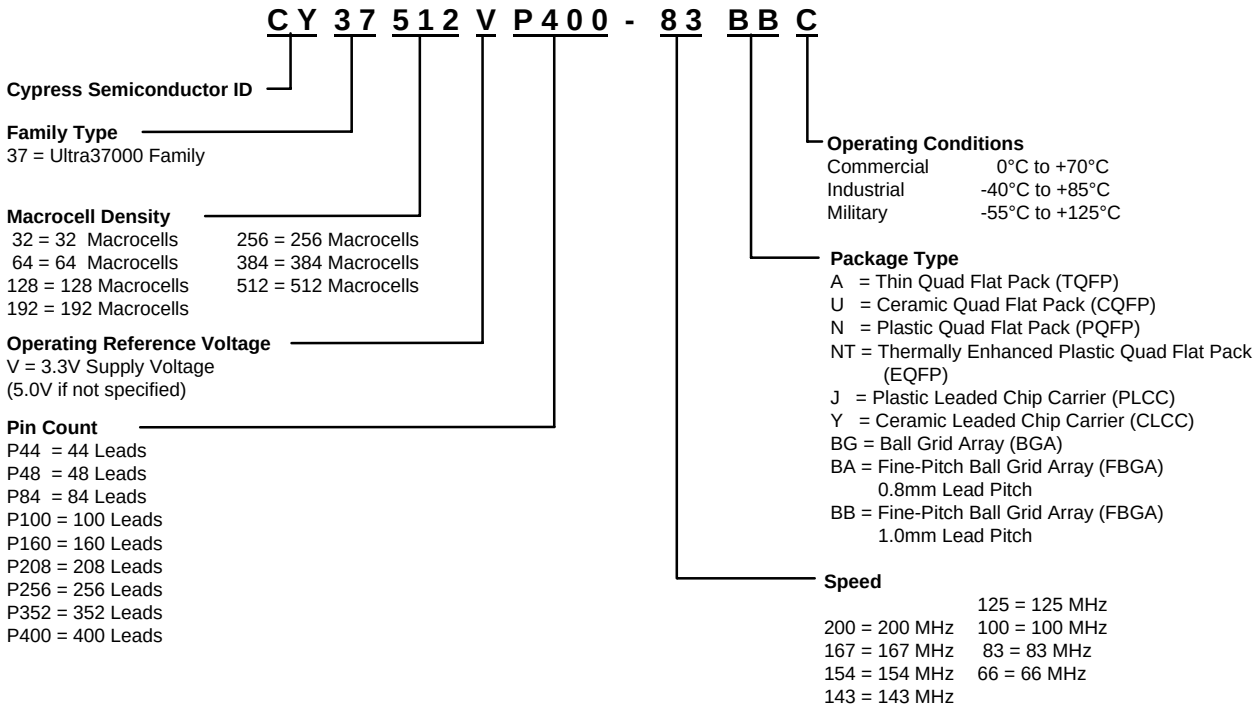
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	GND	GND	I/O_{19}	I/O_{15}	I/O_{13}	I/O_{34}	I/O_{31}	I/O_{28}	I/O_{25}	I/O_{10}	I/O_{7}	I/O_{4}	I/O_{1}	I/O_{263}	I/O_{260}	I/O_{257}	I/O_{254}	I/O_{239}	I/O_{237}	I/O_{232}	I/O_{229}	I/O_{250}	I/O_{248}	I/O_{244}	GND	GND
B	GND	NC	I/O_{18}	I/O_{17}	I/O_{14}	I/O_{35}	I/O_{32}	I/O_{29}	I/O_{26}	I/O_{11}	I/O_{8}	I/O_{5}	I/O_{2}	V_{CC}	I/O_{261}	I/O_{258}	I/O_{255}	I/O_{252}	I/O_{234}	I/O_{231}	I/O_{228}	I/O_{249}	I/O_{246}	I/O_{245}	I/O_{240}	GND
C	I/O_{23}	I/O_{38}	I/O_{37}	I/O_{16}	I/O_{12}	I/O_{33}	I/O_{30}	I/O_{27}	I/O_{24}	I/O_{9}	I/O_{6}	I/O_{3}	I/O_{0}	I/O_{262}	I/O_{259}	I/O_{256}	I/O_{253}	I/O_{238}	I/O_{235}	I/O_{233}	I/O_{230}	I/O_{251}	I/O_{247}	I/O_{225}	I/O_{224}	I/O_{227}
D	I/O_{39}	I/O_{40}	I/O_{36}	NC	NC	I/O_{21}	I/O_{20}	V_{CCO}	V_{CCO}	NC	GND	GND	V_{CCO}	V_{CCO}	GND	GND	NC	V_{CCO}	V_{CCO}	I/O_{236}	I/O_{243}	NC	NC	I/O_{226}	I/O_{222}	I/O_{223}
E	I/O_{42}	TCK	I/O_{41}	NC																			NC	TDI	I/O_{221}	I/O_{220}
F	I/O_{45}	I/O_{44}	I/O_{43}	I/O_{22}																			I/O_{242}	I/O_{219}	I/O_{218}	I/O_{217}
G	I/O_{48}	I/O_{47}	I/O_{46}	I/O_{63}																			I/O_{241}	I/O_{216}	I/O_{215}	I/O_{214}
H	I/O_{49}	I/O_{50}	I/O_{51}	V_{CCO}																			V_{CCO}	I/O_{211}	I/O_{212}	I/O_{213}
J	I/O_{52}	I/O_{53}	I/O_{54}	V_{CCO}																			V_{CCO}	I/O_{208}	I/O_{209}	I/O_{210}
K	I/O_{55}	I/O_{56}	I/O_{57}	NC																			NC	I/O_{205}	I/O_{206}	I/O_{207}
L	I0	I/O_{59}	I/O_{58}	GND							GND	GND	GND	GND	GND	GND							GND	I/O_{204}	I4	I/O_{197}
M	I/O_{61}	I/O_{60}	I1	GND							GND	GND	GND	GND	GND	GND							GND	I3	I/O_{203}	I/O_{202}
N	I/O_{64}	V_{CC}	I/O_{62}	V_{CCO}							GND	GND	GND	GND	GND	GND							V_{CCO}	I/O_{201}	I/O_{200}	I/O_{199}
P	I/O_{65}	I/O_{66}	I/O_{67}	V_{CCO}							GND	GND	GND	GND	GND	GND							V_{CCO}	I/O_{196}	V_{CC}	I/O_{198}
R	I/O_{68}	I/O_{69}	I/O_{70}	GND							GND	GND	GND	GND	GND	GND							GND	I/O_{193}	I/O_{194}	I/O_{195}
T	I/O_{71}	I/O_{84}	I/O_{85}	GND							GND	GND	GND	GND	GND	GND							GND	I/O_{178}	I/O_{179}	I/O_{192}
U	I/O_{88}	I/O_{87}	I/O_{86}	NC																			NC	I/O_{177}	I/O_{176}	I/O_{175}
V	I/O_{91}	I/O_{90}	I/O_{89}	V_{CCO}																			V_{CCO}	I/O_{174}	I/O_{173}	I/O_{172}
W	I/O_{94}	I/O_{93}	I/O_{92}	V_{CCO}																			V_{CCO}	I/O_{171}	I/O_{170}	I/O_{169}
Y	I/O_{95}	I/O_{72}	I/O_{73}	I/O_{110}																			I/O_{153}	I/O_{190}	I/O_{191}	I/O_{168}
AA	I/O_{74}	I/O_{75}	I/O_{76}	I/O_{111}																			I/O_{152}	I/O_{187}	I/O_{188}	I/O_{189}
AB	I/O_{77}	I/O_{78}	I/O_{79}	N/C																			NC	I/O_{184}	I/O_{185}	I/O_{186}
AC	I/O_{81}	I/O_{80}	I/O_{108}	N/C	NC	I/O_{112}	I/O_{113}	V_{CCO}	V_{CCO}	NC	GND	GND	V_{CCO}	V_{CCO}	GND	GND	NC	V_{CCO}	V_{CCO}	I/O_{150}	I/O_{151}	NC	NC	I/O_{155}	I/O_{183}	I/O_{182}
AD	I/O_{109}	I/O_{82}	I/O_{83}	I/O_{117}	I/O_{97}	I/O_{100}	I/O_{102}	I/O_{105}	I/O_{120}	I/O_{123}	I/O_{126}	I/O_{129}	I2	I/O_{133}	I/O_{136}	I/O_{139}	I/O_{142}	I/O_{157}	I/O_{159}	I/O_{161}	I/O_{163}	I/O_{166}	I/O_{146}	I/O_{180}	I/O_{181}	I/O_{154}
AE	GND	NC	I/O_{115}	I/O_{116}	I/O_{119}	I/O_{98}	I/O_{101}	I/O_{103}	I/O_{106}	I/O_{121}	I/O_{124}	I/O_{127}	V_{CC}	I/O_{130}	I/O_{134}	I/O_{137}	I/O_{140}	I/O_{143}	I/O_{160}	I/O_{162}	I/O_{165}	I/O_{144}	I/O_{147}	I/O_{148}	NC	GND
AF	GND	GND	I/O_{114}	I/O_{118}	I/O_{96}	I/O_{99}	TMS	I/O_{104}	I/O_{107}	I/O_{122}	I/O_{125}	I/O_{128}	I/O_{131}	I/O_{132}	I/O_{135}	I/O_{138}	I/O_{141}	I/O_{156}	I/O_{158}	TDO	I/O_{164}	I/O_{167}	I/O_{145}	I/O_{149}	GND	GND

Pin Configurations[19] (continued)

400-Ball Fine-Pitch BGA (BB400)
Top View

A	GND	GND	NC	I/O_{17}	I/O_{16}	I/O_{14}	I/O_{29}	V_{CC}	I/O_{11}	GND	GND	I/O_{257}	V_{CC}	I/O_{239}	I/O_{233}	I/O_{232}	I/O_{230}	NC	GND	GND
B	GND	GND	GND	NC	I/O_{15}	I/O_{13}	I/O_{28}	V_{CC}	I/O_{10}	GND	GND	I/O_{256}	V_{CC}	I/O_{238}	I/O_{231}	I/O_{229}	NC	GND	GND	GND
C	NC	GND	GND	GND	I/O_{20}	I/O_{12}	I/O_{27}	V_{CC}	I/O_{9}	GND	GND	I/O_{255}	V_{CC}	I/O_{237}	I/O_{228}	I/O_{245}	GND	GND	GND	NC
D	I/O_{44}	NC	GND	I/O_{21}	I/O_{19}	I/O_{18}	I/O_{26}	I/O_{25}	I/O_{8}	GND	GND	I/O_{254}	I/O_{235}	I/O_{236}	I/O_{251}	I/O_{244}	I/O_{243}	GND	NC	I/O_{227}
E	I/O_{46}	I/O_{43}	I/O_{23}	I/O_{22}	NC	I/O_{35}	I/O_{34}	I/O_{24}	I/O_{7}	I/O_{4}	I/O_{263}	I/O_{253}	I/O_{234}	I/O_{250}	I/O_{248}	NC	I/O_{241}	I/O_{242}	I/O_{225}	I/O_{226}
F	I/O_{47}	I/O_{45}	I/O_{42}	I/O_{41}	I/O_{40}	NC	I/O_{33}	I/O_{32}	I/O_{6}	I/O_{3}	I/O_{262}	I/O_{252}	I/O_{249}	I/O_{247}	I/O_{220}	I/O_{221}	I/O_{240}	I/O_{222}	I/O_{223}	I/O_{224}
G	I/O_{53}	I/O_{52}	I/O_{51}	I/O_{50}	I/O_{39}	I/O_{38}	I/O_{37}	I/O_{31}	I/O_{5}	I/O_{2}	I/O_{261}	V_{CC}	I/O_{246}	I/O_{217}	I/O_{218}	I/O_{219}	I/O_{212}	I/O_{213}	I/O_{214}	I/O_{215}
H	V_{CC}	V_{CC}	V_{CC}	I/O_{49}	I/O_{48}	I/O_{36}	TCK	V_{CC}	I/O_{30}	I/O_{1}	I/O_{259}	I/O_{260}	V_{CC}	TDI	I/O_{216}	I/O_{210}	I/O_{211}	V_{CC}	V_{CC}	V_{CC}
J	I/O_{59}	I/O_{58}	I/O_{57}	I/O_{56}	I/O_{55}	I/O_{54}	V_{CC}	I/O_{62}	I/O_{60}	I/O_{0}	I/O_{258}	I/O_{202}	I/O_{203}	CLK_3 /I_4	I/O_{204}	I/O_{205}	I/O_{206}	I/O_{207}	I/O_{208}	I/O_{209}
K	GND	GND	GND	GND	I/O_{65}	I/O_{64}	CLK_0 /I_0	I/O_{63}	I/O_{61}	GND	GND	I/O_{198}	I/O_{199}	CLK_2 /I_3	I/O_{200}	I/O_{201}	GND	GND	GND	GND
L	GND	GND	GND	GND	I/O_{69}	I/O_{68}	NC	I/O_{67}	I/O_{66}	GND	GND	I/O_{193}	I/O_{195}	I_2	I/O_{196}	I/O_{197}	GND	GND	GND	GND
M	I/O_{89}	I/O_{88}	I/O_{87}	I/O_{86}	I/O_{85}	I/O_{84}	CLK_1 /I_1	I/O_{71}	I/O_{70}	I/O_{126}	I/O_{132}	I/O_{192}	I/O_{194}	V_{CC}	I/O_{174}	I/O_{175}	I/O_{176}	I/O_{177}	I/O_{178}	I/O_{179}
N	V_{CC}	V_{CC}	V_{CC}	I/O_{91}	I/O_{90}	I/O_{72}	TMS	V_{CC}	I/O_{128}	I/O_{127}	I/O_{133}	I/O_{162}	V_{CC}	TDO	I/O_{180}	I/O_{168}	I/O_{169}	V_{CC}	V_{CC}	V_{CC}
P	I/O_{95}	I/O_{94}	I/O_{93}	I/O_{92}	I/O_{75}	I/O_{74}	I/O_{73}	I/O_{114}	V_{CC}	I/O_{129}	I/O_{134}	I/O_{137}	I/O_{163}	I/O_{181}	I/O_{182}	I/O_{183}	I/O_{170}	I/O_{171}	I/O_{172}	I/O_{173}
R	I/O_{80}	I/O_{79}	I/O_{78}	I/O_{108}	I/O_{77}	I/O_{76}	I/O_{115}	I/O_{117}	I/O_{120}	I/O_{130}	I/O_{135}	I/O_{138}	I/O_{164}	I/O_{165}	NC	I/O_{184}	I/O_{185}	I/O_{186}	I/O_{189}	I/O_{191}
T	I/O_{82}	I/O_{81}	I/O_{110}	I/O_{109}	NC	I/O_{116}	I/O_{118}	I/O_{102}	I/O_{121}	I/O_{131}	I/O_{136}	I/O_{139}	I/O_{156}	I/O_{166}	I/O_{167}	NC	I/O_{154}	I/O_{155}	I/O_{187}	I/O_{190}
U	I/O_{83}	NC	GND	I/O_{111}	I/O_{112}	I/O_{119}	I/O_{104}	I/O_{103}	I/O_{122}	GND	GND	I/O_{140}	I/O_{157}	I/O_{158}	I/O_{150}	I/O_{151}	I/O_{153}	GND	NC	I/O_{188}
V	NC	GND	GND	GND	I/O_{113}	I/O_{96}	I/O_{105}	V_{CC}	I/O_{123}	GND	GND	I/O_{141}	V_{CC}	I/O_{159}	I/O144	I/O_{152}	GND	GND	GND	NC
W	GND	GND	GND	NC	I/O_{97}	I/O_{99}	I/O_{106}	V_{CC}	I/O_{124}	GND	GND	I/O_{142}	V_{CC}	I/O_{160}	I/O_{145}	I/O_{147}	NC	GND	GND	GND
Y	GND	GND	NC	I/O_{98}	I/O_{100}	I/O_{101}	I/O_{107}	V_{CC}	I/O_{125}	GND	GND	I/O_{143}	V_{CC}	I/O_{161}	I/O_{146}	I/O_{148}	I/O_{149}	NC	GND	GND

Ordering Information



5.0V Ordering Information

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	200	CY37032P44-200AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-200JC	J67	44-Lead Plastic Leaded Chip Carrier	
	154	CY37032P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
	125	CY37032P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	

5.0V Ordering Information (continued)

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	200	CY37064P44-200AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-200JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-200JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-200AC	A100	100-Lead Thin Quad Flat Pack	
	154	CY37064P44-154AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-154JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-154JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P44-154AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-154JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-154JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-154AI	A100	100-Lead Thin Quad Flat Pack	
		5962-9951902QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military
	125	CY37064P44-125AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37064P44-125JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37064P44-125AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37064P44-125JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064P100-125AI	A100	100-Lead Thin Quad Flat Pack	
		5962-9951901QYA	Y67	44-Lead Ceramic Leadless Chip Carrier	Military
128	167	CY37128P84-167JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P100-167AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P160-167AC	A160	160-Lead Thin Quad Flat Pack	
	125	CY37128P84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P160-125AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128P84-125JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
		CY37128P100-125AI	A100	100-Lead Thin Quad Flat Pack	
		CY37128P160-125AI	A160	160-Lead Thin Quad Flat Pack	
		5962-9952102QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
	100	CY37128P84-100JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128P100-100AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128P160-100AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128P84-100JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
		CY37128P100-100AI	A100	100-Lead Thin Quad Flat Pack	
		CY37128P160-100AI	A160	160-Lead Thin Quad Flat Pack	
		5962-9952101QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military

5.0V Ordering Information (continued)

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
192	154	CY37192P160-154AC	A160	160-Lead Thin Quad Flat Pack	Commercial
	125	CY37192P160-125AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192P160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
	83	CY37192P160-83AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192P160-83AI	A160	160-Lead Thin Quad Flat Pack	Industrial
256	154	CY37256P160-154AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P208-154NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-154BGC	BG256	256-Lead Ball Grid Array	
	125	CY37256P160-125AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P208-125NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGC	BG256	256-Lead Ball Grid Array	
		CY37256P160-125AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P208-125NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-125BGI	BG256	256-Lead Ball Grid Array	
		5962-9952302QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
	83	CY37256P160-83AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256P208-83NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGC	BG256	256-Lead Ball Grid Array	
		CY37256P160-83AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256P208-83NI	N208	208-Lead Plastic Quad Flat Pack	
		CY37256P256-83BGI	BG256	256-Lead Ball Grid Array	
		5962-9952301QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	125	CY37384P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-125BGC	BG256	256-Lead Ball Grid Array	
	83	CY37384P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384P256-83BGC	BG256	256-Lead Ball Grid Array	
		CY37384P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384P256-83BGI	BG256	256-Lead Ball Grid Array	

5.0V Ordering Information (continued)

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
512	125	CY37512P208-125NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-125BGC	BG256	256-Lead Ball Grid Array	
		CY37512P352-125BGC	BG352	352-Lead Ball Grid Array	
	100	CY37512P208-100NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-100BGC	BG256	256-Lead Ball Grid Array	
		CY37512P352-100BGC	BG352	352-Lead Ball Grid Array	
		CY37512P208-100NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-100BGI	BG256	256-Lead Ball Grid Array	
		CY37512P352-100BGI	BG352	352-Lead Ball Grid Array	
		5962-9952502QZC	U208	208-Lead Ceramic Quad Flat Pack	Military
	83	CY37512P208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512P256-83BGC	BG256	256-Lead Ball Grid Array	
		CY37512P352-83BGC	BG352	352-Lead Ball Grid Array	
		CY37512P208-83NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512P256-83BGI	BG256	256-Lead Ball Grid Array	
		CY37512P352-83BGI	BG352	352-Lead Ball Grid Array	
		5962-9952501QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

3.3V Ordering Information

Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
32	143	CY37032VP44-143AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-143JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032VP48-143BAC	BA50	48-Lead Fine Pitch Ball Grid Array	
	100	CY37032VP44-100AC	A44	44-Lead Thin Quad Flat Pack	Commercial
		CY37032VP44-100JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032VP48-100BAC	BA50	48-Lead Fine Pitch Ball Grid Array	
		CY37032VP44-100AI	A44	44-Lead Thin Quad Flat Pack	Industrial
		CY37032VP44-100JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37032VP48-100BAI	BA50	48-Lead Fine Pitch Ball Grid Array	

3.3V Ordering Information (continued)

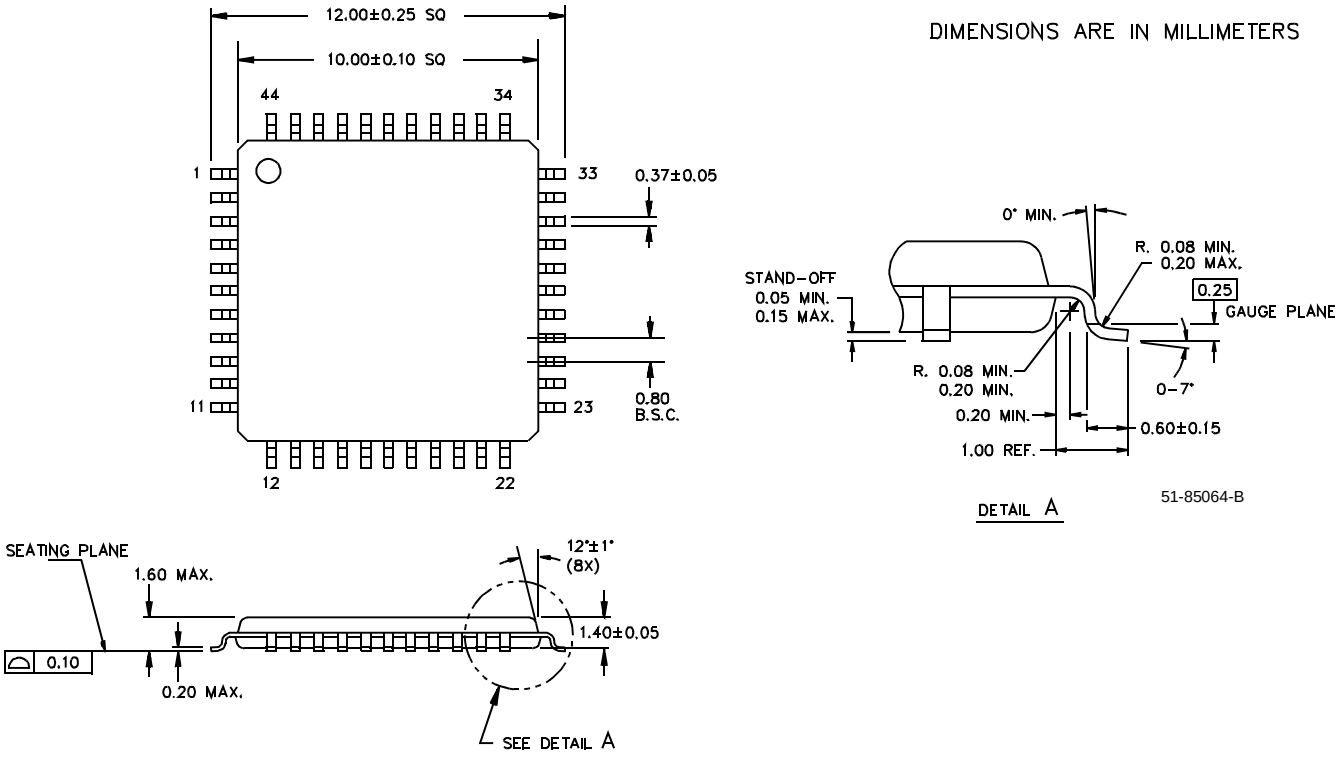
Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
64	143	CY37064VP44-143AC	A44	44-Lead Thin Quad Flatpack	Commercial
		CY37064VP44-143JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064VP48-143BAC	BA50	48-Lead Fine-Pitch Ball Grid Array	
		CY37064VP84-143JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064VP100-143AC	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-143BBC	BB100	100-Lead Fine-Pitch Ball Grid Array	
	100	CY37064VP44-100AC	A44	44-Lead Thin Quad Flatpack	Commercial
		CY37064VP44-100JC	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064VP48-100BAC	BA50	48-Lead Fine-Pitch Ball Grid Array	
		CY37064VP84-100JC	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064VP100-100AC	A100	100-Lead Thin Quad Flatpack	
		CY37064VP100-100BBC	BB100	100-Lead Fine-Pitch Ball Grid Array	
		CY37064VP44-100AI	A44	44-Lead Thin Quad Flatpack	Industrial
		CY37064VP44-100JI	J67	44-Lead Plastic Leaded Chip Carrier	
		CY37064VP48-100BAI	BA50	48-Lead Fine-Pitch Ball Grid Array	
		CY37064VP84-100JI	J83	84-Lead Plastic Leaded Chip Carrier	
		CY37064VP100-100BBI	BB100	100-Lead Fine-Pitch Ball Grid Array	
		CY37064VP100-100AI	A100	100-Lead Thin Quad Flatpack	
		5962-9952001QYA	Y67	44-Lead Ceramic Leaded Chip Carrier	Military
128	125	CY37128VP84-125JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128VP100-125AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128VP100-125BBC	BB100	100-Lead Fine-Pitch Ball Grid Array	
		CY37128VP160-125AC	A160	160-Lead Thin Quad Flat Pack	
	83	CY37128VP84-83JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
		CY37128VP100-83AC	A100	100-Lead Thin Quad Flat Pack	
		CY37128VP100-83BBC	BB100	100-Lead Fine-Pitch Ball Grid Array	
		CY37128VP160-83AC	A160	160-Lead Thin Quad Flat Pack	
		CY37128VP84-83JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
		CY37128VP100-83AI	A100	100-Lead Thin Quad Flat Pack	
		CY37128VP100-83BBI	BB100	100-Lead Fine-Pitch Ball Grid Array	
		CY37128VP160-83AI	A160	160-Lead Thin Quad Flat Pack	
		5962-9952201QYA	Y84	84-Lead Ceramic Leaded Chip Carrier	Military
192	100	CY37192VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
	66	CY37192VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37192VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial

3.3V Ordering Information (continued)

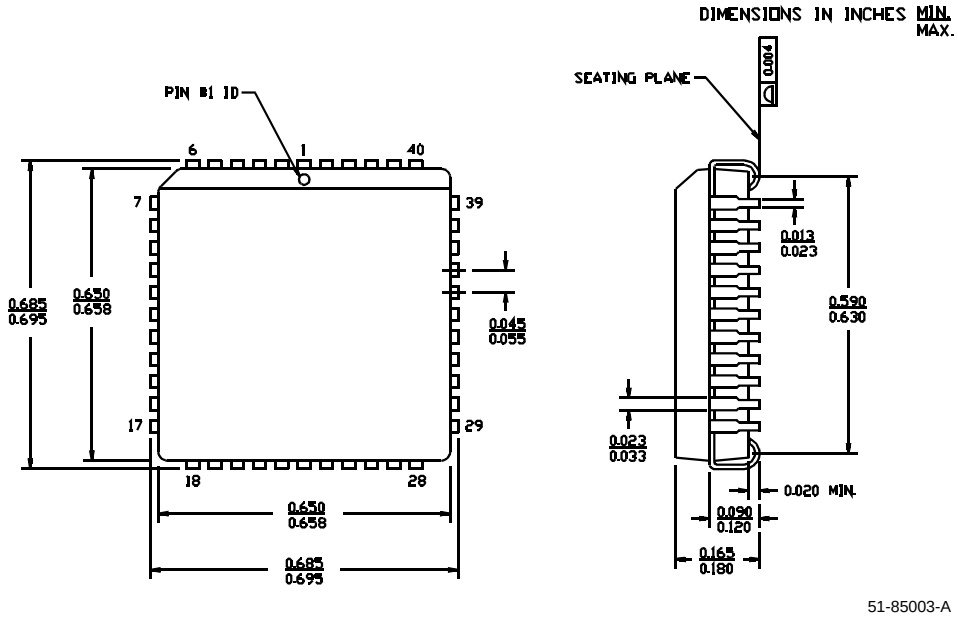
Macro-cells	Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
256	100	CY37256VP160-100AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP208-100NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-100BGC	BG256	256-Lead Ball Grid Array	
		CY37256VP256-100BBC	BB256	256-Lead Fine-Pitch Ball Grid Array	
	66	CY37256VP160-66AC	A160	160-Lead Thin Quad Flat Pack	Commercial
		CY37256VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	
		CY37256VP256-66BGC	BG256	256-Lead Ball Grid Array	
		CY37256VP256-66BBC	BB256	256-Lead Fine-Pitch Ball Grid Array	
		CY37256VP160-66AI	A160	160-Lead Thin Quad Flat Pack	Industrial
		CY37256VP256-66BGI	BG256	256-Lead Ball Grid Array	
		CY37256VP256-66BBI	BB256	256-Lead Fine-Pitch Ball Grid Array	
		5962-9952401QZC	U162	160-Lead Ceramic Quad Flat Pack	Military
384	83	CY37384VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-83BGC	BG256	256-Lead Ball Grid Array	
	66	CY37384VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37384VP256-66BGC	BG256	256-Lead Ball Grid Array	
		CY37384VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37384VP256-66BGI	BG256	256-Lead Ball Grid Array	
512	83	CY37512VP208-83NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-83BGC	BG256	256-Lead Ball Grid Array	
		CY37512VP352-83BGC	BG352	352-Lead Ball Grid Array	
		CY37512VP400-83BBC	BB400	400-Lead Fine-Pitch Ball Grid Array	
	66	CY37512VP208-66NC	N208	208-Lead Plastic Quad Flat Pack	Commercial
		CY37512VP256-66BGC	BG256	256-Lead Ball Grid Array	
		CY37512VP352-66BGC	BG352	352-Lead Ball Grid Array	
		CY37512VP400-66BBC	BB400	400-Lead Fine-Pitch Ball Grid Array	
		CY37512VP208-66NI	N208	208-Lead Plastic Quad Flat Pack	Industrial
		CY37512VP256-66BGI	BG256	256-Lead Ball Grid Array	
		CY37512VP352-66BGI	BG352	352-Lead Ball Grid Array	
		CY37512VP400-66BBI	BB400	400-Lead Fine-Pitch Ball Grid Array	
		5962-9952601QZC	U208	208-Lead Ceramic Quad Flat Pack	Military

Package Diagrams

44-Lead Thin Plastic Quad Flat Pack A44

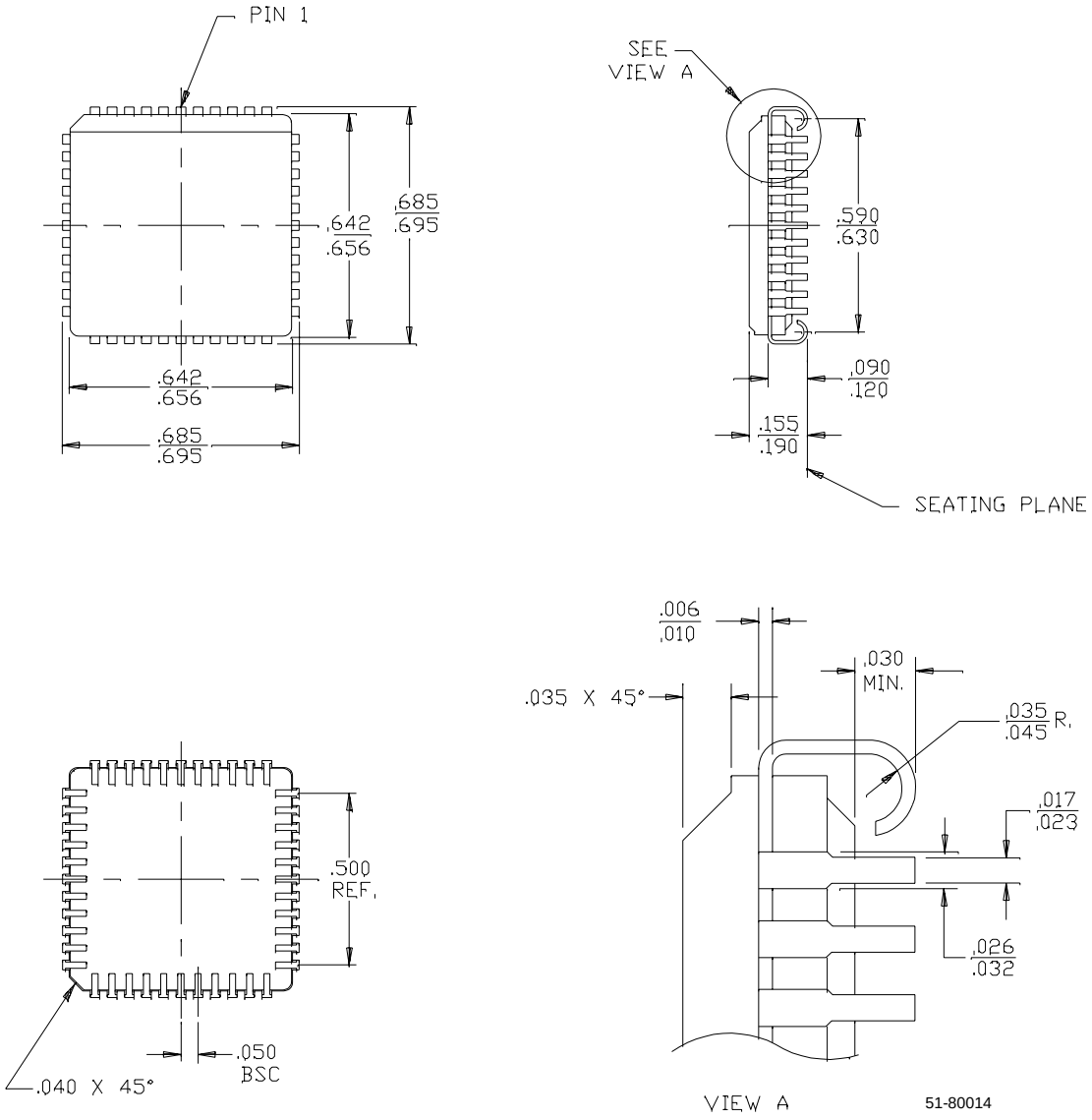


44-Lead Plastic Leaded Chip Carrier J67



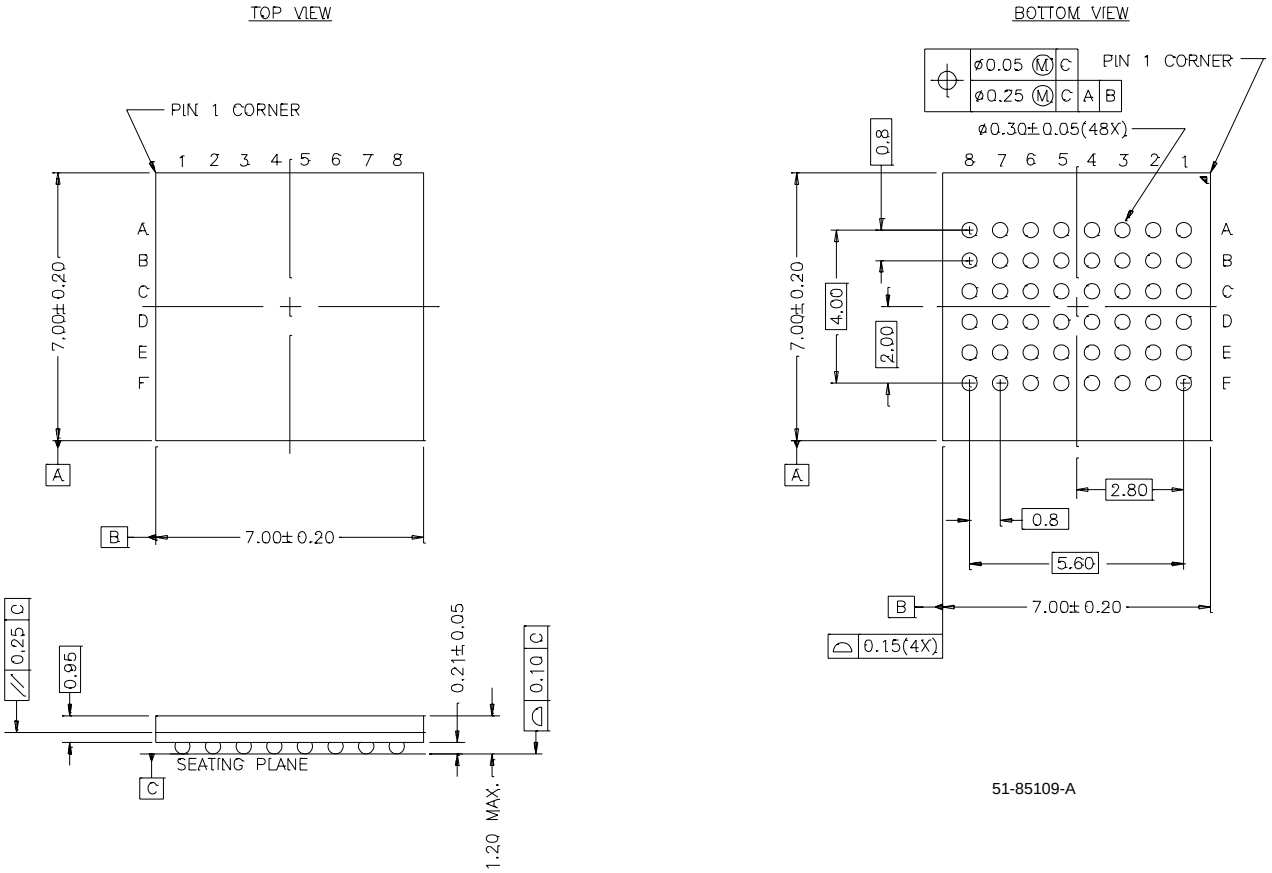
Package Diagrams (continued)

44-Pin Ceramic Leaded Chip Carrier Y67



Package Diagrams (continued)

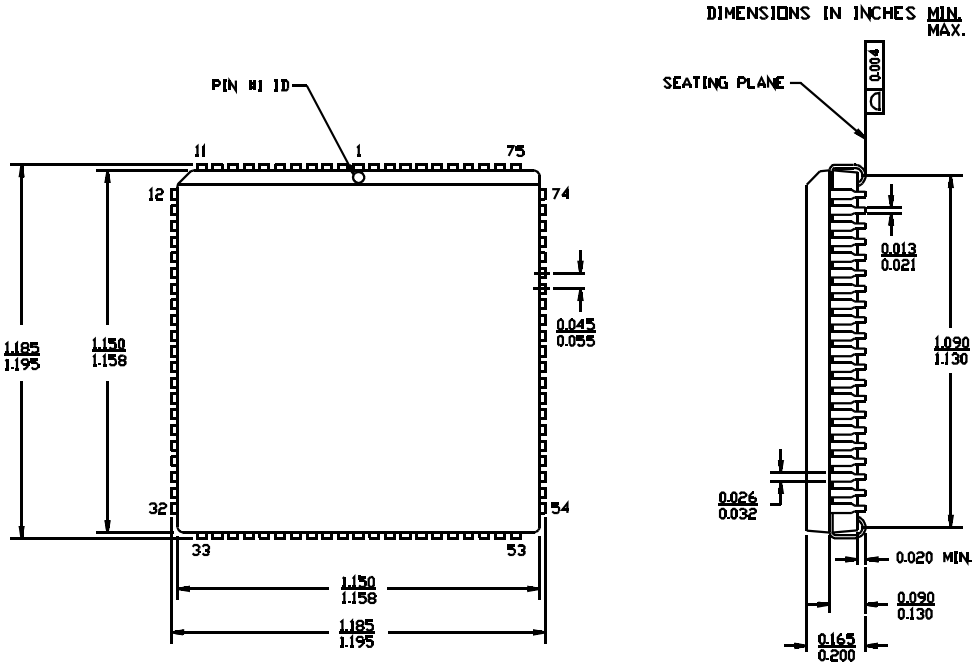
48-Ball (7.0 mm x 7.0 mm x 1.1 mm, 0.80 pitch) Thin BGA BA50



51-85109-A

Package Diagrams (continued)

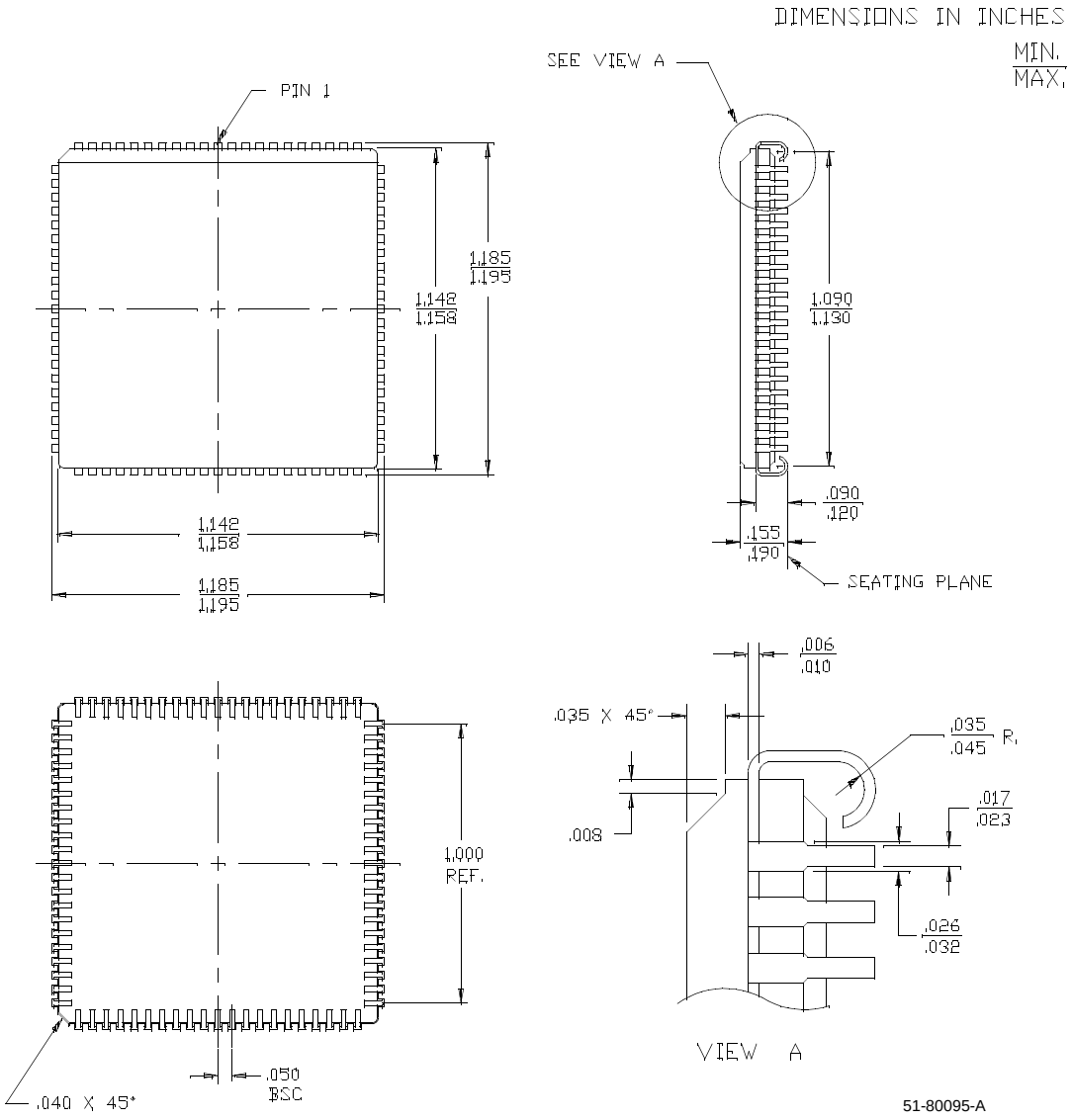
84-Lead Plastic Leaded Chip Carrier J83



51-85006-A

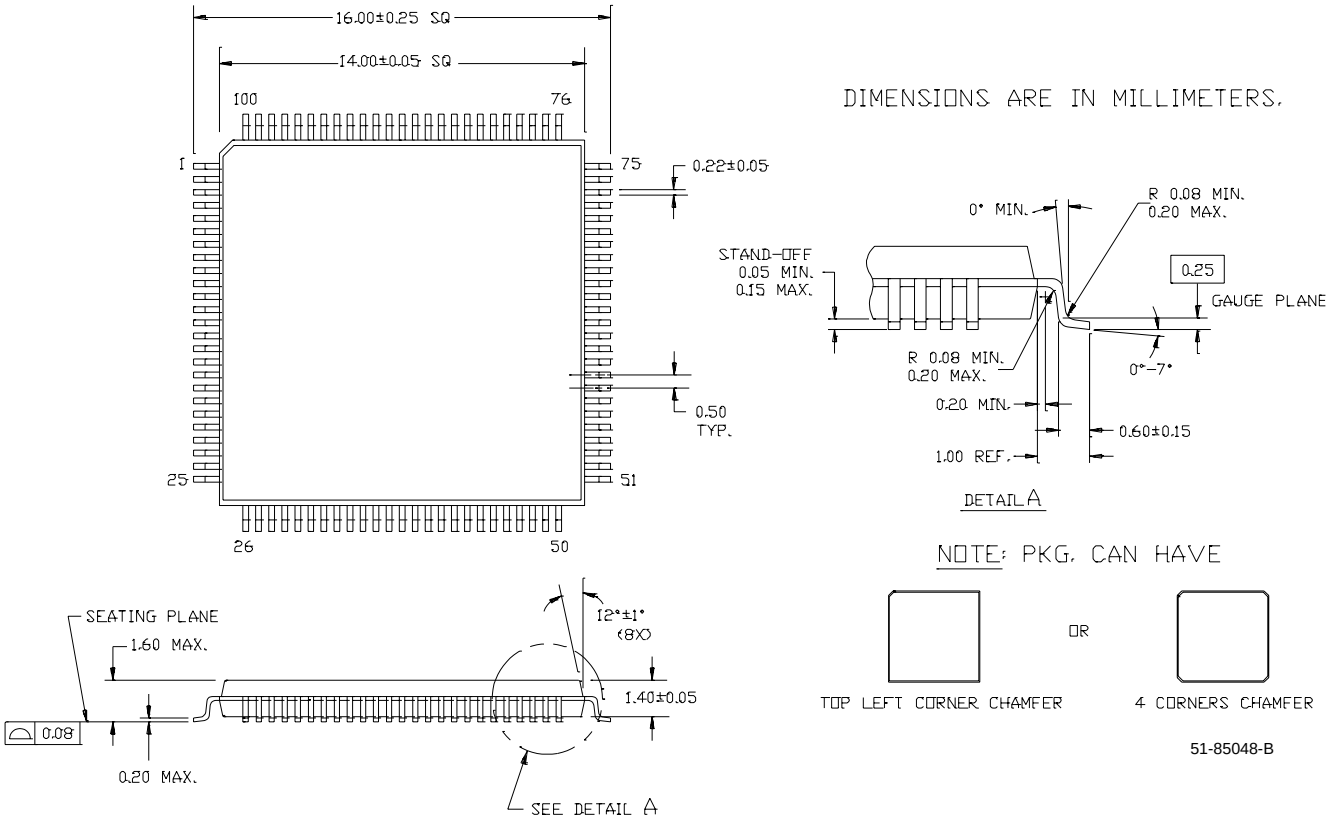
Package Diagrams (continued)

84-Pin Ceramic Leaded Chip Carrier Y84



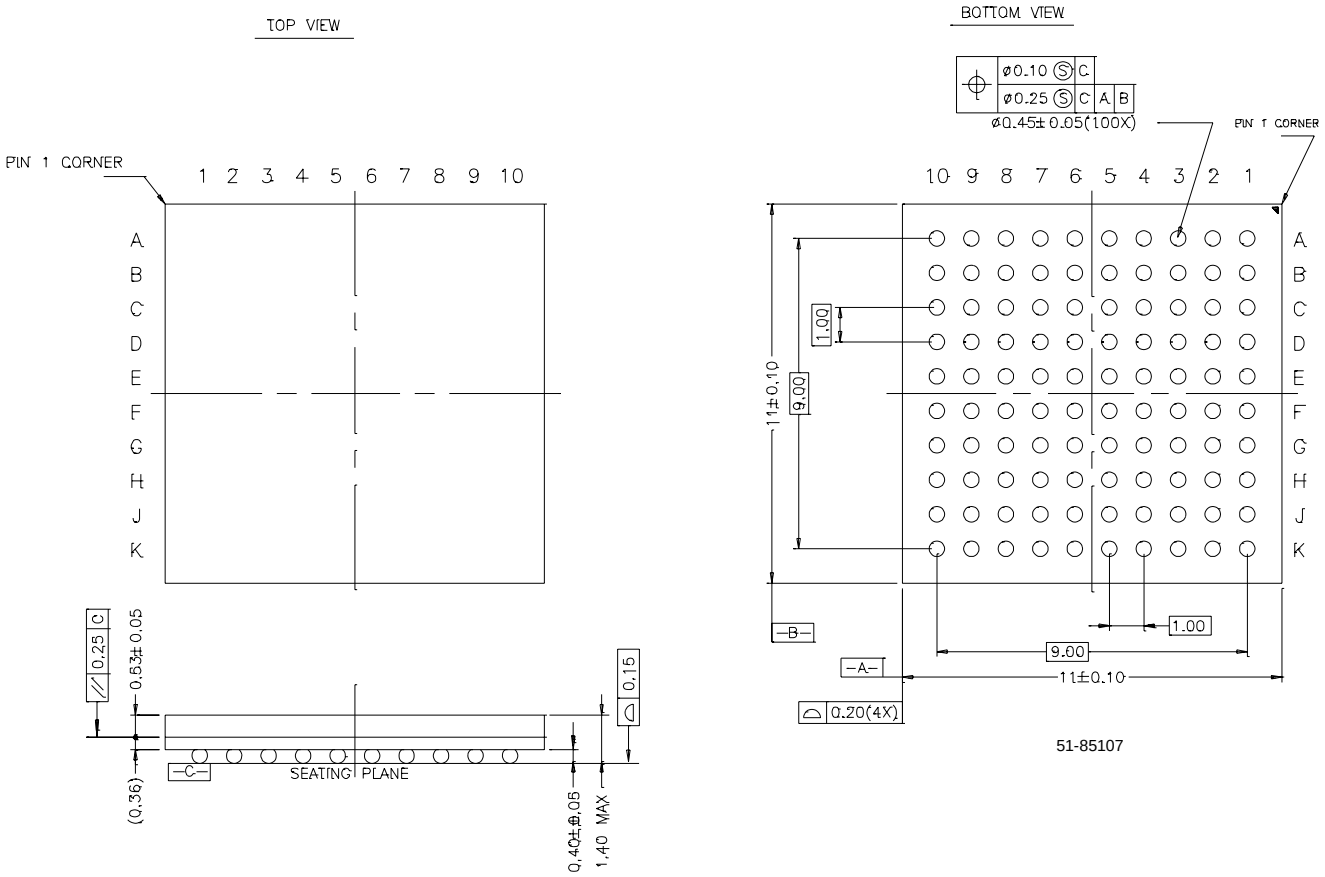
Package Diagrams (continued)

100-Pin Thin Plastic Quad Flat Pack (TQFP) A100



Package Diagrams (continued)

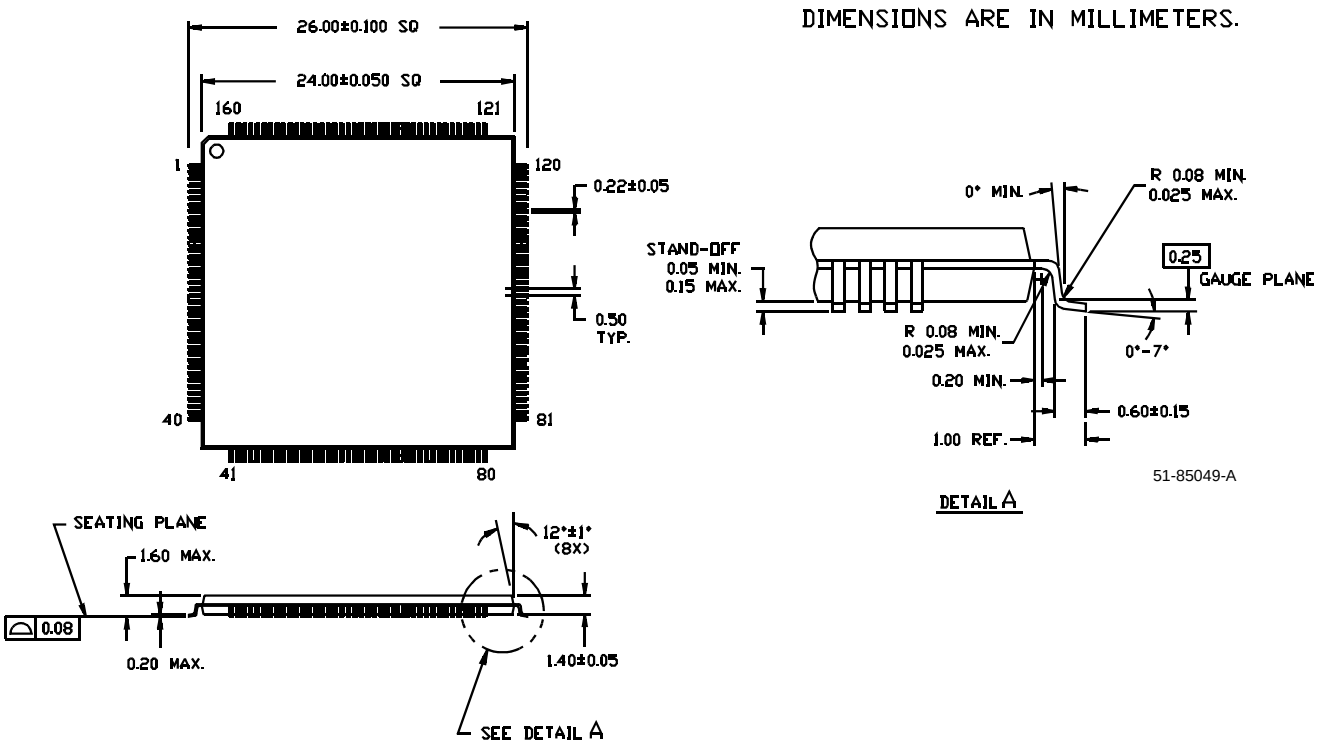
100-Ball Thin Ball Grid Array (11 x 11 x 1.4 mm) BB100



* THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC M0192 (LOW PROFILE BGA FAMILY)

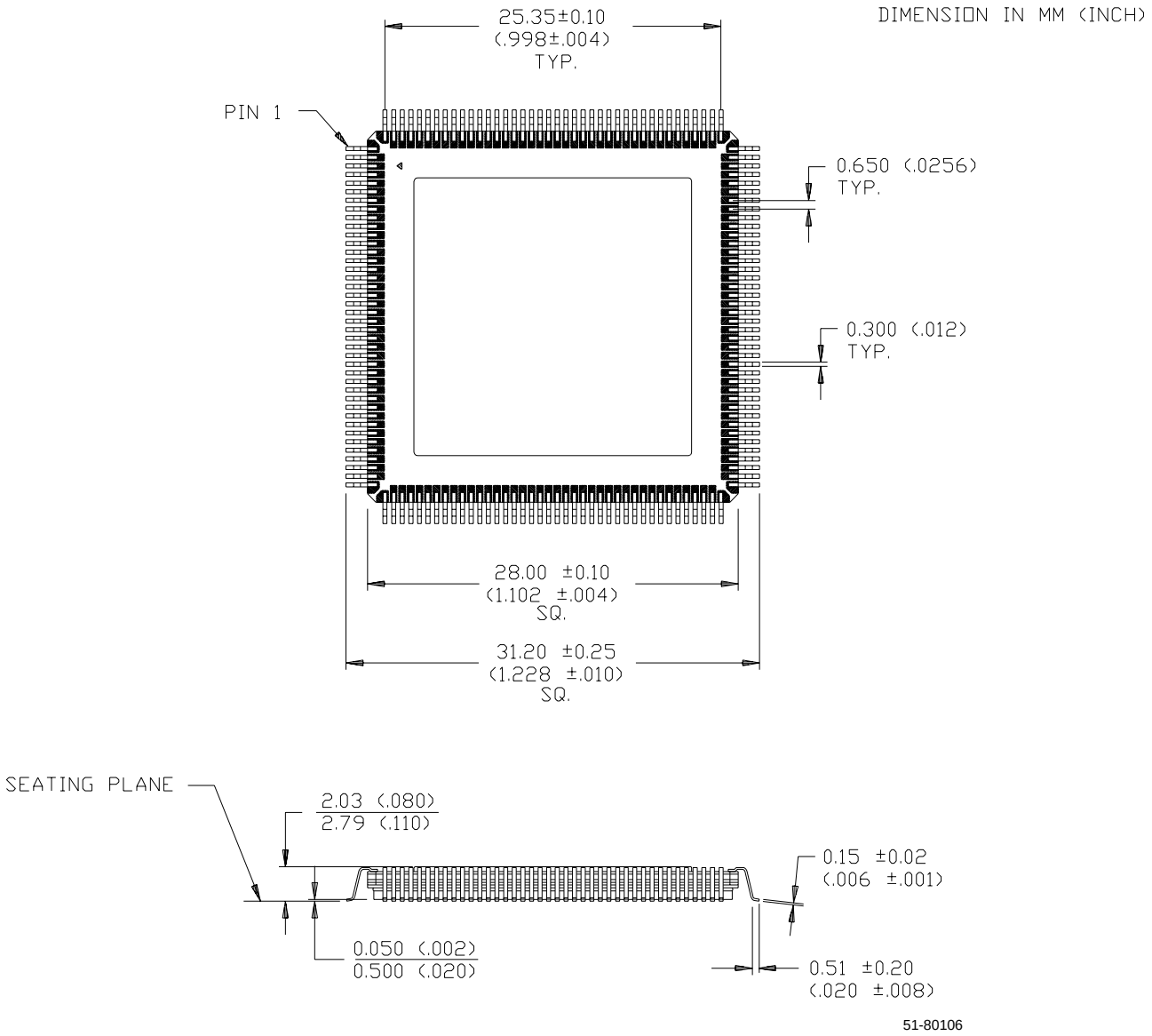
Package Diagrams (continued)

160-Pin Thin Plastic Quad Flat Pack (TQFP) A160



Package Diagrams (continued)

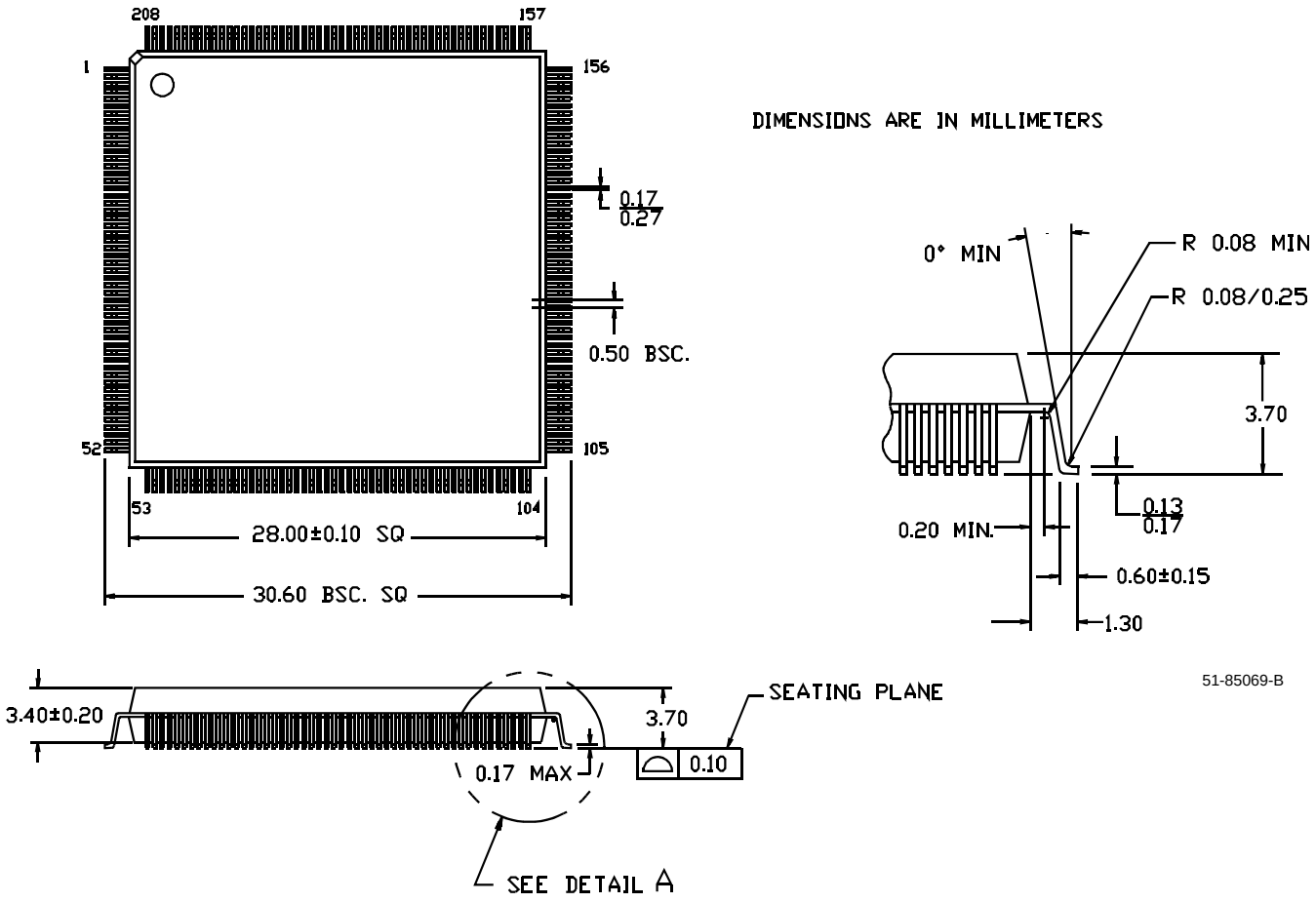
160-Lead Ceramic Quad Flatpack (Cavity Up) U162



51-80106

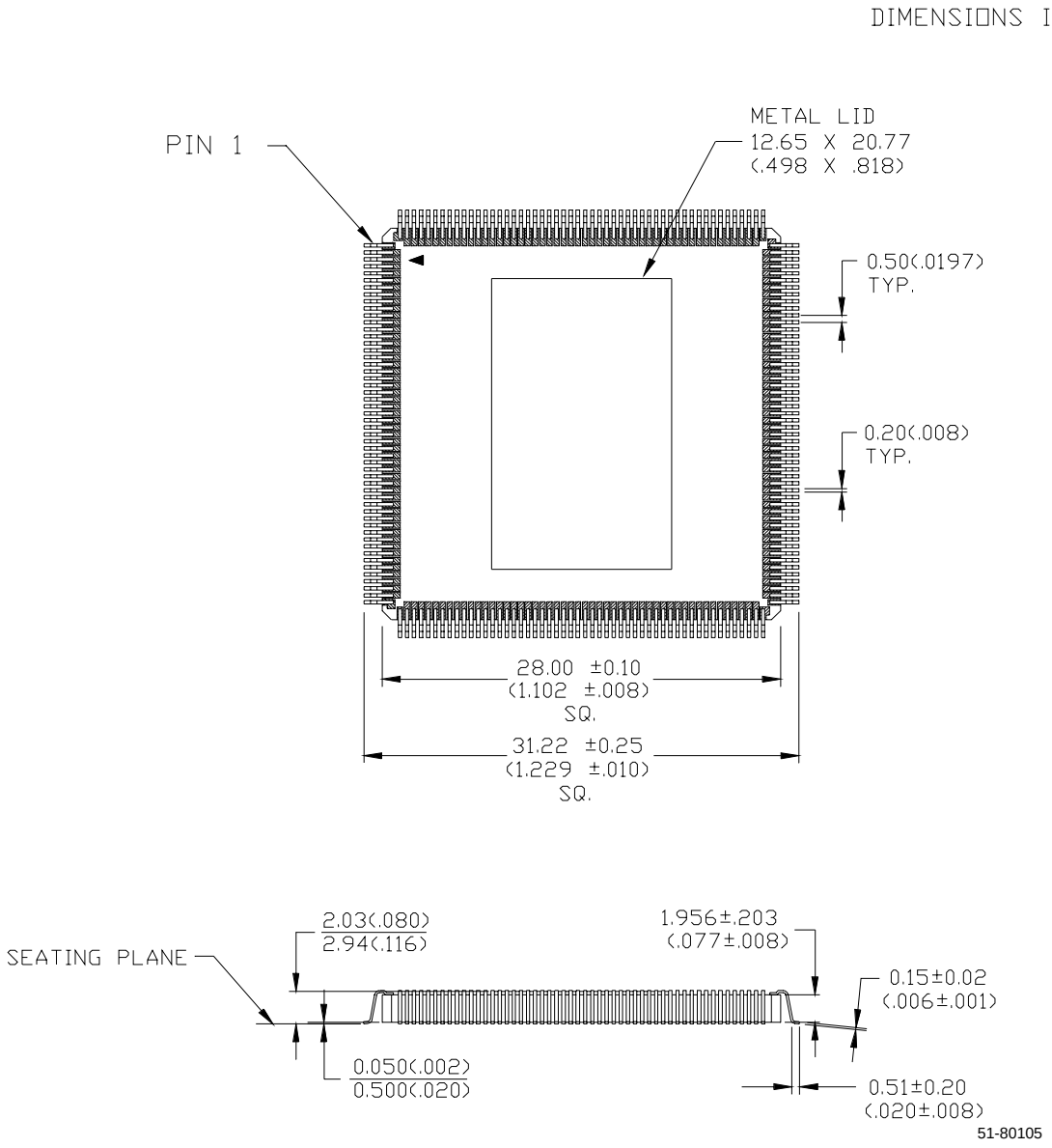
Package Diagrams (continued)

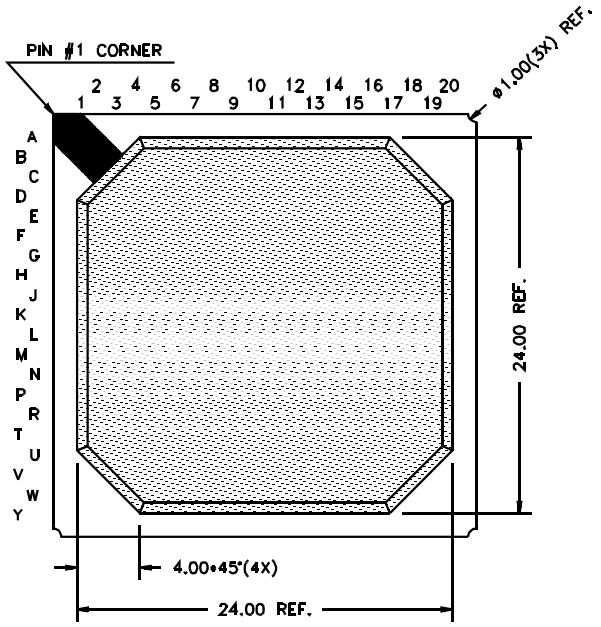
208-Lead Plastic Quad Flatpack N208

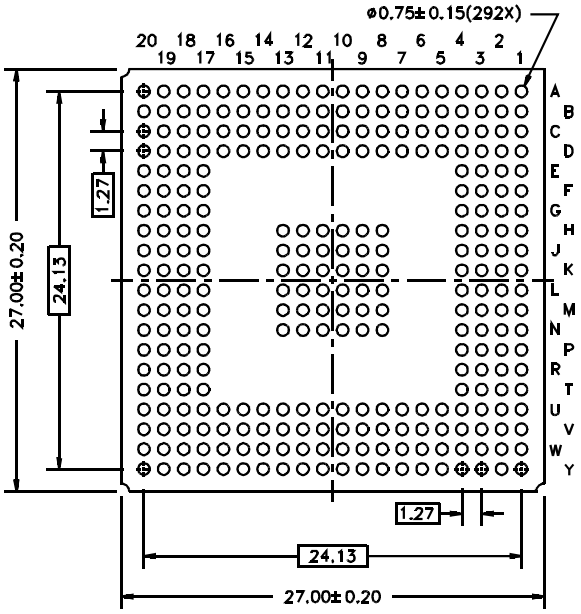


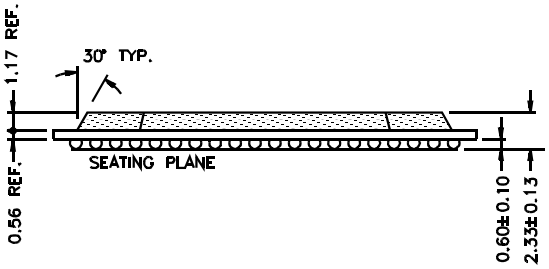
Package Diagrams (continued)

208-Lead Ceramic Quad Flatpack (Cavity Up) U208

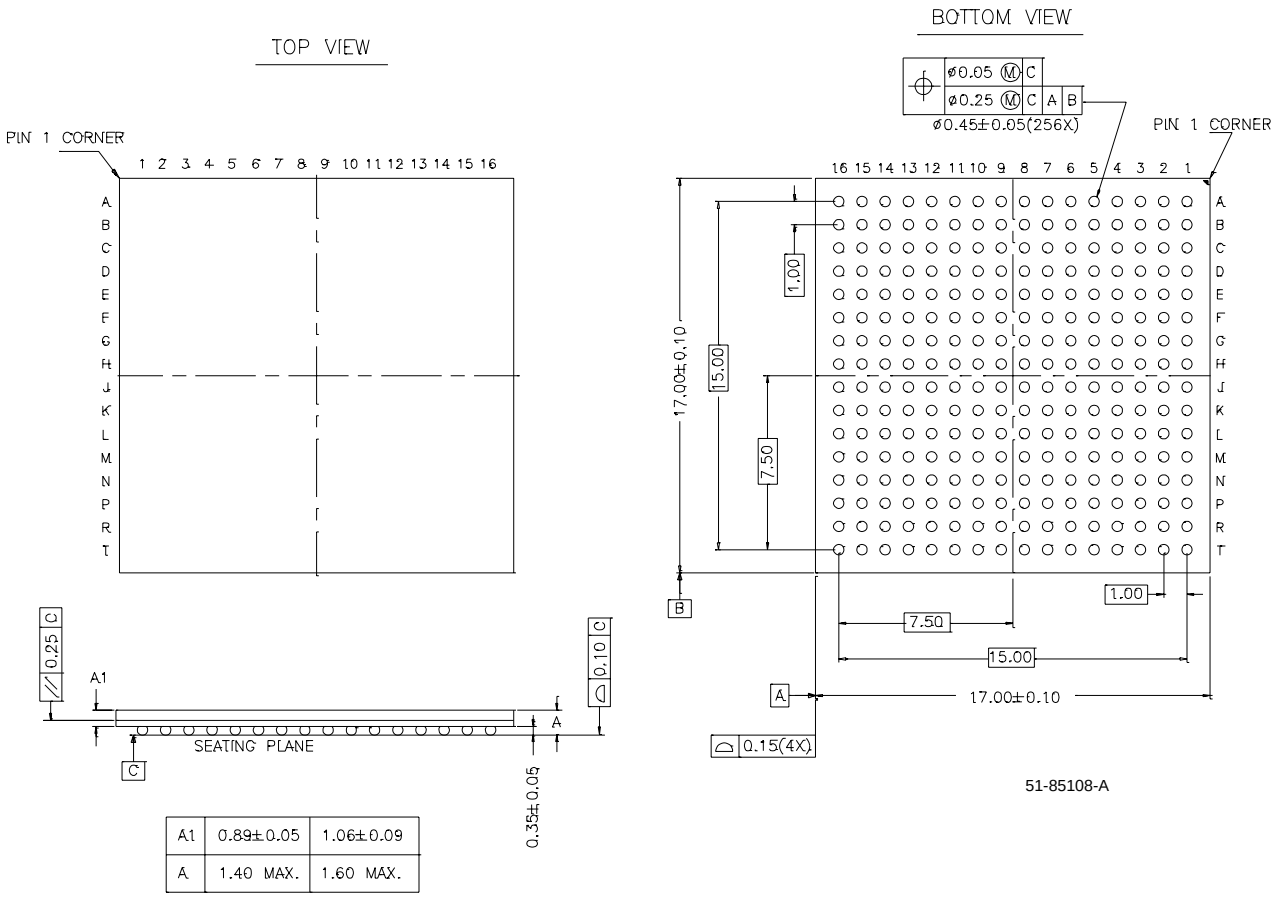



PIN #1 CORNER
ø1.00(3X) REF.
24.00 REF.
4.00•45°(4X)
24.00 REF.


ø0.75±0.15(292X)
1.27
24.13
27.00±0.20
1.27
24.13
27.00±0.20

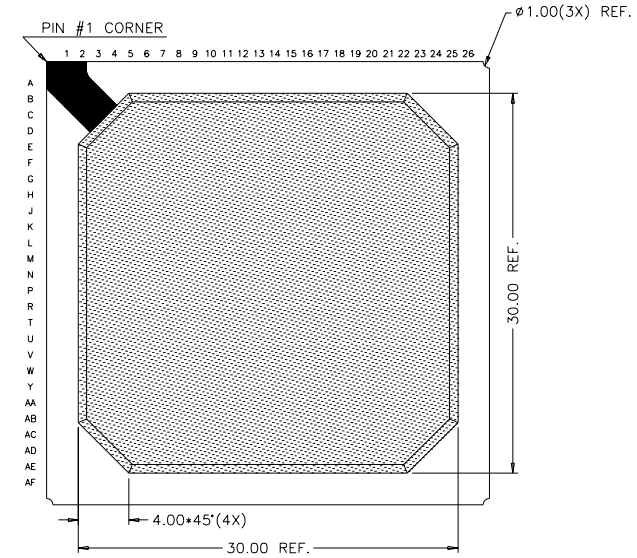

1.17 REF.
30° TYP.
SEATING PLANE
0.56 REF.
0.60±0.10
2.33±0.13

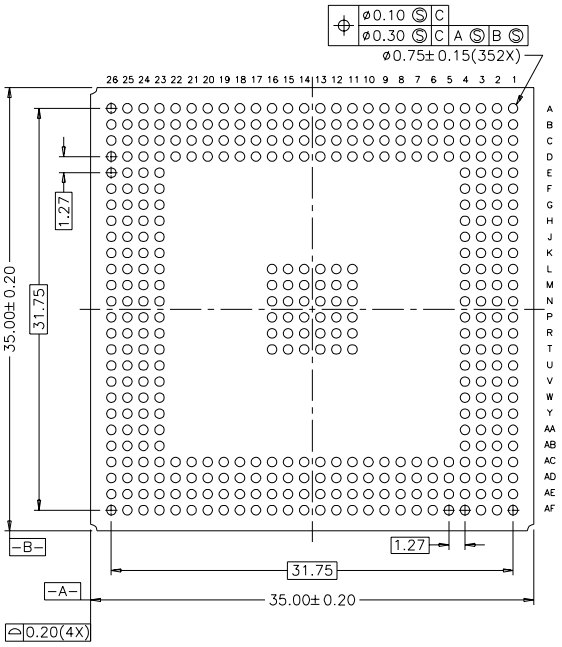
51-85097

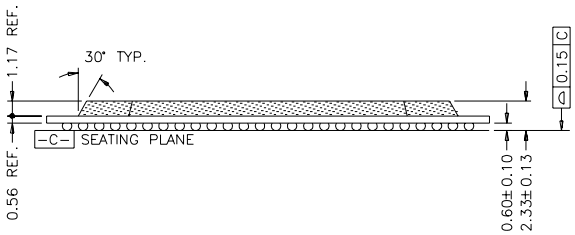


A1	0.89±0.05	1.06±0.09
A	1.40 MAX.	1.60 MAX.

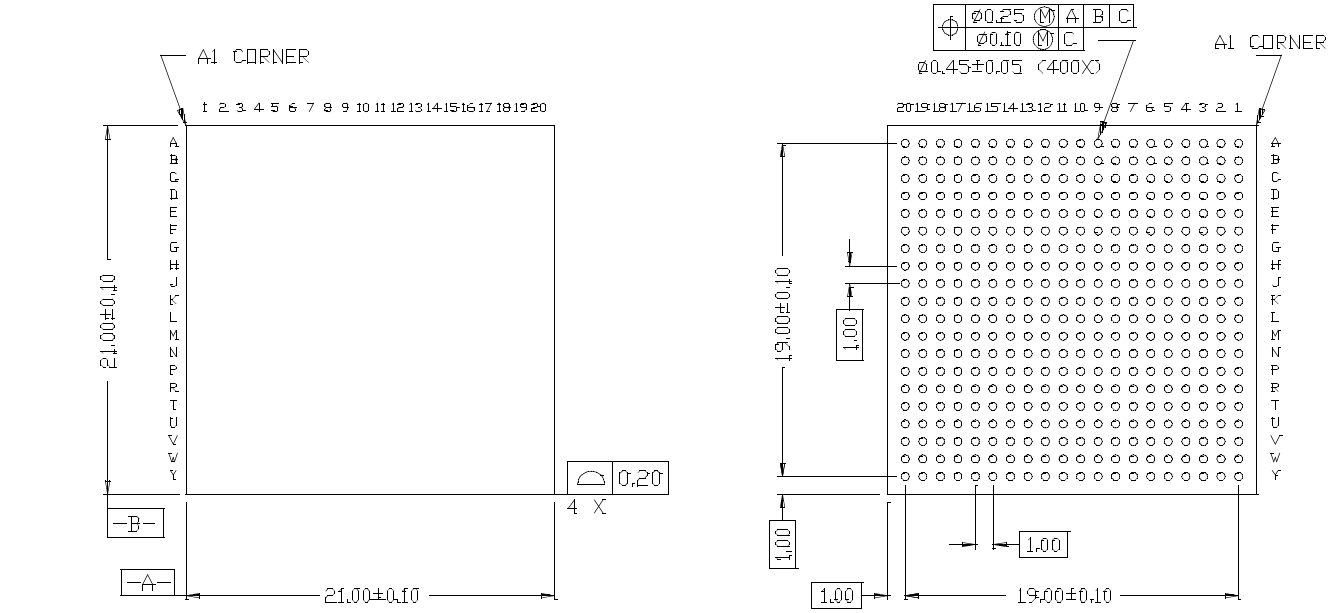
51-85108-A


PIN #1 CORNER
ø1.00(3X) REF.
30.00 REF.
4.00*45°(4X)
30.00 REF.


ø0.10 Ⓢ C
ø0.30 Ⓢ C A Ⓢ B Ⓢ
ø0.75± 0.15(352X)
1.27
31.75
35.00± 0.20
-B-
-A-
1.27
31.75
35.00± 0.20
0.20(4X)

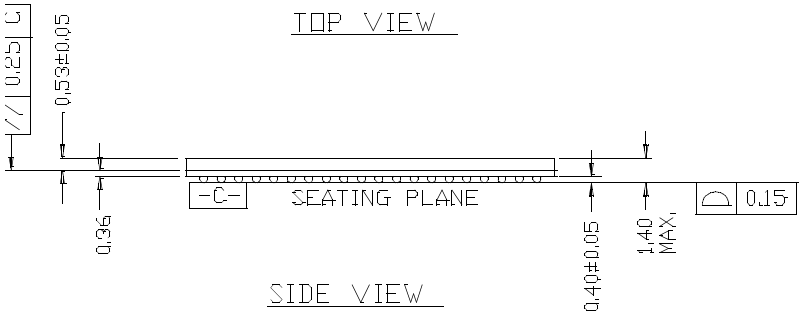

1.17 REF.
30° TYP.
0.15 C
-C- SEATING PLANE
0.56 REF.
0.60± 0.10
2.33± 0.13

51-85103



TOP VIEW

BOTTOM VIEW



SIDE VIEW

51-85111-A

**	106272	04/18/01	SZV	Change from Spec number: 38-00475 to 38-03007

4.8 MAX4131

19-1089; Rev 2; 8/97

MAXIM

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

General Description

The MAX4130–MAX4134 family of operational amplifiers combines 10MHz gain-bandwidth product and excellent DC accuracy with rail-to-rail operation at the inputs and outputs. These devices require only 900µA per amplifier, and operate from either a single supply (+2.7V to +6.5V) or dual supplies (±1.35V to ±3.25V) with a common-mode voltage range that extends 250mV beyond V_{EE} and V_{CC}. They are capable of driving 250Ω loads and are unity-gain stable. In addition, the MAX4131/MAX4133 feature a shutdown mode in which the outputs are placed in a high-impedance state and the supply current is reduced to only 25µA per amplifier.

With their rail-to-rail input common-mode range and output swing, the MAX4130–MAX4134 are ideal for low-voltage, single-supply operation. Although the minimum operating voltage is specified at 2.7V, the devices typically operate down to 1.8V. In addition, low offset voltage and high speed make them the ideal signal-conditioning stages for precision, low-voltage data-acquisition systems. **The MAX4130 comes in the space-saving SOT23-5 package.**

Selection Table

PART	AMPS PER PACKAGE	SHUTDOWN MODE	PIN-PACKAGE
MAX4130	1	—	5 SOT23-5
MAX4131	1	Yes	8 SO/µMAX
MAX4132	2	—	8 SO/µMAX
MAX4133	2	Yes	14 SO
MAX4134	4	—	14 SO

Applications

Battery-Powered Instruments

Portable Equipment

Data-Acquisition Systems

Signal Conditioning

Low-Power, Low-Voltage Applications

Pin Configurations appear at end of data sheet.

Features

- **5-Pin SOT23-5 Package (MAX4130)**
- **+2.7V to +6.5V Single-Supply Operation**
- **Rail-to-Rail Input Common-Mode Voltage Range**
- **Rail-to-Rail Output Voltage Swing**
- **10MHz Gain-Bandwidth Product**
- **900µA Quiescent Current per Amplifier**
- **25µA Shutdown Function (MAX4131/MAX4133)**
- **200µV Offset Voltage**
- **No Phase Reversal for Overdriven Inputs**
- **Drive 250Ω Loads**
- **Stable with 160pF Capacitive Loads**
- **Unity-Gain Stable**

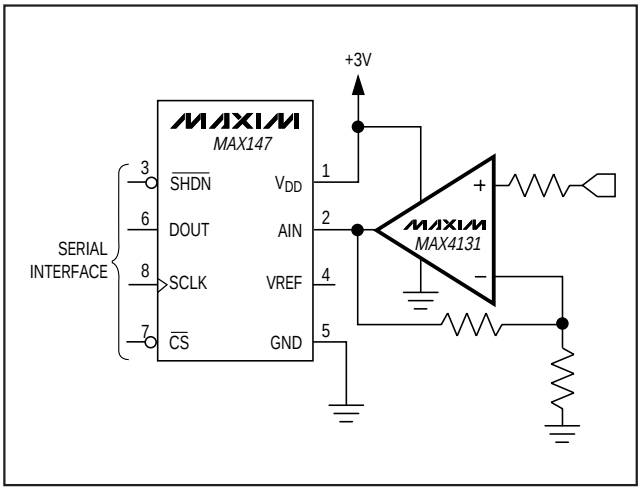
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4130EUK	-40°C to +85°C	5 SOT23-5	AABB
MAX4131C/D	0°C to +70°C	Dice*	—
MAX4131ESA	-40°C to +85°C	8 SO	—
MAX4131EUA	-40°C to +85°C	8 µMAX	—

Ordering Information continued at end of data sheet.

**Dice are specified at T_A = +25°C, DC parameters only.*

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}-V_{EE}).....7.5V
IN+, IN-, $\overline{SHDN}$ Voltage .....(V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Output Short-Circuit Duration (Note 1).....Continuous
(short to either supply)
Continuous Power Dissipation (T_A = +70°C)
5-pin SOT23-5 (derate 7.1mW/°C above +70°C) 571mW
8-pin SO (derate 5.88mW/°C above +70°C).....471mW
8-pin µMAX (derate 4.10mW/°C above +70°C) 330mW
14-pin SO (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Range
MAX413_E__ .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Provided that the maximum package power-dissipation rating is met.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = V_{CC} / 2, R_L tied to V_{CC} / 2, $\overline{SHDN}$ ≥ 2V (or open), **T_A = +25°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{CM} = V_{EE} to V_{CC}	MAX4130EUK		±0.35	±1.50	mV
		MAX4131ESA		±0.20	±0.60	
		MAX4131EUA		±0.35	±1.20	
		MAX4132ESA/MAX4133ESD		±0.25	±0.75	
		MAX4132EUA		±0.40	±1.50	
		MAX4134ESD		±0.35	±1.50	
Input Bias Current	V_{CM} = V_{EE} to V_{CC}			±50	±150	nA
Input Offset Current	V_{CM} = V_{EE} to V_{CC}			±1	±12	nA
Differential Input Resistance	-1.5V < V_{DIFF} < 1.5V			500		kΩ
Common-Mode Input Voltage Range			V_{EE} - 0.25		V_{CC} + 0.25	V
Common-Mode Rejection Ratio	(V_{EE} - 0.25V) < V_{CM} < (V_{CC} + 0.25V)	MAX4130EUK	67	90		dB
		MAX4131ESA	78	98		
		MAX4131EUA	68	88		
		MAX4132ESA/MAX4133ESD	74	94		
		MAX4132EUA	66	86		
		MAX4134ESD	64	84		
Power-Supply Rejection Ratio	V_{CC} = 2.7V to 6.5V		78	100		dB
Output Resistance	A_V = 1			0.1		Ω
Off-Leakage Current	$\overline{SHDN}$ < 0.8V, V_{OUT} = 0V to V_{CC}			±0.1	±1	µA
Large-Signal Voltage Gain	V_{CC} = 2.7V	V_{OUT} = 0.25V to 2.45V, R_L = 100kΩ	92	108		dB
		V_{OUT} = 0.4V to 2.3V, R_L = 250Ω	72	82		
	V_{CC} = 5V	V_{OUT} = 0.25V to 4.75V, R_L = 100kΩ	94	108		
		V_{OUT} = 0.4V to 4.6V, R_L = 250Ω	75	86		

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = V_{CC} / 2, R_L tied to V_{CC} / 2, $\overline{SHDN}$ ≥ 2V (or open), **T_A = +25°C**, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Output Voltage Swing	MAX4130/ MAX4131	R_L = 100kΩ	V_{CC} - V_{OH}		12	20	mV
			V_{OL} - V_{EE}		20	35	
		R_L = 250Ω	V_{CC} - V_{OH}		240	290	
			V_{OL} - V_{EE}		125	170	
	MAX4132/ MAX4133/ MAX4134	R_L = 100kΩ	V_{CC} - V_{OH}		15	30	
			V_{OL} - V_{EE}		25	40	
		R_L = 250Ω	V_{CC} - V_{OH}		280	330	
			V_{OL} - V_{EE}		180	230	
Output Short-Circuit Current					50		mA
$\overline{SHDN}$ Logic Threshold	MAX4131–MAX4134		Low			0.8	V
			High	2.0			
$\overline{SHDN}$ Input Current	MAX4131–MAX4134				±1	±3	µA
Operating Supply-Voltage Range				2.7		6.5	V
Supply Current per Amplifier	V_{CM} = V_{OUT} = V_{CC} / 2		V_{CC} = 2.7V		900	1050	µA
			V_{CC} = 5V		1000	1150	
Shutdown Supply Current per Amplifier	$\overline{SHDN}$ > 0.8V, MAX4131–MAX4134		V_{CC} = 2.7V		25	40	µA
			V_{CC} = 5V		40	60	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = V_{CC} / 2, R_L tied to V_{CC} / 2, $\overline{SHDN}$ ≥ 2V (or open), **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{CM} = V_{EE} to V_{CC}	MAX4130EUK			±3.50	mV
		MAX4131ESA			±0.75	
		MAX4131EUA			±4.40	
		MAX4132ESA/MAX4133ESD			±0.95	
		MAX4132EUA			±4.70	
		MAX4134ESD			±4.00	
Input Offset Voltage Tempco				±2		µV/°C
Input Bias Current	V_{CM} = V_{EE} to V_{CC}				±160	nA
Input Offset Current	V_{CM} = V_{EE} to V_{CC}				±18	nA
Common-Mode Input Voltage Range			V_{EE} - 0.20		V_{CC} + 0.20	V
Common-Mode Rejection Ratio	(V_{EE} - 0.2V) < V_{CM} < (V_{CC} + 0.2V)	MAX4130EUK	62			dB
		MAX4131ESA	76			
		MAX4131EUA	60			
		MAX4132ESA/MAX4133ESD	74			
		MAX4132EUA	58			
		MAX4134ESD	60			

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = V_{CC} / 2, R_L tied to V_{CC} / 2, $\overline{SHDN}$ ≥ 2V (or open), **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	V_{CC} = 2.7V to 6.5V			74			dB
Off-Leakage Current	$\overline{SHDN}$ < 0.8V, V_{OUT} = 0V to V_{CC}					±12	µA
Large-Signal Voltage Gain	V_{CC} = 2.7V	V_{OUT} = 0.25V to 2.45V, R_L = 100kΩ		84			dB
		V_{OUT} = 0.4V to 2.3V, R_L = 250Ω		66			
	V_{CC} = 5V	V_{OUT} = 0.25V to 4.75V, R_L = 100kΩ		86			
		V_{OUT} = 0.4V to 4.6V, R_L = 250Ω		68			
Output Voltage Swing	MAX4130/ MAX4131	R_L = 100kΩ	V_{CC} - V_{OH}			25	mV
			V_{OL} - V_{EE}			40	
		R_L = 250Ω	V_{CC} - V_{OH}			300	
			V_{OL} - V_{EE}			190	
	MAX4132/ MAX4133/ MAX4134	R_L = 100kΩ	V_{CC} - V_{OH}			35	
			V_{OL} - V_{EE}			50	
		R_L = 250Ω	V_{CC} - V_{OH}			350	
			V_{OL} - V_{EE}			250	
$\overline{SHDN}$ Logic Threshold	MAX4131–MAX4134		Low			0.8	V
			High	2.0			
$\overline{SHDN}$ Input Current	MAX4131–MAX4134					±3	µA
Operating Supply-Voltage Range				2.7		6.5	V
Supply Current per Amplifier	V_{CM} = V_{OUT} = V_{CC} / 2		V_{CC} = 2.7V			1100	µA
			V_{CC} = 5V			1200	
Shutdown Supply Current per Amplifier	$\overline{SHDN}$ < 0.8V, MAX4131–MAX4134		V_{CC} = 2.7V			50	µA
			V_{CC} = 5V			70	

AC ELECTRICAL CHARACTERISTICS

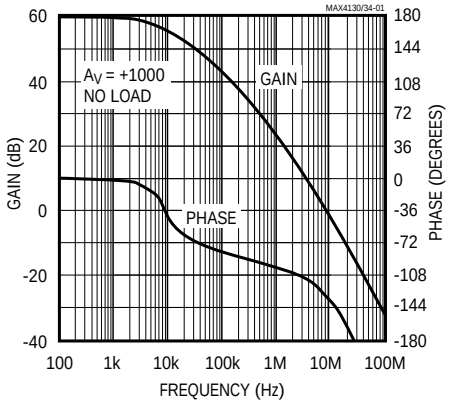
(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, $\overline{SHDN}$ ≥ 2V (or open), **T_A = +25°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gain-Bandwidth Product				10		MHz
Phase Margin				62		degrees
Gain Margin				12		dB
Total Harmonic Distortion	f = 10kHz, V_{OUT} = 2Vp-p (A_V = 1)			0.003		%
Slew Rate				4		V/µs
Settling Time to 0.01%	A_V = 1, V_{OUT} = 2V step			2.0		µs
Turn-On Time	V_{CC} = 0V to 3V step, V_{OUT} = V_{CC} / 2			1		µs
$\overline{SHDN}$ Delay	MAX4131–MAX4134, V_{CC} = 3V, V_{OUT} = V_{CC} / 2	Enable		1		µs
		Disable		0.2		
Input Capacitance				3		pF
Input Noise Voltage Density	f = 1kHz			22		nV/√Hz
Input Noise Current Density	f = 1kHz			0.4		pA/√Hz
Capacitive Load Stability	A_V = 1			160		pF

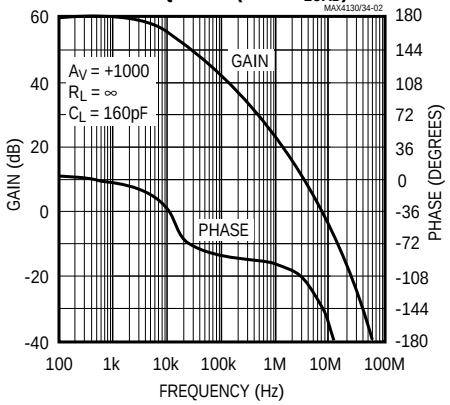
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

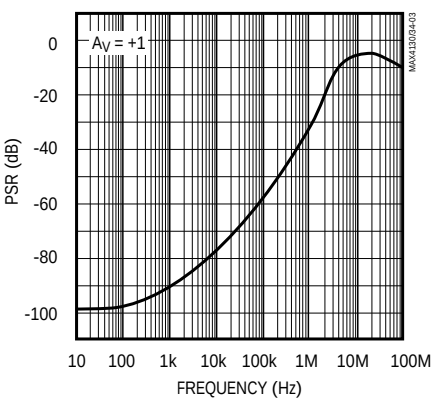
GAIN AND PHASE vs. FREQUENCY



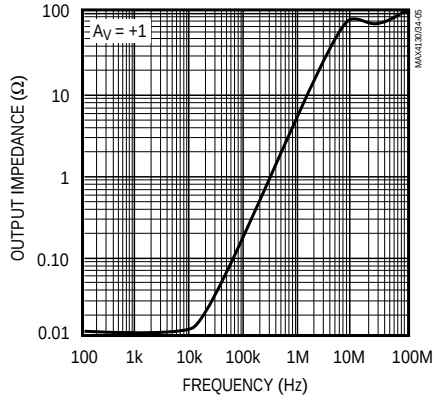
GAIN AND PHASE vs. FREQUENCY (WITH C_{LOAD})



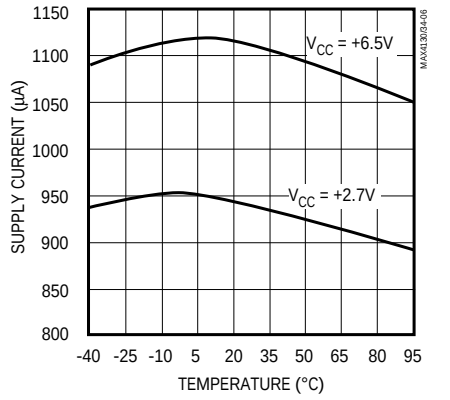
POWER-SUPPLY REJECTION vs. FREQUENCY



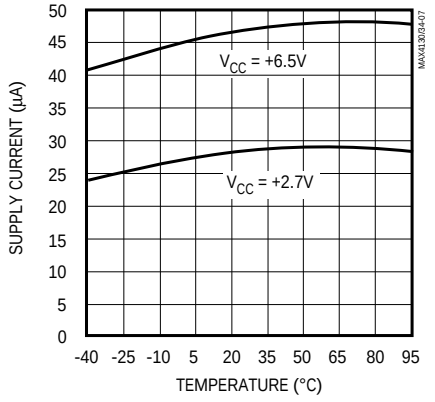
OUTPUT IMPEDANCE vs. FREQUENCY



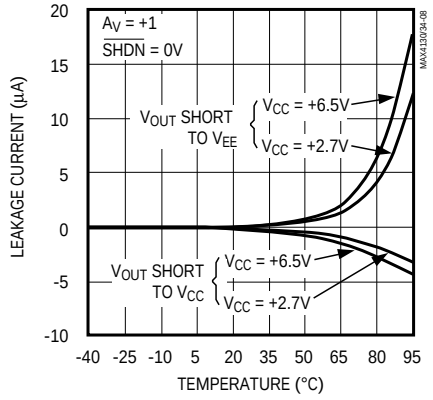
SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE



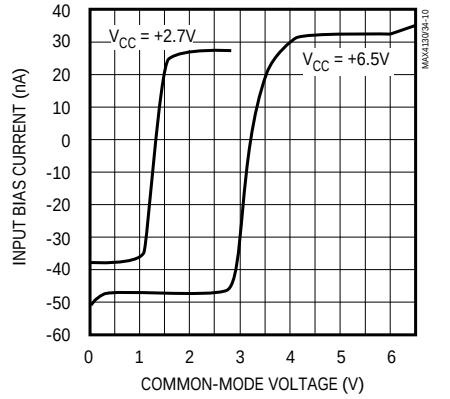
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



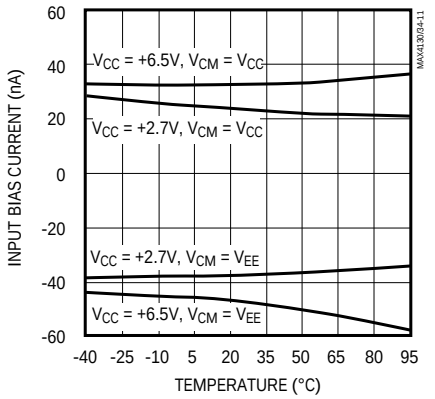
OUTPUT LEAKAGE CURRENT vs. TEMPERATURE



INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



INPUT BIAS CURRENT vs. TEMPERATURE

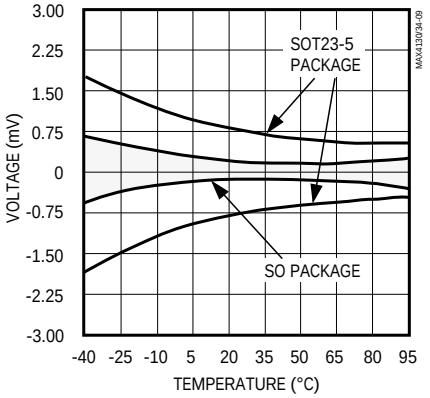


Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

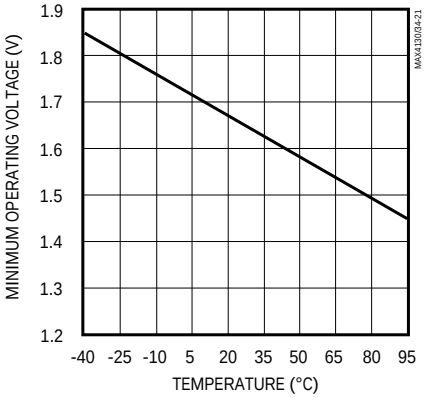
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

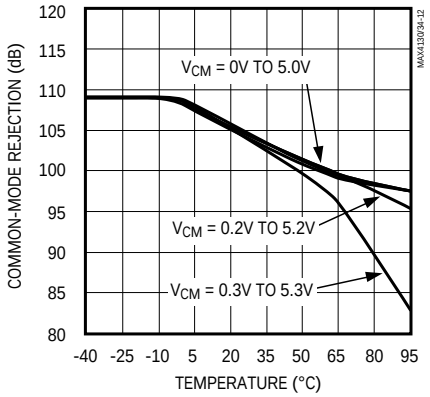
INPUT OFFSET VOLTAGE vs. TEMPERATURE



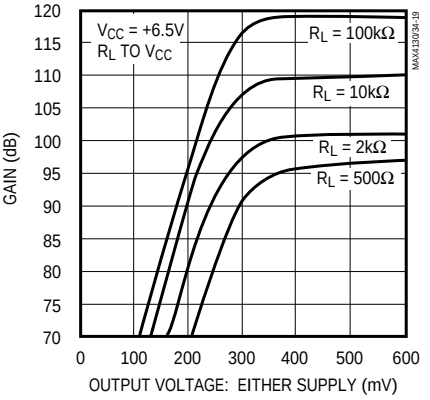
MINIMUM OPERATING VOLTAGE vs. TEMPERATURE



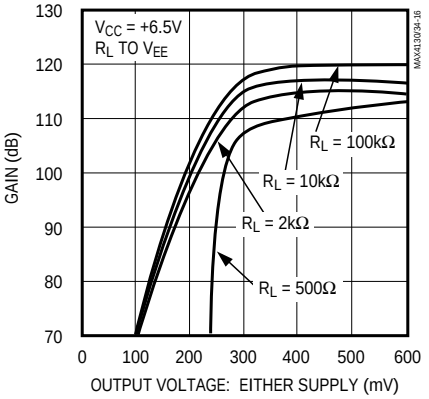
COMMON-MODE REJECTION vs. TEMPERATURE



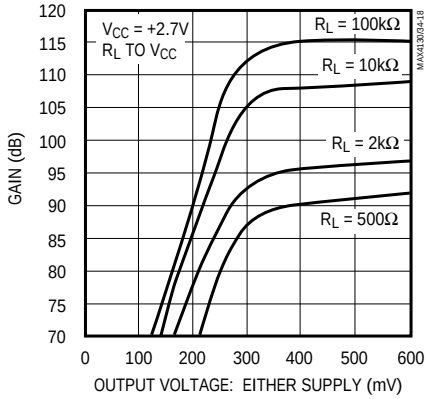
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



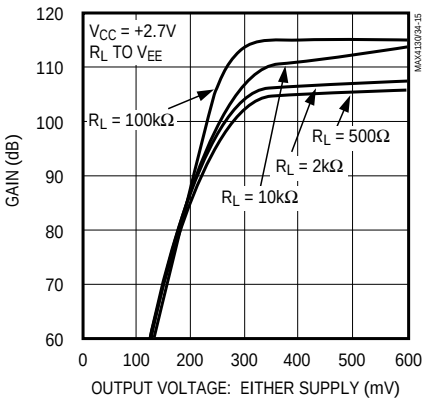
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



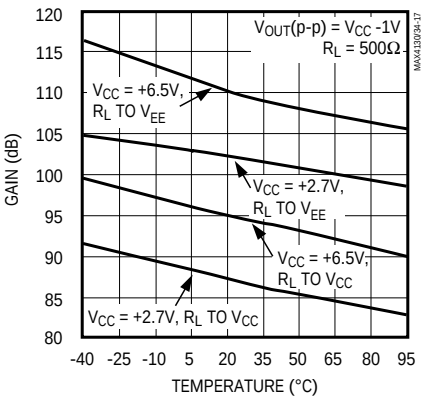
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



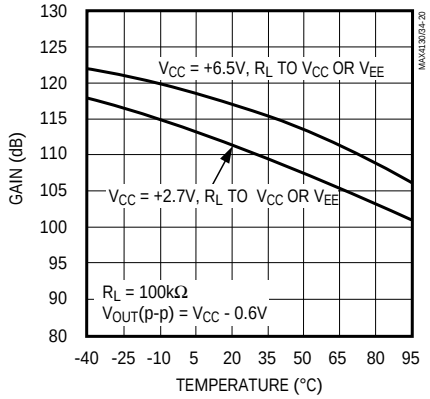
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



LARGE-SIGNAL GAIN vs. TEMPERATURE



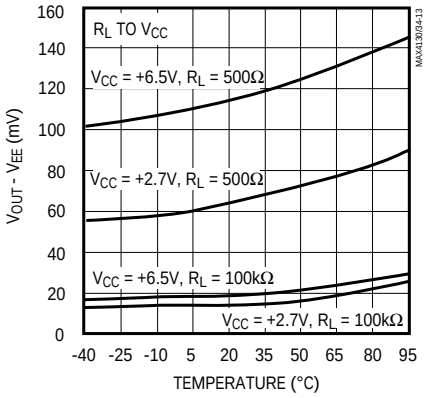
LARGE-SIGNAL GAIN vs. TEMPERATURE



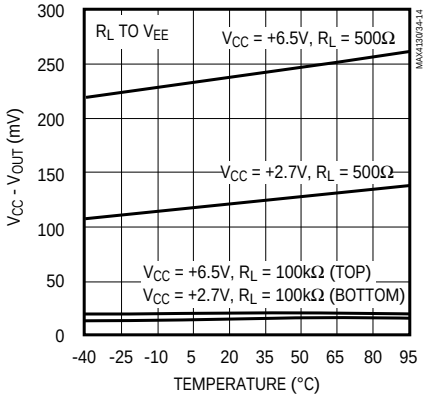
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

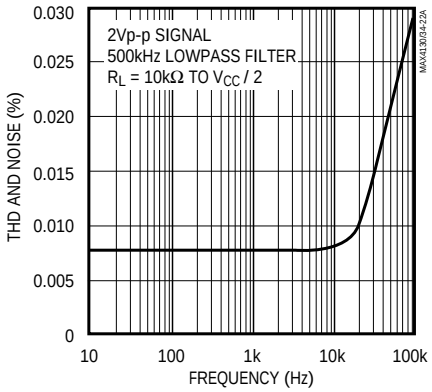
MINIMUM OUTPUT VOLTAGE vs. TEMPERATURE



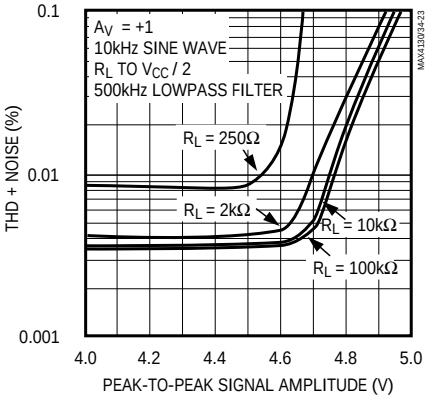
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE



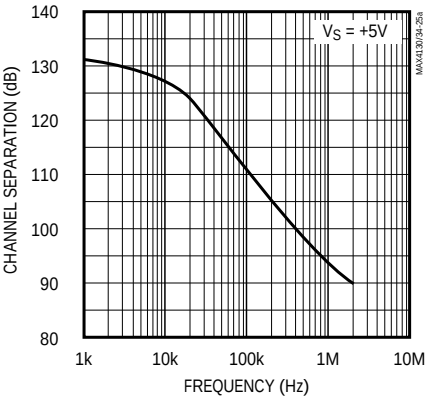
TOTAL HARMONIC DISTORTION AND NOISE vs. FREQUENCY



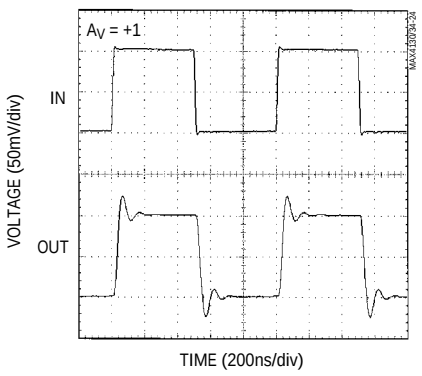
TOTAL HARMONIC DISTORTION AND NOISE vs. PEAK-TO-PEAK SIGNAL AMPLITUDE



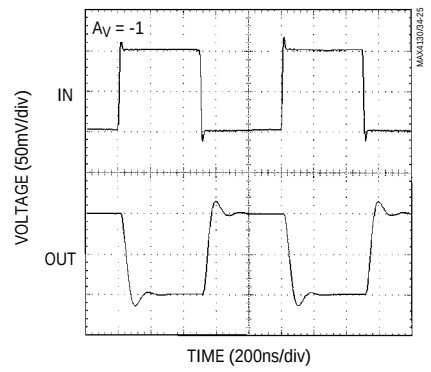
CHANNEL SEPARATION vs. FREQUENCY



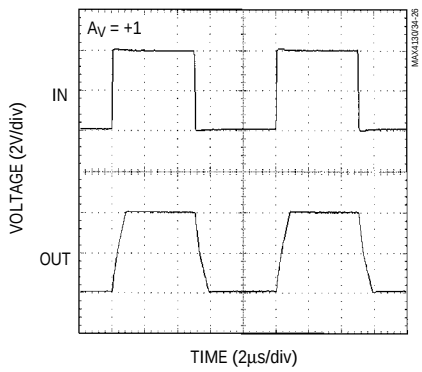
MAX4131 SMALL-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



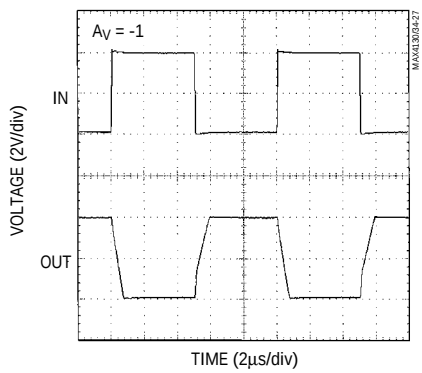
MAX4131 SMALL-SIGNAL TRANSIENT RESPONSE (INVERTING)



MAX4131 LARGE-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



MAX4131 LARGE-SIGNAL TRANSIENT RESPONSE (INVERTING)



Pin Description

MAX4130	MAX4131	MAX4132	MAX4133	MAX4134	NAME	FUNCTION
1	6	—	—	—	OUT	Output
2	4	4	4	11	V_{EE}	Negative Supply. Ground for single-supply operation.
3	3	—	—	—	IN+	Noninverting Input
4	2	—	—	—	IN-	Inverting Input
5	7	8	14	4	V_{CC}	Positive Supply
—	1, 5	—	5, 7, 8, 10	—	N.C.	No Connect. Not internally connected.
—	8	—	—	—	$\overline{SHDN}$	Shutdown Control. Tie high or leave floating to enable amplifier.
—	—	1, 7	1, 13	1, 7	OUT1, OUT2	Outputs for amps 1 and 2
—	—	2, 6	2, 12	2, 6	IN1-, IN2-	Inverting Inputs for amps 1 and 2
—	—	3, 5	3, 11	3, 5	IN1+, IN2+	Noninverting Inputs for amps 1 and 2
—	—	—	6, 9	—	$\overline{SHDN1}$, $\overline{SHDN2}$	Shutdown Control, independent for amps 1 and 2. Tie high or leave floating to enable amplifier.
—	—	—	—	8, 14	OUT3, OUT4	Outputs for amps 3 and 4
—	—	—	—	9, 13	IN3-, IN4-	Inverting Inputs for amps 3 and 4
—	—	—	—	10, 12	IN3+, IN4+	Noninverting Inputs for amps 3 and 4

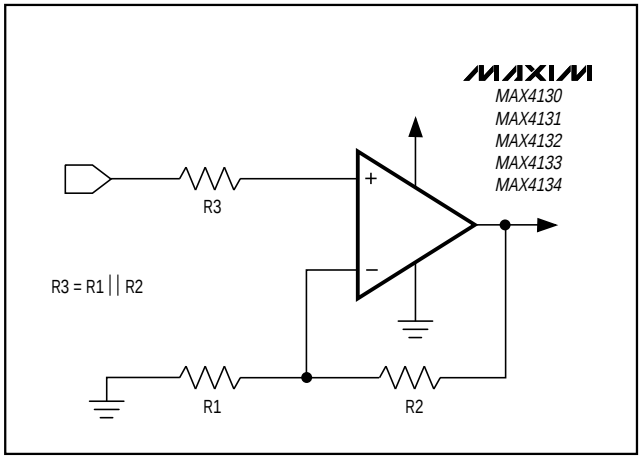


Figure 1a. Reducing Offset Error Due to Bias Current (Noninverting)

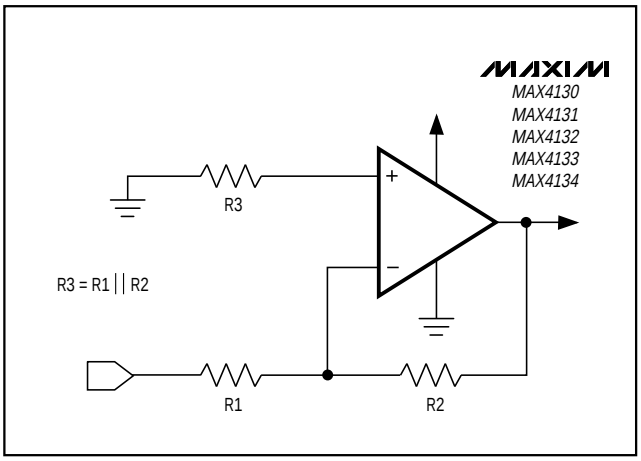


Figure 1b. Reducing Offset Error Due to Bias Current (Inverting)

Applications Information

Rail-to-Rail Input Stage

Devices in the MAX4130–MAX4134 family of high-speed amplifiers have rail-to-rail input and output stages designed for low-voltage, single-supply operation. The input stage consists of separate NPN and PNP differential stages that combine to provide an input common-mode range that extends 0.2V beyond the supply rails. The PNP stage is active for input voltages close to the negative rail, and the NPN stage is active for input voltages near the positive rail. The input offset voltage is typically below 200µV. The switchover transition region, which occurs near V_{CC} / 2, has been extended to minimize the slight degradation in common-mode rejection ratio caused by the mismatch of the input pairs. Their low offset voltage, high bandwidth, and rail-to-rail common-mode range make these op amps excellent choices for precision, low-voltage data-acquisition systems.

Since the input stage switches between the NPN and PNP pairs, the input bias current changes polarity as the input voltage passes through the transition region. Reduce the offset error caused by input bias currents flowing through external source impedances by matching the effective impedance seen by each input (Figures 1a, 1b). High source impedances, together with input capacitance, can create a parasitic pole that produces an underdamped signal response. Reducing the input impedance or placing a small (2pF to 10pF) capacitor across the feedback resistor improves response.

The MAX4130–MAX4134's inputs are protected from large differential input voltages by 1kΩ series resistors and back-to-back triple diodes across the inputs (Figure 2). For differential input voltages less than 1.8V, input resistance is typically 500kΩ. For differential input voltages greater than 1.8V, input resistance is approximately 2kΩ. The input bias current is given by the following equation:

$$I_{BIAS} = \frac{V_{DIFF} - 1.8V}{2k\Omega}$$

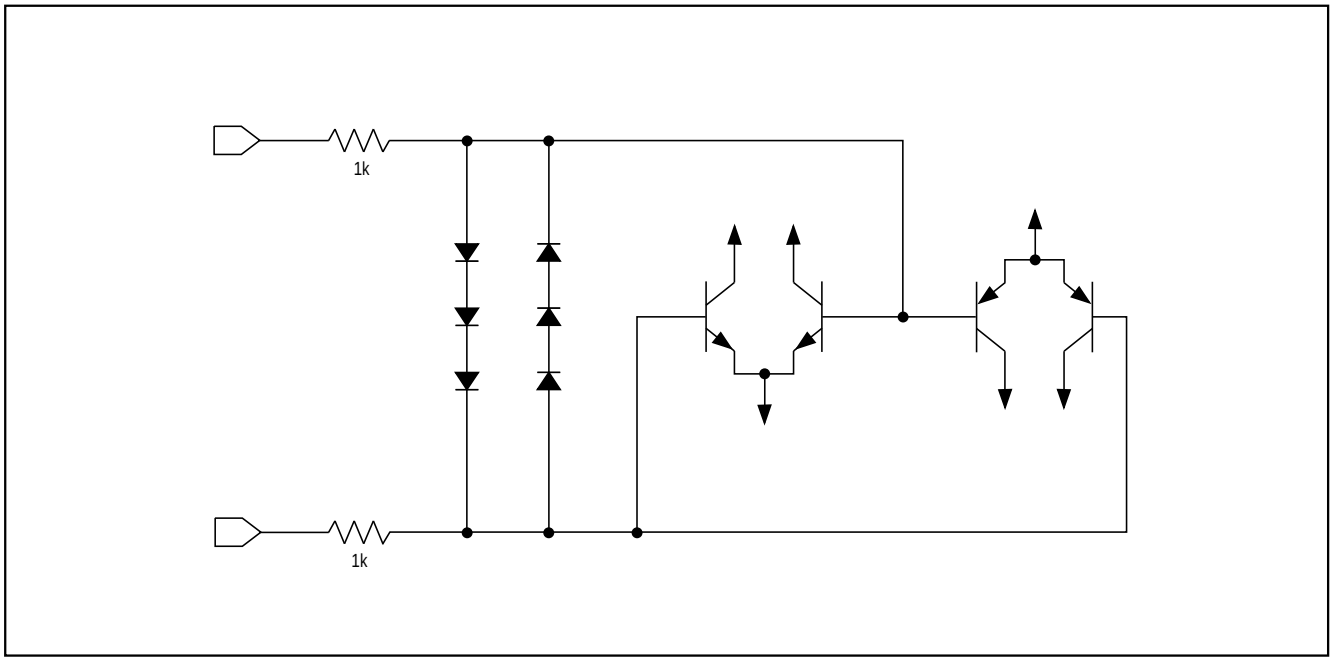


Figure 2. Input Protection Circuit

Rail-to-Rail Output Stage

The minimum output voltage is within millivolts of ground for single-supply operation where the load is referenced to ground (V_{EE}). Figure 3 shows the input voltage range and output voltage swing of a MAX4131 connected as a voltage follower. With a +3V supply and the load tied to ground, the output swings from 0.00V to 2.90V. The maximum output voltage swing depends on the load, but will be within 150mV of a +3V supply, even with the maximum load (500Ω to ground).

Driving a capacitive load can cause instability in most high-speed op amps, especially those with low quiescent current. The MAX4130–MAX4134 have a high tolerance for capacitive loads. They are stable with capacitive loads up to 160pF. Figure 4 gives the stable operating region for capacitive loads. Figures 5 and 6 show the response with capacitive loads and the results of adding an isolation resistor in series with the output (Figure 7). The resistor improves the circuit's phase margin by isolating the load capacitor from the op amp's output.

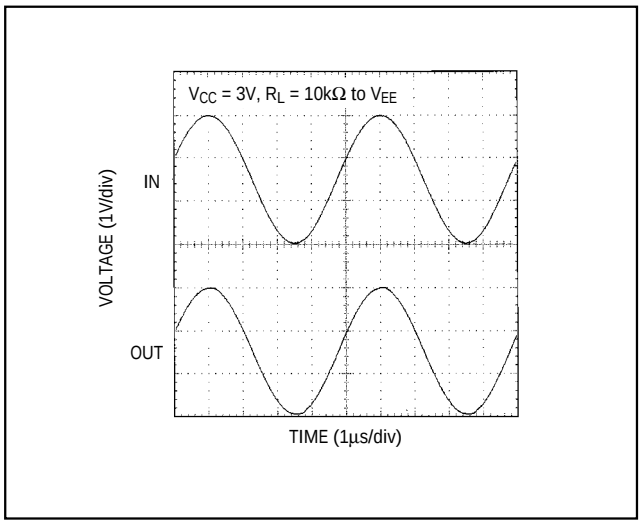


Figure 3. Rail-to-Rail Input/Output Voltage Range

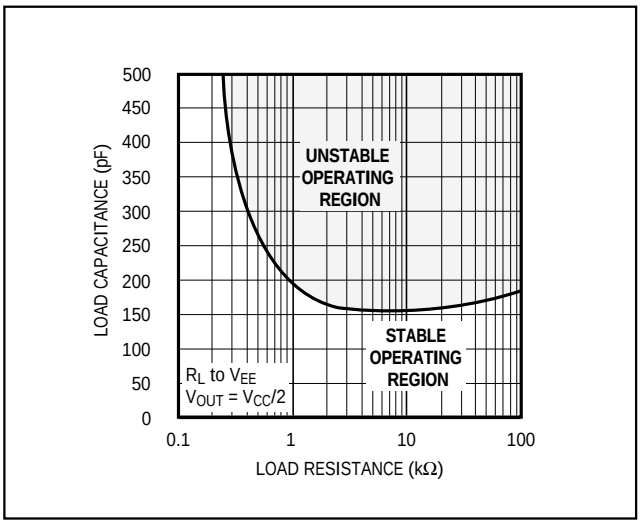


Figure 4. Capacitive-Load Stability

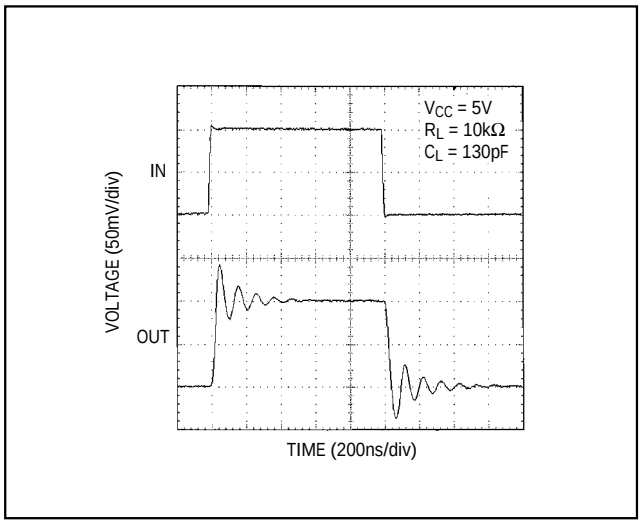


Figure 5. MAX4131 Small-Signal Transient Response with Capacitive Load

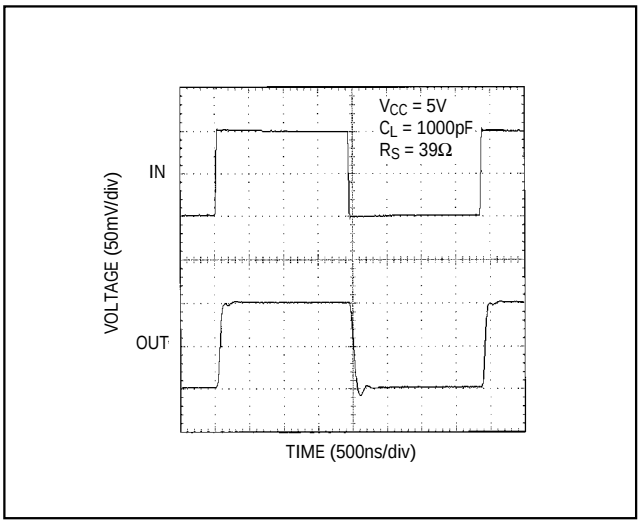


Figure 6. MAX4131 Transient Response to Capacitive Load with Isolation Resistor

Power-Up and Shutdown Mode

The MAX4130–MAX4134 amplifiers typically settle within 1µs after power-up. Figures 9 and 10 show the output voltage and supply current on power-up, using the test circuit of Figure 8.

The MAX4131 and MAX4133 have a shutdown option. When the shutdown pin ($\overline{SHDN}$) is pulled low, the supply current drops below 25µA per amplifier and the amplifiers are disabled with the outputs in a high-impedance state. Pulling $\overline{SHDN}$ high or leaving it floating enables the amplifier. In the dual-amplifier MAX4133, the shutdown functions operate independently. Figures 11 and 12 show the output voltage and supply current responses of the MAX4131 to a shutdown pulse, using the test circuit of Figure 8.

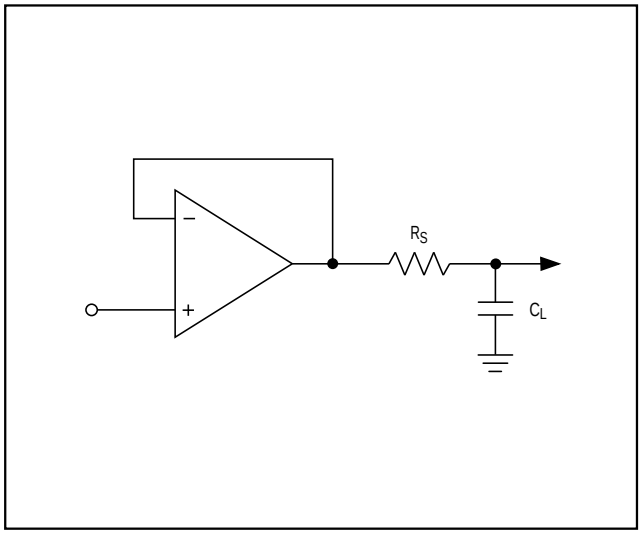


Figure 7. Capacitive-Load Driving Circuit

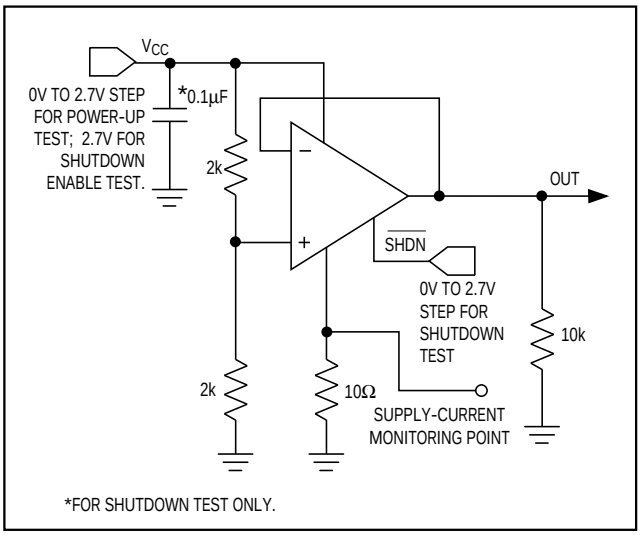


Figure 8. Power-Up/Shutdown Test Circuit

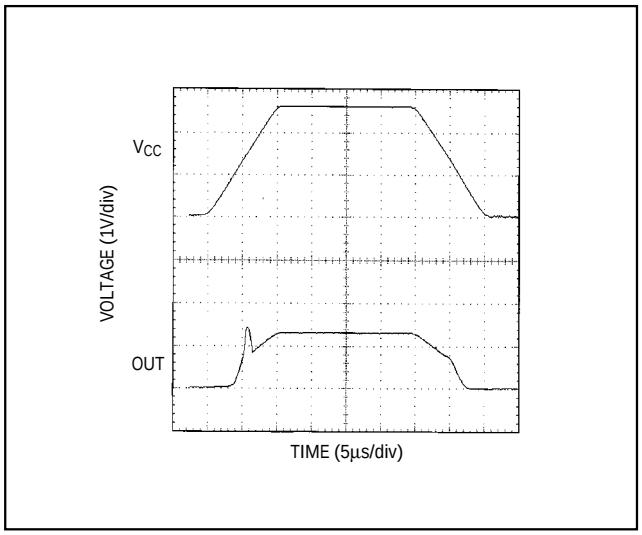


Figure 9. Power-Up Output Voltage

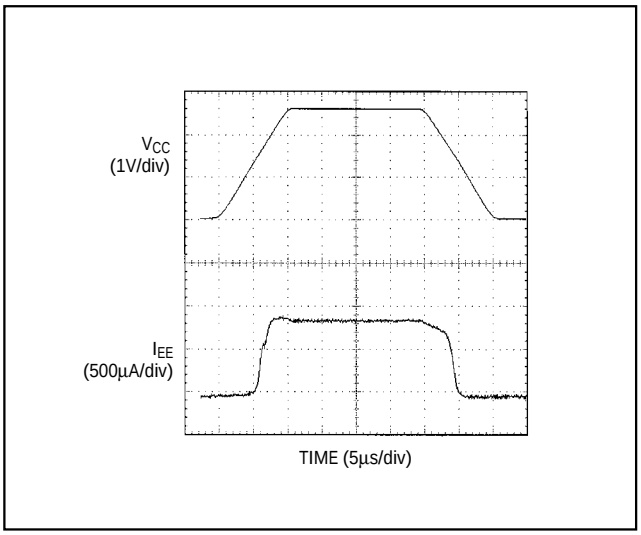


Figure 10. Power-Up Supply Current

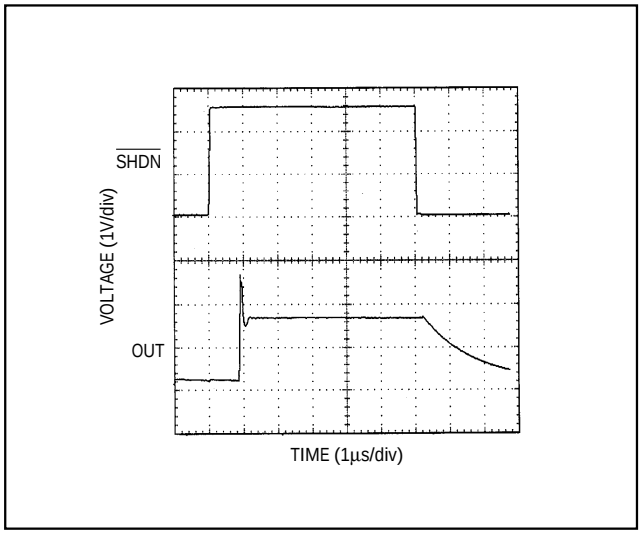


Figure 11. Shutdown Output Voltage

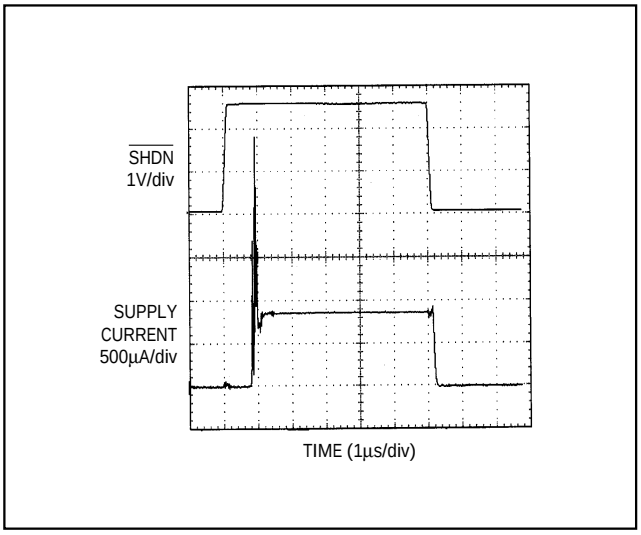


Figure 12. Shutdown Enable/Disable Supply Current

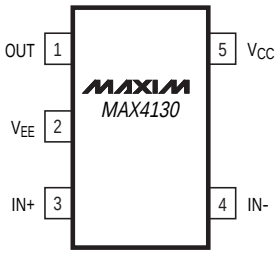
Power Supplies and Layout

The MAX4130–MAX4134 operate from a single +2.7V to +6.5V power supply, or from dual supplies of ±1.35V to ±3.25V. For single-supply operation, bypass the power supply with a 0.1µF ceramic capacitor in parallel with at least 1µF. For dual supplies, bypass each supply to ground.

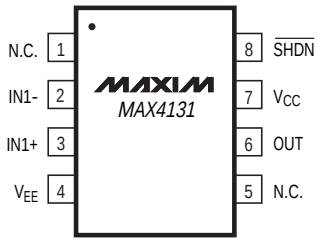
Good layout improves performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. Decrease stray capacitance by placing external components close to the op amp's pins, minimizing trace lengths and resistor leads.

Pin Configurations

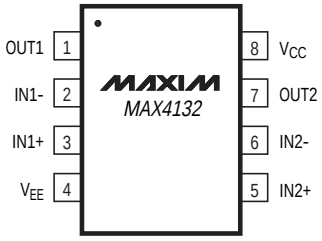
TOP VIEW



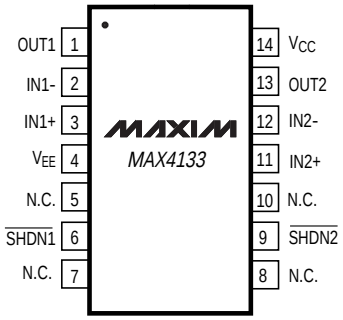
SOT23-5



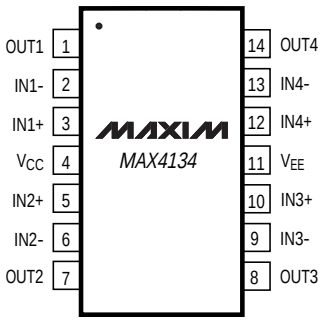
SO/μMAX



SO/μMAX



SO



SO

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4132ESA	-40°C to +85°C	8 SO	—
MAX4132EUA	-40°C to +85°C	8 µMAX	—
MAX4133C/D	0°C to +70°C	Dice*	—
MAX4133ESD	-40°C to +85°C	14 SO	—
MAX4134ESD	-40°C to +85°C	14 SO	—

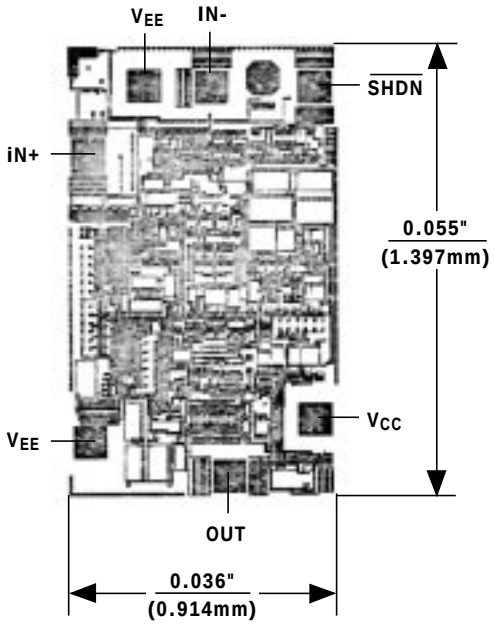
**Dice are specified at T_A = +25°C, DC parameters only.*

_____Chip Information

MAX4130 TRANSISTOR COUNT: 170
MAX4132 TRANSISTOR COUNT: 340
MAX4134 TRANSISTOR COUNT: 680

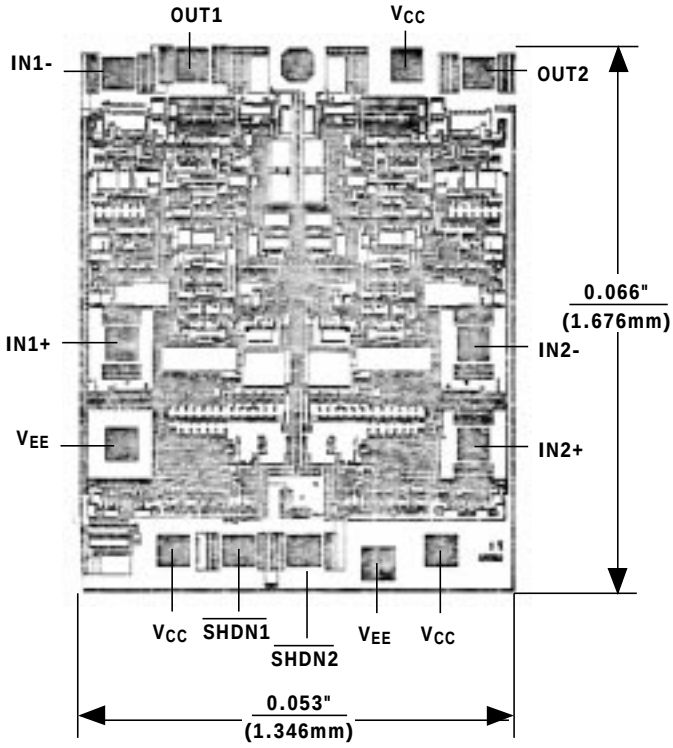
_____Chip Topographies

MAX4131

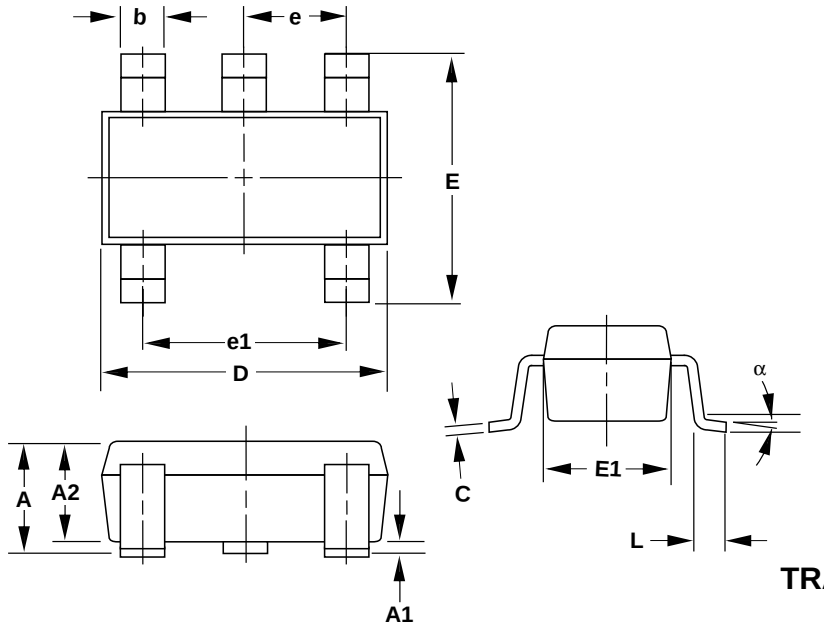


TRANSISTOR COUNT: 170
SUBSTRATE CONNECTED TO V_{EE}

MAX4133



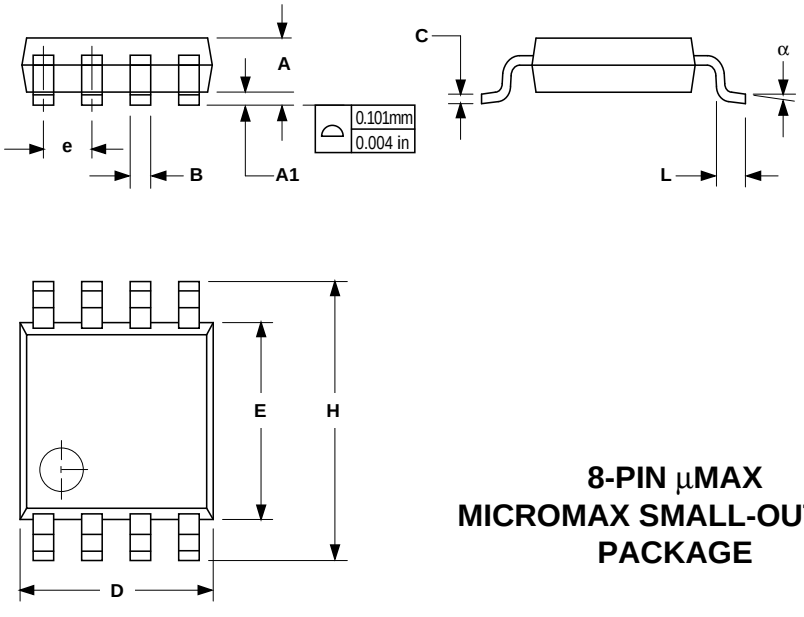
TRANSISTOR COUNT: 340
SUBSTRATE CONNECTED TO V_{EE}



DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95ref	
e1	1.90ref	
α	0°	10°

21-0057B

5-PIN SOT23-5 SMALL-OUTLINE TRANSISTOR PACKAGE



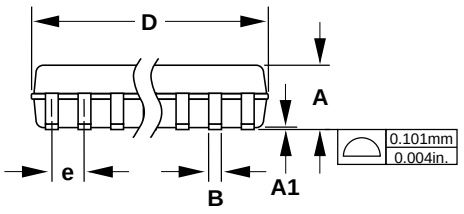
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
E	0.116	0.120	2.95	3.05
e	0.0256		0.65	
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

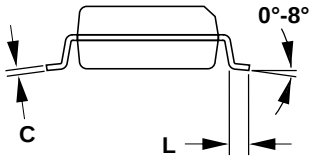
21-0036D

8-PIN μMAX MICROMAX SMALL-OUTLINE PACKAGE

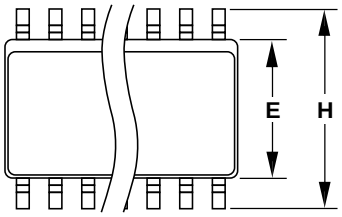
Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

Package Information (continued)





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27



Narrow SO SMALL-OUTLINE PACKAGE (0.150 in.)

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A

4.9 MAX427

19-0095; Rev 0; 11/92

MAXIM

Low Noise, High-Precision Op Amps

General Description

The MAX427/MAX437 ±15V operational amplifiers feature a superior combination of low wideband noise, and ultra-low offset voltage and drift; 2.5nV/√Hz (1kHz) noise, less than 15µV offset voltage (5µV typ), and less than 0.8µV/°C drift (0.1µV/°C typ). Voltage gain is 20 million when driving a 2kΩ load to ±12V, and 12 million with a 600Ω load to ±10V.

The MAX427 is unity-gain stable, with an 8MHz gain bandwidth and a 2.5V/µs slew rate. The decompensated MAX437 has a 60MHz gain bandwidth, a 15V/µs slew rate, and is stable for closed-loop gains of 5 or greater.

For applications requiring even lower noise and low-power performance from ±5V supplies, see the MAX410/MAX412/MAX414 data sheet.

Applications

Low-Noise Signal Processing

Threshold Detection

Strain-Gauge Amplifiers

Microphone Preamplifiers

Features

- ♦ **15µV Max Offset Voltage**
- ♦ **0.8µV/°C Max Drift**
- ♦ **Low Noise Performance:**
  4.5nV/√Hz Max (10Hz)
  3.8nV/√Hz Max (1kHz)
- ♦ **High-Voltage Gain:**
  7 Million Min (2kΩ Load)
  3 Million Min (600Ω Load)
- ♦ **117dB Min CMRR**
- ♦ **60MHz Gain-Bandwidth Product (MAX437)**

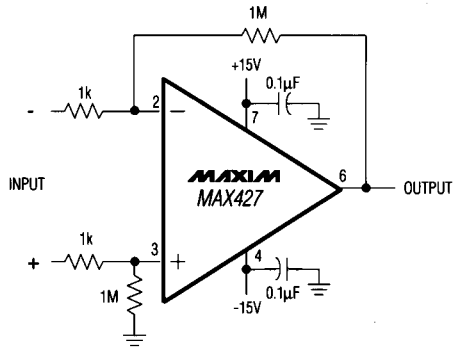
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX427CPA	0°C to +70°C	8 Plastic DIP
MAX427CSA	0°C to +70°C	8 SO
MAX427C/D	0°C to +70°C	Dice*
MAX427EPA	-40°C to +85°C	8 Plastic DIP
MAX427ESA	-40°C to +85°C	8 SO
MAX427MJA	-55°C to +125°C	8 CERDIP**
MAX437CPA	0°C to +70°C	8 Plastic DIP
MAX437CSA	0°C to +70°C	8 SO
MAX437C/D	0°C to +70°C	Dice*
MAX437EPA	-40°C to +85°C	8 Plastic DIP
MAX437ESA	-40°C to +85°C	8 SO
MAX437MJA	-55°C to +125°C	8 CERDIP**

** Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for availability and processing to MIL-STD-883.*

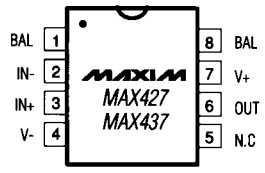
Typical Application Circuit

PRECISION HIGH-GAIN DIFFERENTIAL AMPLIFIER



Pin Configuration

TOP VIEW



DIP/SO

Ultra-Low Noise, High-Precision Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Continuous
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX427/MAX437C_A ..... 0°C to +70°C
MAX427/MAX437E_A ..... -40°C to +85°C
MAX427/MAX437MJA ..... -55°C to +125°C
Junction Temperature Range ..... -65°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
Note 2: MAX427/MAX437 inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 3)	V_{OS}			5	15	µV
Long-Term V_{OS} Stability (Notes 4, 5)	V_{OS}/TIME			0.2	1.0	µV/Mo
Input Bias Current	I_B			±10	±35	nA
Input Offset Current	I_{OS}			7	30	nA
Input Voltage Range	I_{VR}		±11.0	±12.5		V
Input Resistance – Common Mode	R_{INCM}			7		GΩ
Input Noise Voltage (Notes 5, 6)	e_{np-p}	0.1Hz to 10Hz		0.06	0.13	μV_{p-p}
Input Noise-Voltage Density (Note 5)	e_n	f_O = 10Hz		2.8	4.5	$nV/\sqrt{Hz}$
		f_O = 1kHz		2.5	3.8	
Input Noise-Current Density (Notes 5, 7)	i_n	f_O = 10Hz		1.5	4.0	$pA/\sqrt{Hz}$
		f_O = 1kHz		0.4	0.6	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±12V	7	20		V/µV
		$R_L \geq 1k\Omega$, V_O = ±10V	5	16		
		$R_L \geq 600\Omega$, V_O = ±10V	3	12		
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±13.0	±13.8		V
		$R_L \geq 600\Omega$	±11.0	±12.5		
Open-Loop Output Resistance	R_O	V_O = 0, I_O = 0		70		Ω
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11V	117	130		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4V to ±18V	110	130		dB
Gain-Bandwidth Product (Note 5)	GBP	MAX427, f_O = 100kHz	5.0	8.0		MHz
		MAX437, f_O = 10kHz, $A_{VCL} \geq 5$	45	60		
Slew Rate (Note 5)	SR	MAX427, $R_L \geq 2k\Omega$	1.7	2.8		V/µs
		MAX437, $R_L \geq 2k\Omega$, $A_{VCL} \geq 5$	11	17		
Power Dissipation	PD	V_O = 0		80	120	mW
Offset Adjustment Range		R_P = 10kΩ		±4.0		mV

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 3)	V_{OS}			20	50	µV
Average Offset-Voltage Drift (Notes 5, 8)	TCV_{OS}			0.1	0.8	µV/°C
Input Bias Current	I_B			±20	±60	nA
Input Offset Current	I_{OS}			15	50	nA
Input Voltage Range	I_{VR}	MAX4_7C/E	±10.5	±11.8		V
		MAX4_7M	±10.3	±11.5		
Large-Signal Voltage Gain	AV_O	R_L ≥ 2kΩ, V_O = ±10V	3.0	14.0		V/µV
		R_L ≥ 1kΩ, V_O = ±10V	2.0	10.0		
Maximum Output-Voltage Swing	V_O	R_L ≥ 2kΩ	±12.5	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±10V	112	126		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	104	126		dB
Power Dissipation	PD			100	150	mW

Note 3: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 sec after application of power.

Note 4: Long-Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5µV – refer to typical performance curve.

Note 5: Guaranteed by design.

Note 6: See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the *Applications Information* section.

Note 7: See the test circuit for current noise measurement in the *Applications Information* section.

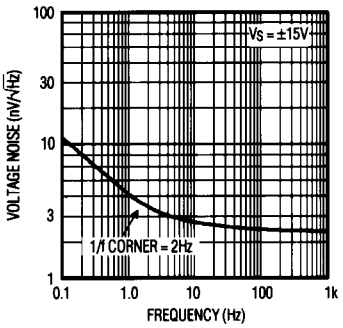
Note 8: The average input offset drift performance is within the specifications unnulled or when nulled with a pot having a range of 8kΩ to 20kΩ. Contact factory for the availability of a higher-performance, 100% tested drift parameter of 0.4µV/°C max.

Ultra-Low Noise, High-Precision Op Amps

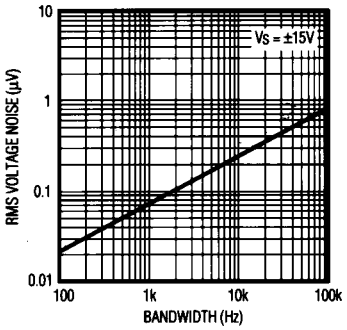
Typical Operating Characteristics

(TA = +25°C, unless otherwise noted.)

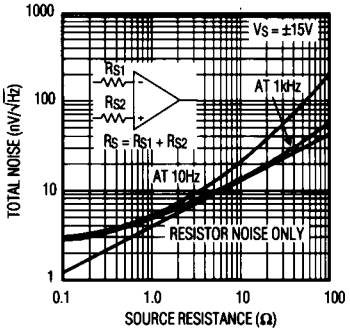
VOLTAGE-NOISE DENSITY vs. FREQUENCY



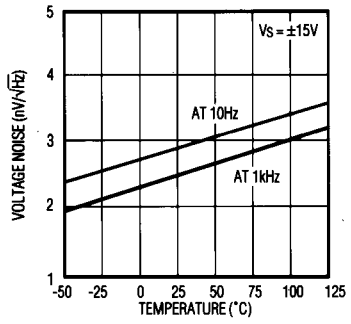
INPUT WIDEBAND VOLTAGE NOISE vs. BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



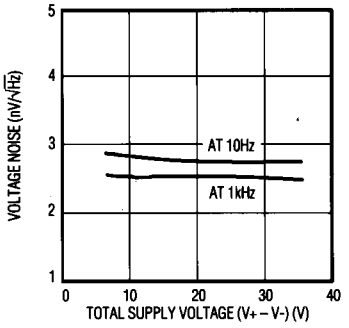
TOTAL NOISE vs. SOURCE RESISTANCE



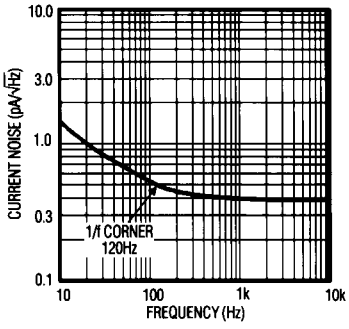
VOLTAGE-NOISE DENSITY vs. TEMPERATURE



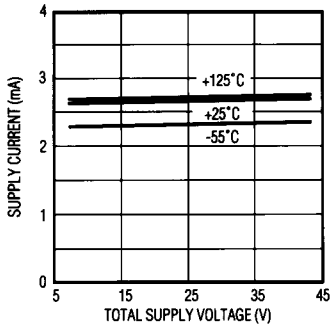
VOLTAGE-NOISE DENSITY vs. SUPPLY VOLTAGE



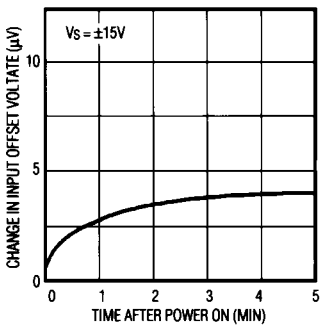
CURRENT-NOISE DENSITY vs. FREQUENCY



SUPPLY CURRENT vs. SUPPLY VOLTAGE



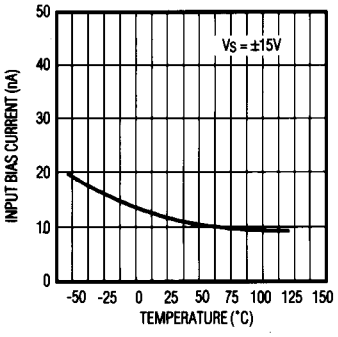
WARM-UP OFFSET-VOLTAGE DRIFT



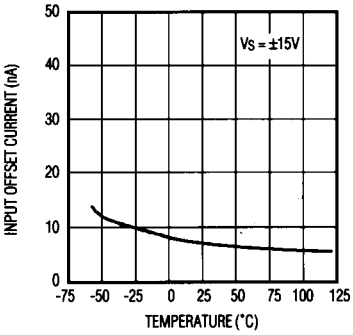
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

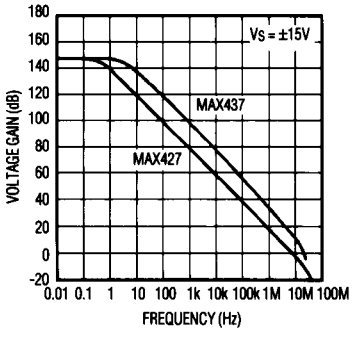
INPUT BIAS CURRENT vs. TEMPERATURE



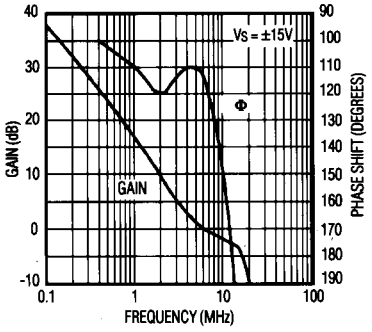
INPUT OFFSET CURRENT vs. TEMPERATURE



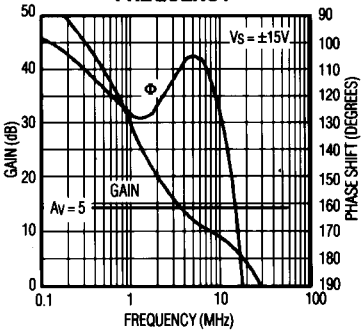
VOLTAGE GAIN vs. FREQUENCY



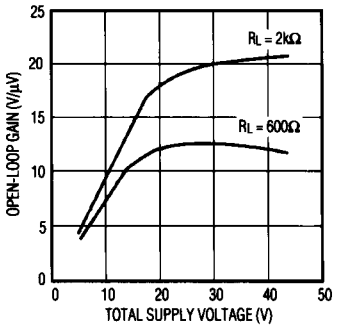
MAX427 GAIN, PHASE SHIFT vs. FREQUENCY



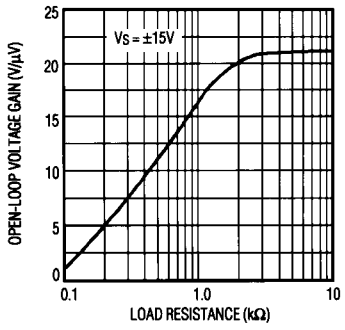
MAX437 GAIN, PHASE SHIFT vs. FREQUENCY



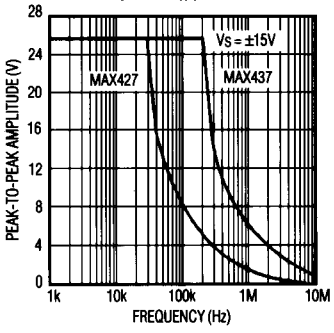
OPEN-LOOP VOLTAGE GAIN vs. SUPPLY VOLTAGE



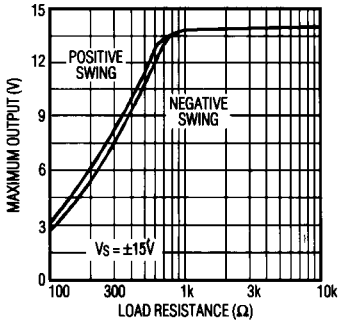
OPEN-LOOP VOLTAGE GAIN vs. LOAD RESISTANCE



MAXIMUM OUTPUT SWING vs. FREQUENCY



MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE

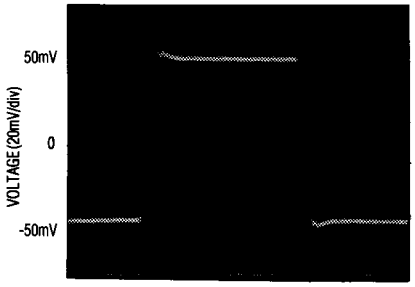


Ultra-Low Noise, High-Precision Op Amps

Typical Operating Characteristics (continued)

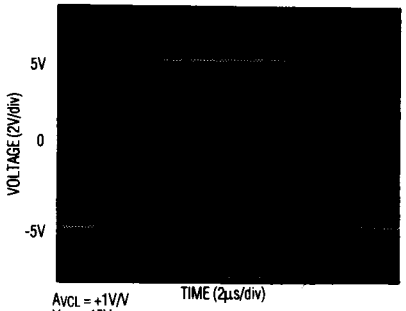
(T_A = +25°C, unless otherwise noted.)

MAX427
SMALL-SIGNAL TRANSIENT RESPONSE



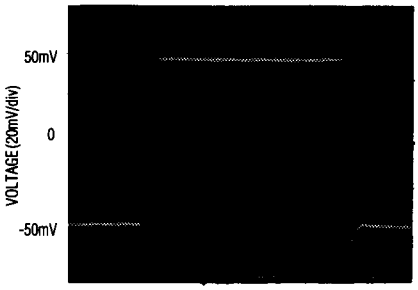
A_{VCL} = +1V/V, C_L = 15pF
V_S = ±15V

MAX427
LARGE-SIGNAL TRANSIENT RESPONSE



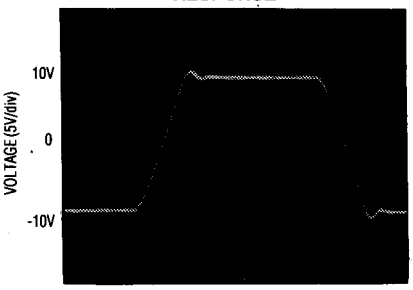
A_{VCL} = +1V/V
V_S = ±15V

MAX437
SMALL-SIGNAL TRANSIENT RESPONSE



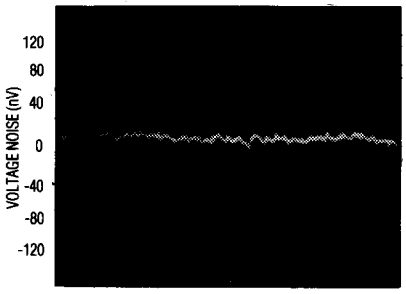
V_S ±15V
A_{VCL} = +5V/V

MAX437
LARGE-SIGNAL TRANSIENT RESPONSE



V_S = ±15V
A_{VCL} = +5V/V

LOW-FREQUENCY NOISE



0.1Hz TO 10Hz PEAK-TO-PEAK NOISE
NOTE: (OBSERVATION TIME LIMITED TO 10 SECONDS.)

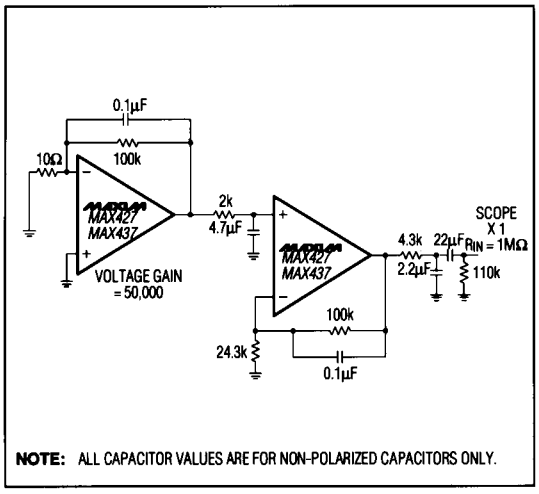


Figure 1. Voltage-Noise Test Circuit (0.1Hz to 10Hz)

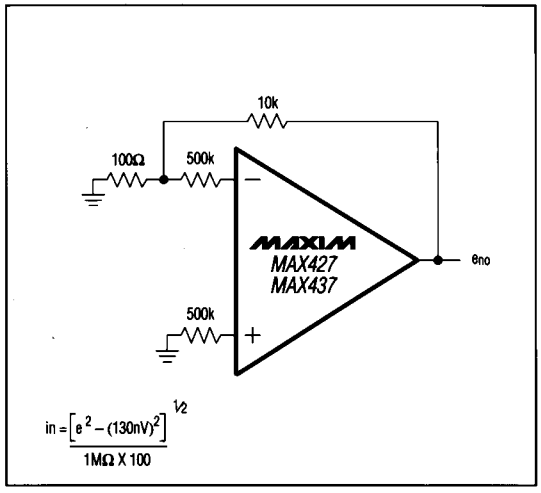


Figure 2. Current-Noise Test Circuit

Applications Information

The MAX427/MAX437 provide stable operation with load capacitances of up to 2nF and ±10V output swings; larger capacitances should be decoupled with a 50Ω series resistor inside the feedback loop. The MAX427 is unity-gain stable and the MAX437 is stable at gains of five or greater.

Thermoelectric voltages generated by dissimilar metals at the input terminals degrade the drift performance. Connections to both inputs should be maintained at the same temperature for best operation.

Offset-Voltage Adjustment

Input offset voltage (V_{OS}) is trimmed at the wafer level. If V_{OS} adjustment is necessary, a 10kΩ trim potentiometer (pot) may be used and will not degrade TCV_{OS} (Figure 3). Other trim pot values from 1kΩ to 1MΩ can be used with a slight degradation (0.1µV/°C to 0.2µV/°C) of TCV_{OS}. Adjusting, but not zeroing, V_{OS} creates a drift of approximately (V_{OS}/300)µV/°C. The adjustment range with a 10kΩ trim pot is ±4mV. For a smaller range, reduce nulling sensitivity by connecting a smaller pot in series with fixed resistors; for example, Figure 4 has a ±70µV adjustment range.

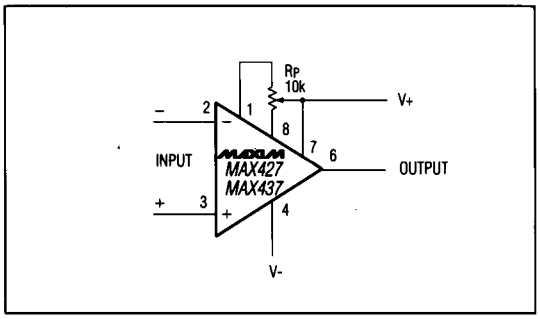


Figure 3. Offset Nulling Circuit

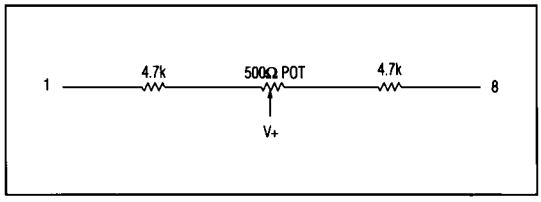


Figure 4. Alternate Offset-Voltage Adjustment

Ultra-Low Noise, High-Precision Op Amps

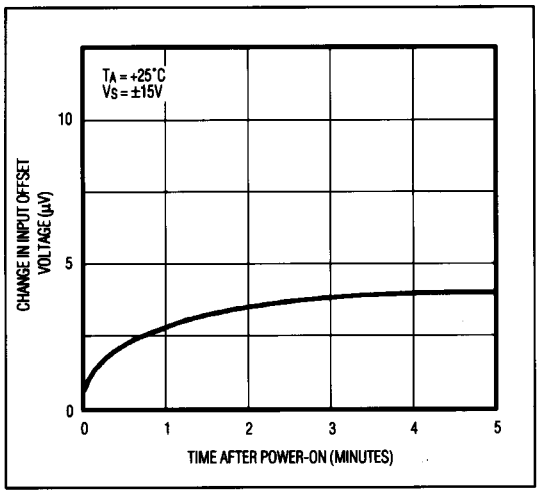


Figure 5. Warm-Up Offset Voltage Drift

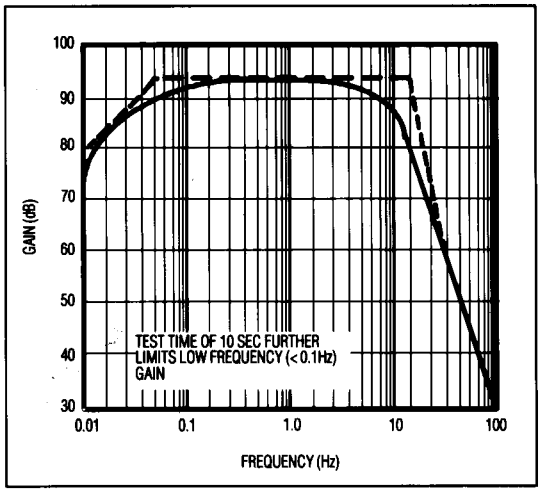


Figure 6. 0.1Hz to 10Hz V_{p-p} Noise Tester Frequency Response

Noise Measurements

To measure the 60nV_{p-p} noise specification of the MAX427/MAX437 in the 0.1Hz to 10Hz range, observe the following precautions:

1. The device must warm up for at least five minutes. Figure 5 shows how V_{OS} typically increases 4µV with increases in chip temperature after power-up. In the 10sec measurement interval, temperature-induced effects can exceed 10nV.

2. For similar reasons, the device must be well-shielded from air currents, including those caused by motion. This minimizes thermocouple effects.

3. As shown in Figure 6, the 0.1Hz corner is defined by only one zero. A maximum test time of 10sec acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

4. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement correlates well with a 0.1Hz to 10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

Unity-Gain Buffer Applications (MAX427 Only)

Figure 7 shows the circuit and output waveform with $R_f \leq 100\Omega$, and the input driven with a fast, large signal pulse (>1V).

During the fast rise portion of the output, the input protection diodes short the output to the input, and a current, limited only by the output short-circuit protection, is drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirement ($I_L \leq 20mA$ at 10V) and a smooth transition occurs.

When $R_f \geq 2k\Omega$, a pole created with R_f and the amplifier's input capacitance (8pF) causes additional phase shift and reduces phase margin. A small capacitor (20pF to 50pF) in parallel with R_f eliminates this problem.

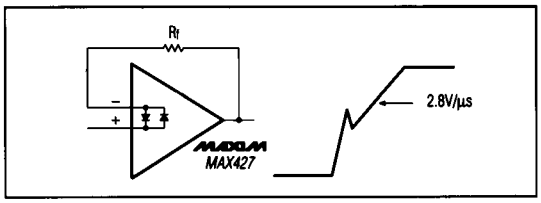


Figure 7. Pulsed Operation of Unity-Gain Buffer

Comments on Noise

The MAX427/MAX437 are very low-noise amplifiers. They achieve outstanding input voltage noise characteristics by operating the input stage at a high quiescent current. Input bias and offset currents, which would normally increase with the quiescent current, are minimized by bias-current cancellation circuitry. The MAX427/MAX437 have I_B and I_{OS} of only ±35nA and 30nA respectively at +25°C. This is particularly important with high source-resistances.

Voltage noise is inversely proportional to the square-root of bias current, but current noise is proportional to the square-root of bias current. The MAX427/MAX437 low-noise advantages are reduced when high source resistors are used.

Total noise = $[(\text{voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise})^2]^{1/2}$

Figure 8 shows noise vs. source resistance at 1kHz. To use this plot for wideband noise, multiply the vertical scale by the square-root of the bandwidth. The MAX427/MAX437 maintain low input noise voltage with $R_S < 1k\Omega$. With $R_S > 1k\Omega$, total noise increases and is dominated by the resistor noise, not the current or the voltage noise. It is only with $R_S \geq 20k\Omega$ that current noise dominates. Current noise is not important for applications with $R_S < 20k\Omega$. The MAX427/MAX437 have lower total noise than the MAX400/OP07 for $R_S < 10k\Omega$. As R_S increases, the crossover between the MAX427/MAX437 and the MAX400/OP07 noise occurs in the $R_S = 15k\Omega$ to $40k\Omega$ region.

Figure 9 shows 0.1Hz to 10Hz peak-to-peak noise. Here, resistor noise is negligible and current noise (i_n) becomes important, because $i_n \propto 1/\sqrt{f}$. The crossover with the MAX400/OP07 occurs in the $R_S = 3k\Omega$ to $5k\Omega$ range, depending on whether balanced or unbalanced source resistors are used (at $3k\Omega$ the I_B and I_{OS} error can be three times the V_{OS} specification). For low-frequency applications, the MAX400/OP07 are better than the MAX427/MAX437 when $R_S > 3k\Omega$, except when gain error is important. Figure 10 illustrates the 10Hz noise. As expected, the results fall between those of the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table 1.

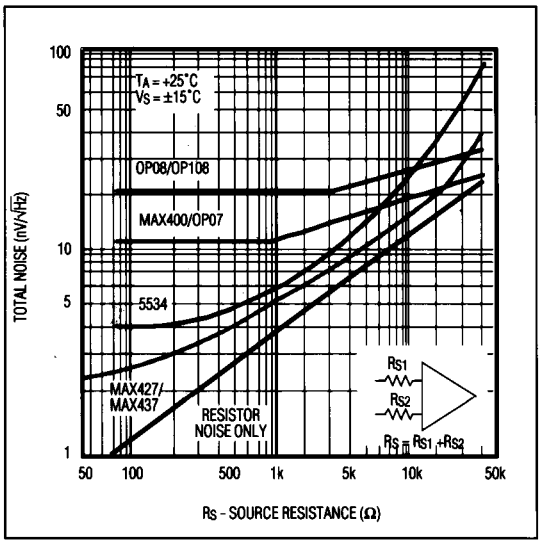


Figure 8. Noise vs. Source Resistance (Including Resistor Noise) at 1kHz

Table 1. Signal Source vs. Source Impedance

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain Gauge	<500Ω	Typically used in low-frequency applications.
Magnetic Tapehead	< 1500Ω	Low I_B is very important to reduce self-magnetization problems when direct coupling is used. MAX427 I_B can be neglected.
Linear Variable Differential Transformer	< 1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

Ultra-Low Noise, High-Precision Op Amps

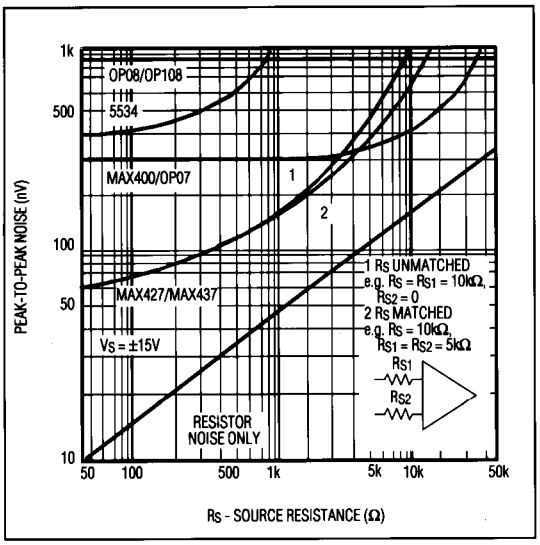


Figure 9. Peak-to-Peak Noise (0.1 to 10Hz) vs. Source Resistance (Includes Resistor Noise)

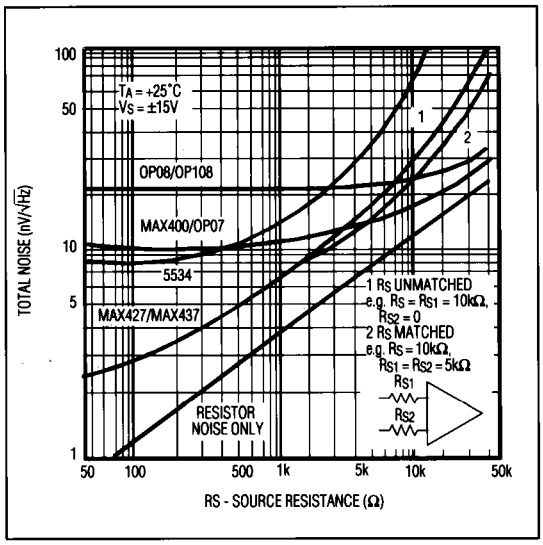
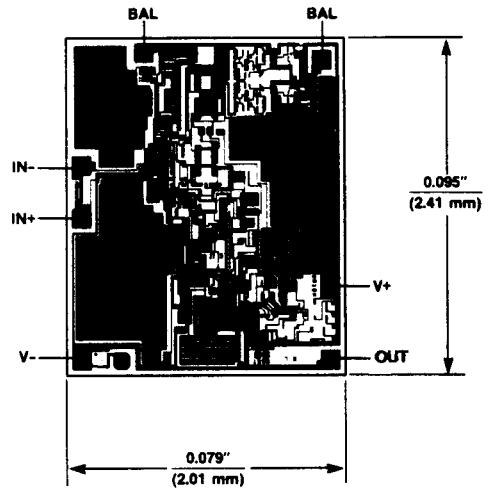


Figure 10. 10Hz Noise vs. Source Resistance (Includes Resistor Noise)

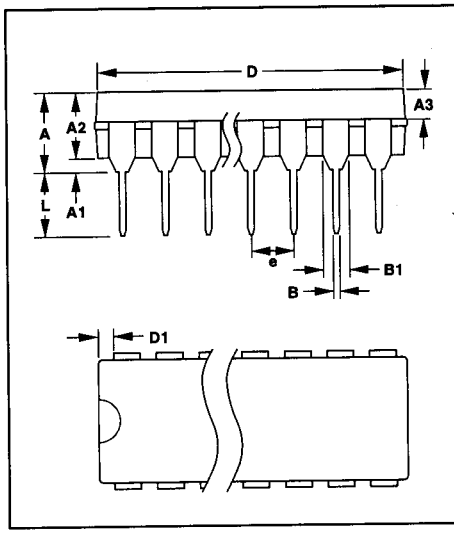
Chip Topography



MAX427/MAX437

SUBSTRATE CONNECTED TO V-

Package Information



Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

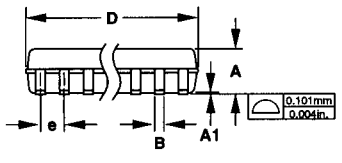
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

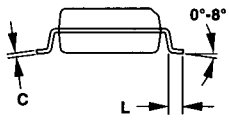
PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

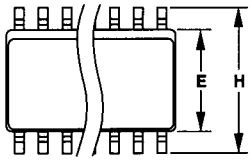
21-0043A

Ultra-Low Noise, High-Precision Op Amps

Package Information (continued)





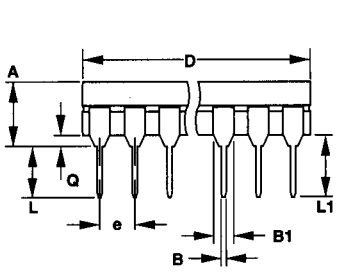


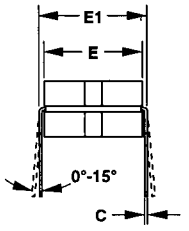
Narrow SO SMALL-OUTLINE PACKAGE (0.150 in.)

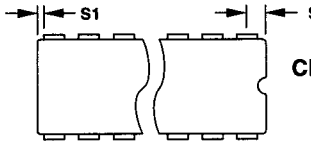
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A







CERDIP CERAMIC DUAL-IN-LINE PACKAGE (0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	–	0.405	–	10.29
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51

21-0045A

4.10 MAX547

19-0257; Rev 3; 12/95

MAXIM

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

General Description

The MAX547 contains eight 13-bit, voltage-output digital-to-analog converters (DACs). On-chip precision output amplifiers provide the voltage outputs. The MAX547 operates from a ±5V supply. Bipolar output voltages with up to ±4.5V voltage swing can be achieved with no external components. The MAX547 has four separate reference inputs; each is connected to two DACs, providing different full-scale output voltages for every DAC pair.

The MAX547 features double-buffered interface logic with a 13-bit parallel data bus. Each DAC has an input latch and a DAC latch. Data in the DAC latch sets the output voltage. The eight input latches are addressed with three address lines. Data is loaded to the input latch with a single write instruction. An asynchronous load ($\overline{LD\_}$) input transfers data from the input latch to the DAC latch. The four $\overline{LD\_}$ inputs each control two DACs, and all DAC latches can be updated simultaneously by asserting all $\overline{LD\_}$ pins. An asynchronous clear ($\overline{CLR}$) input resets the output of all eight DACs to AGND_. Asserting $\overline{CLR}$ resets both the DAC and the input latch to bipolar zero (1000hex). On power-up, reset circuitry performs the same function as $\overline{CLR}$. All logic inputs are TTL/CMOS compatible.

The MAX547 is available in 44-pin plastic quad flat pack and 44-pin PLCC packages.

Applications

Automatic Test Equipment
Minimum Component-Count Analog Systems
Digital Offset/Gain Adjustment
Arbitrary Function Generators
Industrial Process Controls
Avionics Equipment

Features

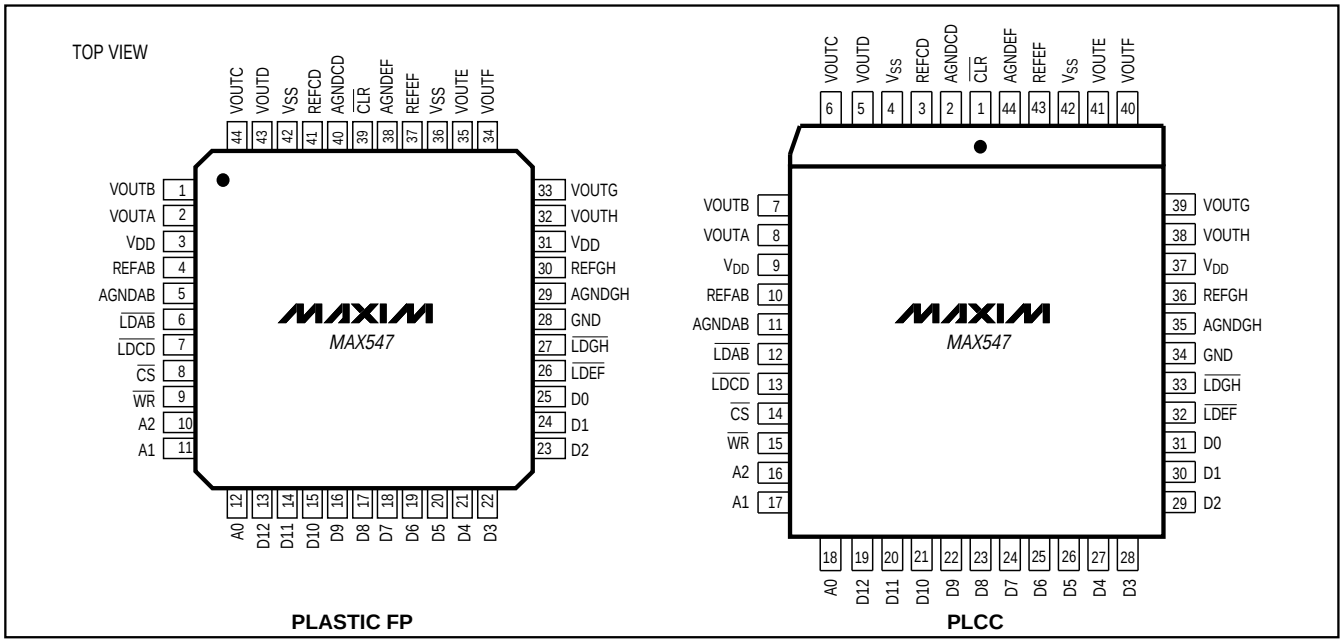
- **Full 13-Bit Performance without Adjustments**
- **8 DACs in One Package**
- **Buffered Voltage Outputs**
- **Calibrated Linearity**
- **Guaranteed Monotonic to 13 Bits**
- **±5V Supply Operation**
- **Unipolar or Bipolar Outputs Swing to ±4.5V**
- **Fast Output Settling (5µs to ±½LSB)**
- **Double-Buffered Digital Inputs**
- **Asynchronous Load Inputs Load Pairs of DAC Latches**
- **Asynchronous $\overline{CLR}$ Input Resets DACs to Analog Ground**
- **Power-On Reset Circuit Resets DACs to Analog Ground**
- **Microprocessor and TTL/CMOS Compatible**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX547ACQH	0°C to +70°C	44 PLCC	±2
MAX547BCQH	0°C to +70°C	44 PLCC	±4
MAX547ACMH	0°C to +70°C	44 Plastic FP	±2
MAX547BCMH	0°C to +70°C	44 Plastic FP	±4
MAX547BC/D	0°C to +70°C	Dice*	±4

Ordering Information continued at end of data sheet.
**Contact factory for dice specifications.*

Pin Configurations



Octal, 13-Bit Voltage-Output DAC with Parallel Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
V_{SS} to GND.....-6V to +0.3V
Digital Input Voltage to GND .....-0.3V to (V_{DD} + 0.3V)
REF_ .....(AGND_ - 0.3V) to (V_{DD} + 0.3V)
AGND_ .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
VOUT_ .....V_{DD} to V_{SS}
Maximum Current into REF_ Pin.....±10mA
Maximum Current into Any Other Signal Pin .....±50mA

Continuous Power Dissipation (T_A = +70°C)
PLCC (derate 13.33mW/°C above +70°C).....1067mW
Plastic FP (derate 11.11mW/°C above +70°C).....889mW
Operating Temperature Ranges
MAX547_C_H.....0°C to +70°C
MAX547_E_H.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -5V, REF_ = 4.096V, AGND_ = GND = 0V, R_L = 10kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		13			Bits
Relative Accuracy	INL	MAX547A		±0.5	±2	LSB
		MAX547B		±0.5	±4	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Bipolar Zero-Code Error				±5	±20	LSB
Gain Error				±1	±8	LSB
Power-Supply Rejection Ratio	PSRR	$\Delta Gain/\Delta V_{DD}$ (Note 1)			±0.0025	%/%
		$\Delta Gain/\Delta V_{SS}$ (Note 1)			±0.0025	
Load Regulation		R_L = ∞ to 10kΩ		0.3		LSB
REFERENCE INPUT (Note 2)						
Reference Input Range	REF	(Notes 2, 3)	AGND_		V_{DD}	V
Reference Input Resistance	RREF	Each REF_ pin (Note 3)	5			kΩ
ANALOG OUTPUT						
Maximum Output Voltage				V_{DD} - 0.5		V
Minimum Output Voltage				V_{SS} + 0.5		V
DYNAMIC PERFORMANCE—ANALOG SECTION						
Voltage-Output Slew Rate				3		V/µs
Output Settling Time		To ±½ LSB of full scale (Note 4)		5		µs
Digital Feedthrough				5		nV-s
Digital Crosstalk				5		nV-s
DIGITAL INPUTS (V_{DD} = 5V ±5%)						
Input Voltage High	V_{IH}		2.4			V
Input Voltage Low	V_{IL}				0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}			1.0	µA
Input Capacitance	C_{IN}	(Note 5)			10	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{SS} = -5V, REF_ = 4.096V, AGND_ = GND = 0V, R_L = 10kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply Range	V_{DD}	(Note 6)	4.75		5.25	V
Negative Supply Range	V_{SS}	(Note 6)	-5.25		-4.75	V
Positive Supply Current	I_{DD}	T_A = T_{MIN} to T_{MAX}		14	44	mA
Negative Supply Current	I_{SS}	T_A = T_{MIN} to T_{MAX}		11	40	mA

Note 1: PSRR is tested by changing the respective supply voltage by ±5%.
Note 2: For best performance, REF_ should be greater than AGND_ + 2V and less than V_{DD} - 0.6V. The device operates with reference inputs outside this range, but performance may degrade. For further information on the reference, see the *Reference and Analog-Ground Inputs* section in the *Detailed Description*.
Note 3: Reference input resistance is code dependent. See *Reference and Analog-Ground Inputs* section in the *Detailed Description*.
Note 4: Typical settling time with 1000pF capacitive load is 10µs.
Note 5: Guaranteed by design. Not production tested.
Note 6: Guaranteed by supply-rejection test.

TIMING CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -5V, REF_ = 4.096V, AGND_ = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

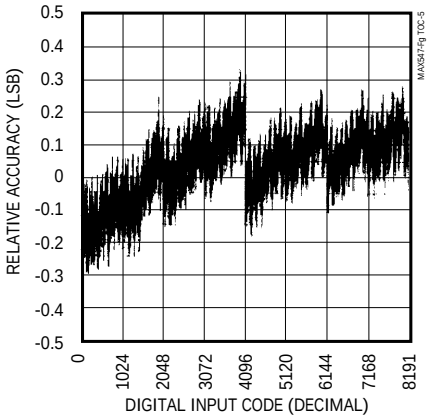
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Pulse Width Low	t_1		50			ns
$\overline{WR}$ Pulse Width Low	t_2		50			ns
$\overline{LD\_}$ Pulse Width Low	t_3		50			ns
$\overline{CLR}$ Pulse Width Low	t_4		100			ns
$\overline{CS}$ Low to $\overline{WR}$ Low	t_5		0			ns
$\overline{CS}$ High to $\overline{WR}$ High	t_6		0			ns
Data Valid to $\overline{WR}$ Setup	t_7		50			ns
Data Valid to $\overline{WR}$ Hold	t_8		0			ns
Address Valid to $\overline{WR}$ Setup	t_9		10			ns
Address Valid to $\overline{WR}$ Hold	t_{10}		0			ns

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

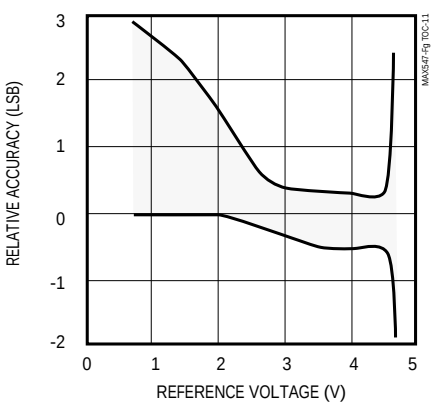
Typical Operating Characteristics

(V_{DD} = 5V, V_{SS} = -5V, REF_ = 4.096V, AGND_ = GND = 0V, T_A = +25°C, unless otherwise noted.)

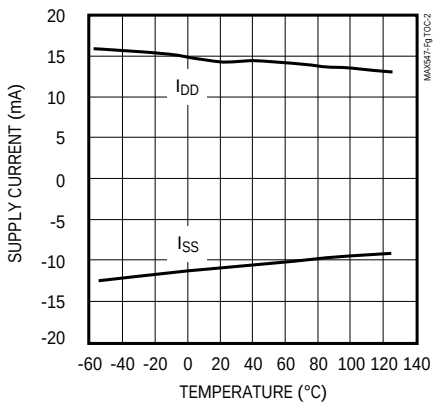
RELATIVE ACCURACY vs. DIGITAL INPUT CODE



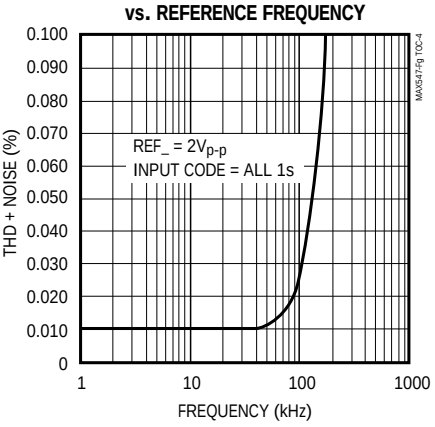
RELATIVE ACCURACY vs. REFERENCE VOLTAGE



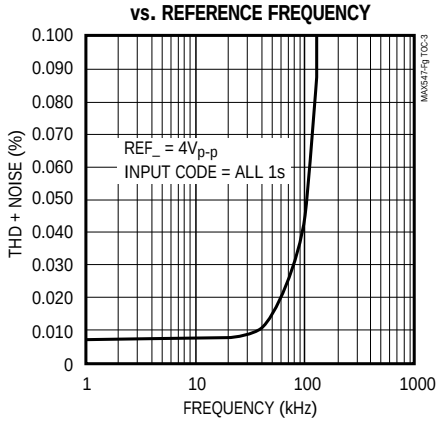
SUPPLY CURRENT vs. TEMPERATURE



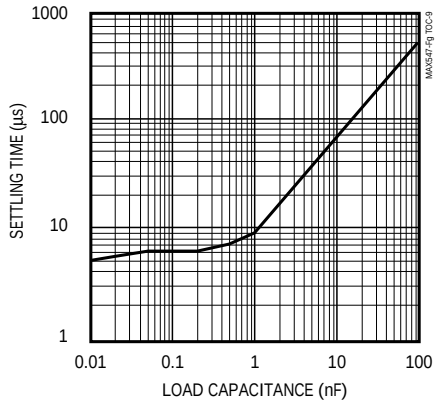
TOTAL HARMONIC DISTORTION + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY



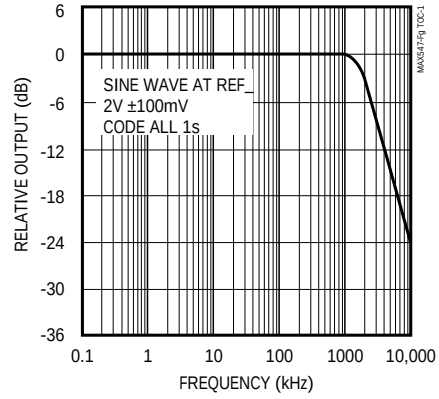
TOTAL HARMONIC DISTORTION + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY



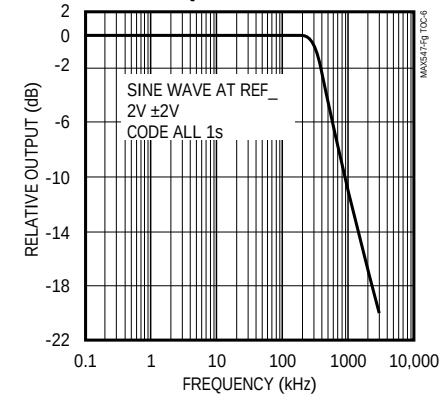
SETTLING TIME vs. LOAD CAPACITANCE



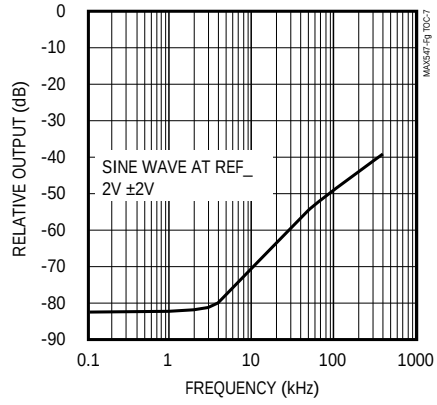
REFERENCE INPUT SMALL-SIGNAL FREQUENCY RESPONSE



REFERENCE INPUT LARGE-SIGNAL FREQUENCY RESPONSE



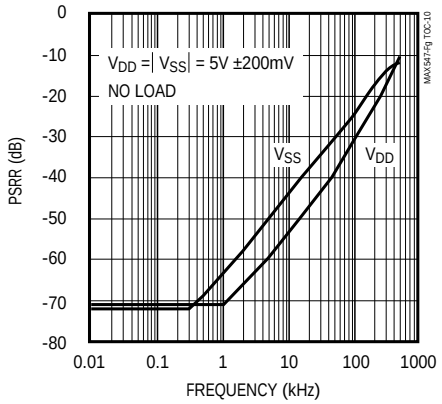
REFERENCE FEEDTHROUGH



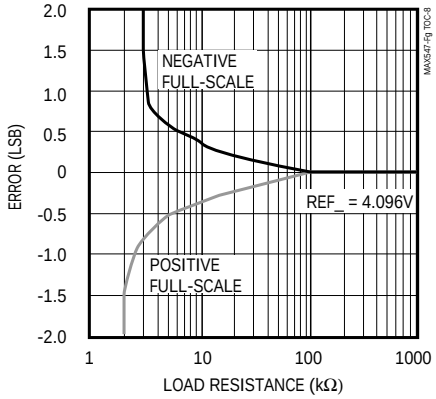
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{SS} = -5V, REF_ = 4.096V, AGND_ = GND = 0V, T_A = +25°C, unless otherwise noted.)

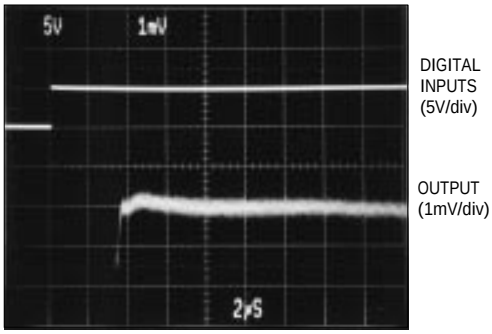
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



FULL-SCALE ERROR vs. LOAD RESISTANCE



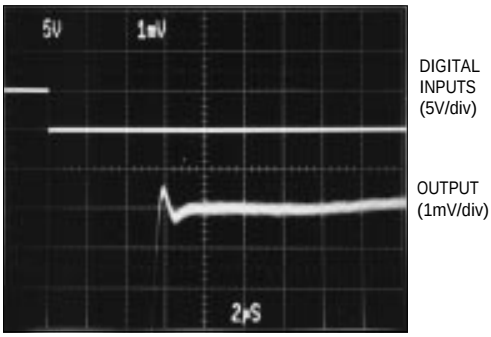
POSITIVE SETTLING TIME TO FULL-SCALE STEP (ALL BITS OFF TO ALL BITS ON)



2µs/div

REF_ = 4.096V, C_L = 100pF, R_L = 5kΩ

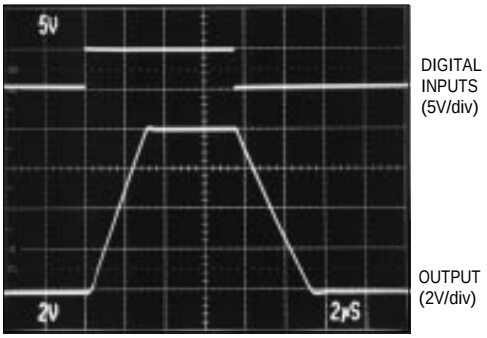
NEGATIVE SETTLING TIME TO FULL-SCALE STEP (ALL BITS ON TO ALL BITS OFF)



2µs/div

REF_ = 4.096V, C_L = 100pF, R_L = 5kΩ

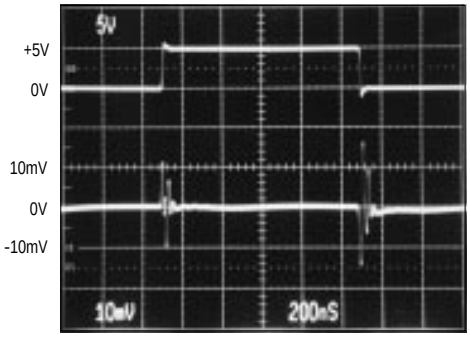
DYNAMIC RESPONSE (ALL BITS OFF, ON, OFF)



2µs/div

REF_ = 4.096V, C_L = 100pF, R_L = 5kΩ

DIGITAL FEEDTHROUGH (GLITCH IMPULSE)



200ns/div

TOP: DIGITAL TRANSITION ON ALL DATA BITS

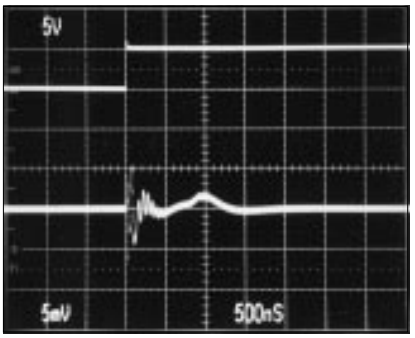
BOTTOM: DAC OUTPUT WITH $\overline{WR}$ HIGH 10mV/div

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

Typical Operating Characteristics (continued)

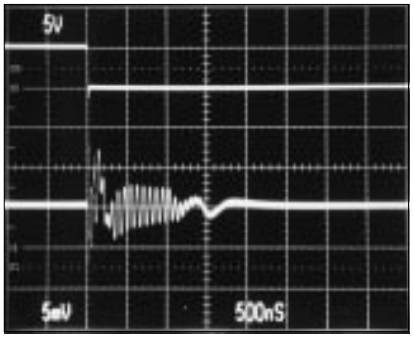
(V_{DD} = 5V, V_{SS} = -5V, REF_ = 4.096V, AGND_ = GND = 0V, T_A = +25°C, unless otherwise noted.)

ADJACENT-CHANNEL CROSSTALK



500ns/div
REF_ = 4.096V, C_L = 50pF, R_L = 10kΩ
A: DIGITAL INPUTS, DAC A, DATA BITS from ALL Os to OAAAhex
B: OUTPUT, DAC B

ADJACENT-CHANNEL CROSSTALK



500ns/div
REF_ = 4.096V, C_L = 50pF, R_L = 10kΩ
A: DIGITAL INPUTS, DAC A, DATA BITS from OAAAhex to ALL Os
B: OUTPUT, DAC B

Pin Description

PIN		NAME	FUNCTION
PLCC	FLAT PACK		
1	39	$\overline{CLR}$	Clear Input (active low). Driving this asynchronous input low sets the content of all latches to 1000hex. All DAC outputs are reset to AGND_.
2	40	AGNDCD	Analog Ground for DAC C and DAC D
3	41	REFCD	Reference Voltage Input for DAC C and DAC D. Bypass to AGNDCD with a 0.1µF to 1µF capacitor.
4, 42	42, 36	V_{SS}	Negative Power Supply, -5V (2 pins). Connect both pins to the supply voltage. Bypass each pin to the system analog ground with a 0.1µF to 1µF capacitor.
5	43	VOUTD	DAC D Output Voltage
6	44	VOUTC	DAC C Output Voltage
7	1	VOUTB	DAC B Output Voltage
8	2	VOUTA	DAC A Output Voltage
9, 37	3, 31	V_{DD}	Positive Power Supply, 5V (2 pins). Connect both pins to the supply voltage. Bypass each pin to the system analog ground with a 0.1µF to 1µF capacitor.
10	4	REFAB	Reference Voltage Input for DAC A and DAC B. Bypass to AGNDAB with a 0.1µF to 1µF capacitor.
11	5	AGNDAB	Analog Ground for DAC A and DAC B
12	6	$\overline{LDAB}$	Load Input (active low). Driving this asynchronous input low transfers the contents of input latches A and B to the respective DAC latches.
13	7	$\overline{LDCD}$	Load Input (active low). Driving this asynchronous input low transfers the contents of input latches C and D to the respective DAC latches.
14	8	$\overline{CS}$	Chip Select (active low)
15	9	$\overline{WR}$	Write Input (active low). $\overline{WR}$, along with $\overline{CS}$, loads data into the DAC input latch selected by A0–A2.

Pin Description (continued)

PIN		NAME	FUNCTION
PLCC	FLAT PACK		
16	10	A2	Address Bit 2
17	11	A1	Address Bit 1
18	12	A0	Address Bit 0
19–31	13–25	D12–D0	Data Bits 12–0
32	26	$\overline{\text{LDEF}}$	Load Input (active low). Driving this asynchronous input low transfers the contents of input latches E and F to the respective DAC latches.
33	27	$\overline{\text{LDGH}}$	Load Input (active low). Driving this asynchronous input low transfers the contents of input latches G and H to the respective DAC latches.
34	28	GND	Digital Ground
35	29	AGNDGH	Analog Ground for DAC G and DAC H
36	30	REFGH	Reference Voltage Input for DAC G and DAC H. Bypass to AGNDGH with a 0.1µF to 1µF capacitor.
38	32	VOUTH	DAC H Output Voltage
39	33	VOUTG	DAC G Output Voltage
40	34	VOUTF	DAC F Output Voltage
41	35	VOUTE	DAC E Output Voltage
43	37	REFEF	Reference Voltage Input for DAC E and DAC F. Bypass to AGNDEF with a 0.1µF to 1µF capaci-
44	38	AGNDEF	Analog Ground for DAC E and DAC F

Detailed Description

Analog Section

The MAX547 contains eight 13-bit, voltage-output DACs. These DACs are “inverted” R-2R ladder networks that convert 13-bit digital inputs into equivalent analog output voltages, in proportion to the applied reference voltages. The MAX547 has one reference input (REF_) and one analog-ground input (AGND_) for each pair of DACs. The four REF_ inputs allow different full-scale output voltages for each DAC pair, and the four AGND_ inputs allow different offset voltages for each DAC pair.

The DAC ladder outputs are buffered with op amps that operate with a gain of two. The inverting node of the amplifier is connected to the respective reference input, resulting in bipolar output voltages from -REF_ to 4095/4096 REF_. Figure 1 shows the simplified DAC circuit.

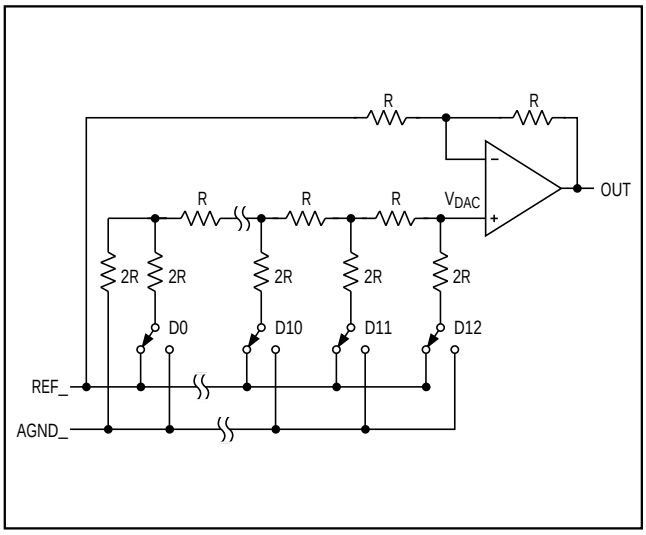


Figure 1. DAC Simplified Circuit Diagram

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

Reference and Analog-Ground Inputs

The REF_ inputs can range between AGND_ and V_{DD}. However, the DAC outputs will operate to V_{DD} - 0.6V and V_{SS} + 0.6V, due to the output amplifiers' voltage-swing limitations. The AGND_ inputs can be offset by any voltage within the supply rails. The offset-voltage potential must be lower than the reference-voltage potential. For more information, refer to the *Digital Code* and *Analog Output Voltage* section in the *Applications Information.*

The input impedance of the REF_ inputs is code dependent. It is at its lowest value (5kΩ min) when the input code of the referring DAC pair is 0 1010 1010 1010 (0AAAhex). Its maximum value, typically 50kΩ, occurs when the code is 0000hex. When all reference inputs are driven from the same source, the minimum load impedance is 1.25kΩ. Since the input impedance at REF_ is code dependent, load regulation of the reference used is important. For more information, see *Reference Selection* in the *Applications Information* section.

The input capacitance at REF_ is also code dependent, and typically varies from 125pF to 300pF. Its minimum value occurs when the code of the referring DAC pair is set to all 0s. It is at its maximum value with all 1s on both DACs.

Output Buffer Amplifiers

The MAX547's voltage outputs are internally buffered by precision gain-of-two amplifiers with a typical slew rate of 3V/µs. With a full-scale transition at its output, the typical settling time to ±½LSB is 5µs when loaded with 10kΩ in parallel with 50pF, or 6µs when loaded with 10kΩ in parallel with 100pF.

Digital Inputs and Interface Logic

All digital inputs are compatible with both TTL and CMOS logic. The MAX547 interfaces with microprocessors using a data bus at least 13 bits wide. The interface is double buffered, allowing simultaneous update of all DACs. There are two latches for each DAC (see *Functional Diagram*): an input latch that receives data from the data bus, and a DAC latch that receives data from the input latch. Address lines A0, A1, and A2 select which DAC's input latch receives data from the data bus, as shown in Table 1. Transfer data from the input latches to the DAC latches by asserting the asynchronous $\overline{LD\_}$ signal. Each DAC's analog output reflects the data held in its DAC latch. All control inputs are level triggered.

Data can be latched or transferred directly to the DAC. $\overline{CS}$ and $\overline{WR}$ control the input latch and $\overline{LD\_}$ transfers information from the input latch to the DAC latch. The input latch is transparent when $\overline{CS}$ and $\overline{WR}$ are low, and the DAC latch is transparent when $\overline{LD\_}$ is low. The address lines (A0, A1, A2) must be valid throughout the time $\overline{CS}$ and $\overline{WR}$ are low (Figure 3). Otherwise, the data can be inadvertently written to the wrong DAC. Data is latched within the input latch when either $\overline{CS}$ or $\overline{WR}$ is high. Taking $\overline{LD\_}$ high latches data into the DAC latches.

If $\overline{LD\_}$ is brought low when $\overline{WR}$ and $\overline{CS}$ are low, it must be held low for t_3 or longer after $\overline{WR}$ and $\overline{CS}$ are high (Figure 3).

Pulling the asynchronous $\overline{CLR}$ input low sets all DAC outputs to a nominal 0V, regardless of the state of $\overline{CS}$, $\overline{WR}$, and $\overline{LD\_}$. Taking $\overline{CLR}$ high latches 1000hex into all input latches and DAC latches.

Table 1. MAX547 DAC Addressing

A2	A1	A0	FUNCTION
0	0	0	DAC A input latch
0	0	1	DAC B input latch
0	1	0	DAC C input latch
0	1	1	DAC D input latch
1	0	0	DAC E input latch
1	0	1	DAC F input latch
1	1	0	DAC G input latch
1	1	1	DAC H input latch

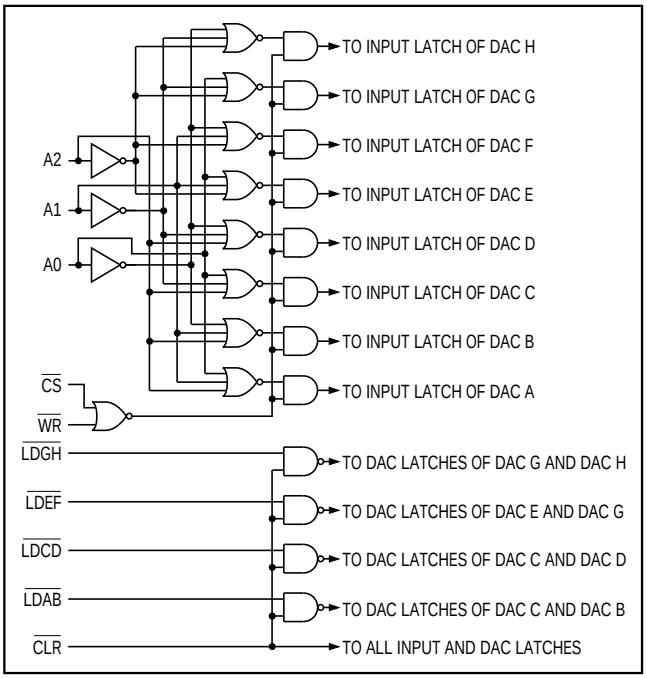
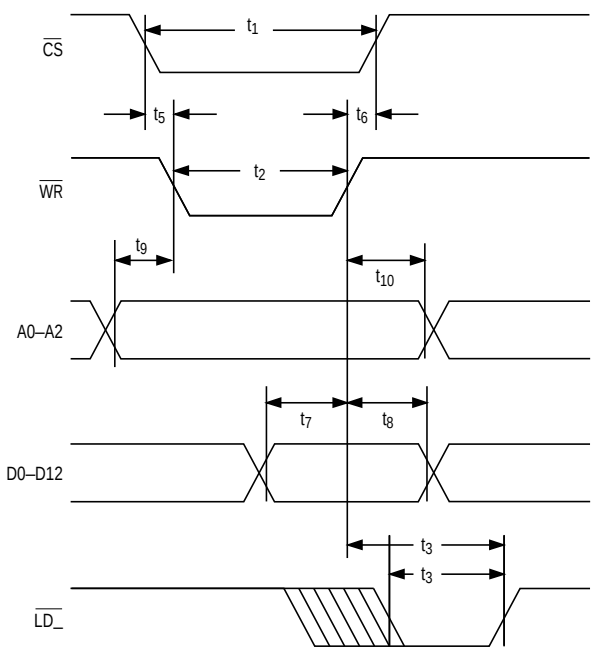


Figure 2. Input Control Logic

Table 2. Interface Truth Table

$\overline{CLR}$	$\overline{LD\_}$	$\overline{WR}$	$\overline{CS}$	FUNCTION
1	0	0	0	Both latches transparent
1	1	1	X	Both latches latched
1	1	X	1	Both latches latched
1	X	0	0	Input latch transparent
1	X	1	X	Input latch latched
1	X	X	1	Input latch latched
1	0	X	X	DAC latch transparent
0	X	X	X	All input and DAC latches at 1000hex, outputs at AGND_



NOTES:

1. ALL INPUT RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 5ns$.
2. MEASUREMENT REFERENCE LEVEL IS $(V_{INH} + V_{INL})/2$.
3. IF $\overline{LD\_}$ IS ACTIVATED WHILE $\overline{WR}$ IS LOW THEN $\overline{LD\_}$ MUST STAY LOW FOR t_3 OR LONGER AFTER $\overline{WR}$ GOES HIGH.

Figure 3. Write-Cycle Timing

Applications Information

Multiplying Operation

The MAX547 can be used for multiplying applications. Its reference accepts both DC and AC signals. The voltage at each REF_ input sets the full-scale output voltage for its respective DACs. Since the reference inputs accept only positive voltages, multiplying operation is limited to two quadrants. Do not bypass the reference inputs when applying AC signals to them. Refer to the graphs in the *Typical Operating Characteristics* for dynamic performance of the DACs and output buffers.

Digital Code and Analog Output Voltage

The MAX547 uses offset binary coding. A 13-bit twos-complement code can be converted to a 13-bit offset binary code by adding $2^{12} = 4096$.

Bipolar Output Voltage Range (AGND_ = 0V)

For symmetrical bipolar operation, tie AGND_ to the system ground. Table 3 shows the relationship between digital code and output voltage. The following paragraphs give a detailed explanation of this mode.

The DAC ladder output voltage (V_{DAC}) is multiplied by 2 and level shifted by the reference voltage, which is internally connected to the output amplifiers (Figure 1). Since the feedback resistors are the same size, the amplifier's output voltage is 2 times the voltage at its noninverting input, minus the reference voltage.

$$VOUT = 2(V_{DAC}) - REF\_$$

where V_{DAC} is the voltage at the amplifier's noninverting input (DAC ladder output voltage), and REF_ is the voltage applied to the reference input of the DAC.

With AGND_ connected to the system ground, the DAC ladder output voltage is:

$$V_{DAC} = \frac{D}{2^n}(REF\_) = \frac{D}{2^{13}}(REF\_)$$

where D is the numeric value of the DAC's binary input code and n is the DAC's resolution (13 bits). Replace V_{DAC} in the equation and calculate the output voltage.

$$VOUT\_ = 2\left(\frac{D}{2^{13}}\right)(REF\_) - REF\_$$

$$= REF\_\left(\frac{D}{2^{12}} - 1\right) = REF\_\left(\frac{D}{4096} - 1\right)$$

D ranges from 0 (2^0) to 8191 ($2^{13} - 1$).

$$1LSB = REF\_\left(\frac{1}{4096}\right)$$

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

Table 3. MAX547 Bipolar Code Table

(AGND_ = 0V)

INPUT	OUTPUT
1 1111 1111 1111	$+REF\_\left(\frac{4095}{4096}\right)$
1 0000 0000 0001	$+REF\_\left(\frac{1}{4096}\right)$
1 0000 0000 0000	0V
0 1111 1111 1111	$-REF\_\left(\frac{1}{4096}\right)$
0 0000 0000 0001	$-REF\_\left(\frac{4095}{4096}\right)$
0 0000 0000 0000	-REF_

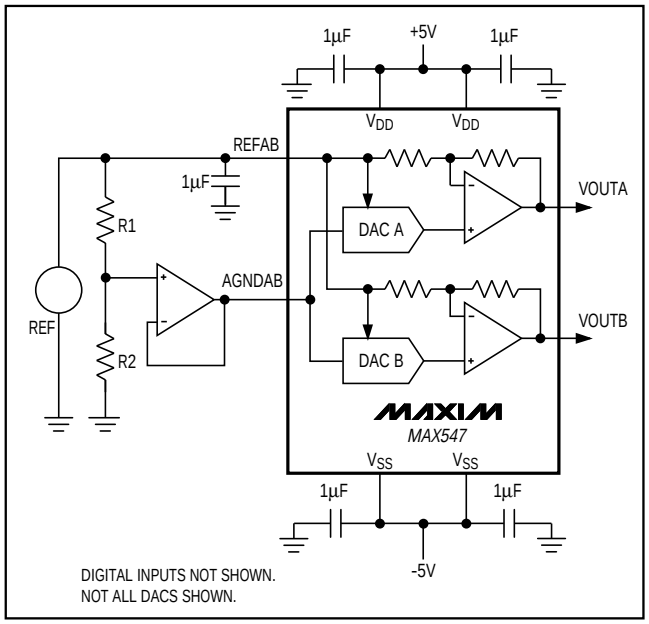


*Figure 4. Offsetting AGND_*

Positive Unipolar Output Voltage Range (AGND_ = REF_/2)

For positive unipolar output operation, set AGND_ to (REF_/2). For example, if you use Figure 4's circuit with, a 4.096V reference and offset AGND_ by 2.048V with matched resistors (R1 = R2) and an op amp, it results in a 0V to 4.0955V (nominal) unipolar output voltage, where 1LSB = 500µV. In general, the maximum current flowing out of any AGND_ pin is given by:

$$I_{AGND\_} = \left(\frac{REF\_ - AGND\_}{5k\Omega}\right)$$

Table 4. MAX547 Positive Unipolar Code Table

(AGND_ = $\frac{REF\_}{2}$)

INPUT	OUTPUT
1 1111 1111 1111	$+REF\_\left(\frac{8191}{8192}\right)$
1 0000 0000 0000	+REF_ /2
0 0000 0000 0000	0V

Customizing the Output Voltage Range

The AGND_ inputs can be offset by any voltage within the supply rails if the voltage at the referring REF_ input is higher than the voltage at the AGND_ input. Select the reference voltage and the voltage at AGND_ so the resulting output voltages do not come within ±0.6V of the supply rails. Figure 4's circuit shows one way to add positive offset to AGND_; make sure that the op amp used has sufficient current-sink capability to take up the remaining AGND_ current:

$$I_{AGND\_} = \left(\frac{REF\_ - AGND\_}{5k\Omega}\right)$$

Another way is to digitally offset AGND_ by connecting the output of one DAC to one or more AGND_ inputs. Do not connect a DAC output to its own AGND_ input.

Table 5 summarizes the relationship between the reference and AGND_ potentials and the output voltage in the different modes of operation.

Power-Supply Sequencing

The sequence in which the supply voltages come up is not critical. However, we recommend that on power-up, V_{SS} comes up first, V_{DD} next, followed by the reference voltages. If you use other sequences, limit the current into any reference pin to 10mA. Also, make sure that V_{SS} is never more than 300mV above ground. If there is a risk that this can occur at power-up, connect a Schottky diode between V_{SS} and GND, as shown in Figure 5. We recommend that you not power up the logic input pins before establishing the supply voltages. If this is not possible and the digital lines can drive more than 10mA, you should place current-limiting resistors (e.g., 470Ω) in series with the logic pins.

Reference Selection

If you want a ±2.5V full-scale output voltage swing, you can use the MAX873 reference. It operates from a single 5V supply and is specified to drive up to 10mA. Therefore, it can drive all four reference inputs simultaneously. Because the maximum load impedance can vary from 1.25kΩ to 12.5kΩ (four reference inputs in parallel), the reference load current ranges from 2mA to 0.2mA (1.8mA maximum load step). The MAX873's

Table 5. Reference, AGND_ and Output Relationships

PARAMETER	BIPOLAR OPERATION (AGND_ = 0V)	POSITIVE UNIPOLAR OPERATION (AGND_ = REF_/2)	CUSTOM OPERATION
Bipolar Zero Level, or Unipolar Mid-scale, (Code = 1000000000000)	AGND_ (=0V)	AGND_ $\left(=\frac{REF\_}{2}\right)$	AGND_
Differential Reference Voltage (V_{DR})	REF_	REF_/2	REF_ - AGND_
Negative Full-scale Output (Code = All 0s)	-REF_	0V	AGND_ - V_{DR}
Positive Full-Scale Output (Code = All 1s)	$\left(\frac{4095}{4096}\right)\left(REF\_\right)$	$\left(\frac{8191}{8192}\right)\left(REF\_\right)$	AGND_ + $\left(\frac{4095}{4096}\right)\left(V_{DR}\right)$
LSB Weight	$\frac{REF\_}{4096}$	$\left(\frac{REF\_}{8192}\right)$	$\frac{V_{DR}}{4096}$
VOUT_ as a Function of Digital Code (D, 0 to 8191)	$\left(\frac{D}{4096} - 1\right)\left(REF\_\right)$	$\left(\frac{D}{8192}\right)\left(REF\_\right)$	AGND_ + $\left(\frac{D}{4096} - 1\right)\left(V_{DR}\right)$

load regulation is specified to 20ppm/mA max over temperature, resulting in a maximum error of 36ppm (90µV). This corresponds to a maximum error caused by reference load regulation of only 0.147LSB [0.147LSB = 90µV/(5V/8192)LSB] over temperature.

If you want a ±4.096V full-scale output swing (1LSB = 1mV), you can use the calibrated, low-drift, low-dropout MAX676. Operating from a 5V supply, it is fully specified to drive two REF_ inputs with less than 60.4µV error (0.0604LSB) over temperature, caused by the maximum load step.

Reference Buffering

Another way to obtain high accuracy is to buffer a reference with an op amp. When driving all reference inputs simultaneously, keep the closed-loop output impedance of the op amp below 0.03Ω to ensure an error of less than 0.1LSB. The op amp must also drive the capacitive load (typically 500pF to 1200pF).

Each reference input can also be buffered separately by using the circuit in Figure 6. A reference load step caused by a digital transition only affects the DAC pair where the code transition occurs. It also allows the use of references with little drive capability. Keep the closed-loop output impedance of each op amp below 0.12Ω, to ensure an error of less than 0.1LSB. Figure 6 shows the op amp's inverting input directly connected to the MAX547's reference terminal. This eliminates the influence of board lead resistance by sensing the voltage with a low-current path sense line directly at the reference input.

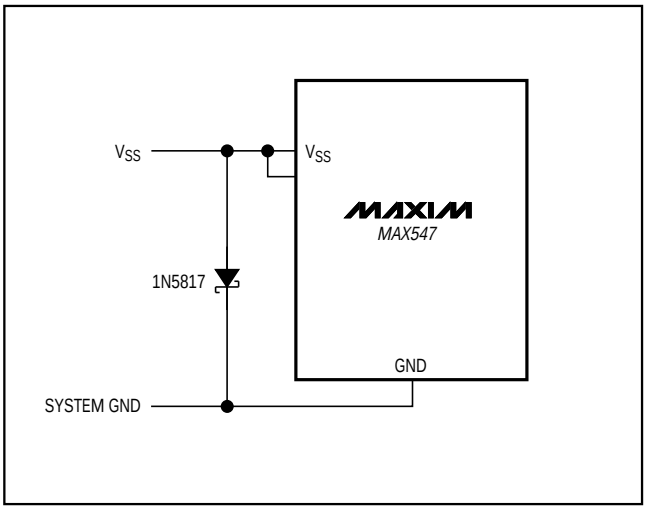


Figure 5. Optional Schottky Diode between V_{SS} and GND

Adding feedback resistors to individual reference buffer amplifiers enables different reference voltages to be generated from a single reference.

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

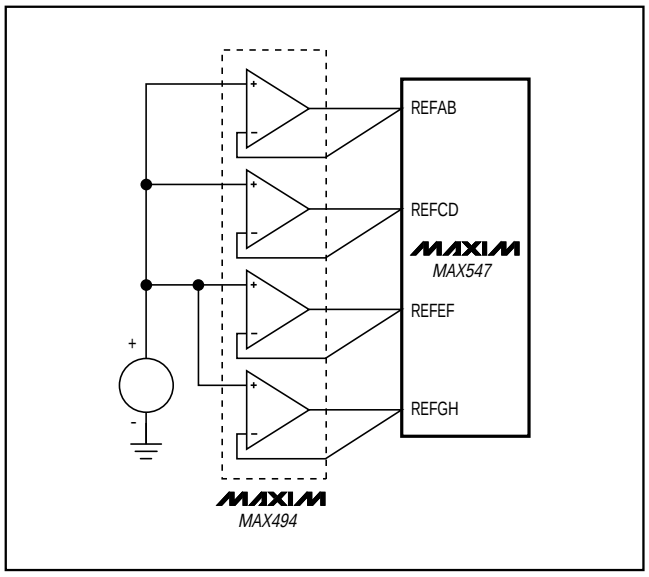


Figure 6. Reference Buffering

Power-Supply Bypassing and Ground Management

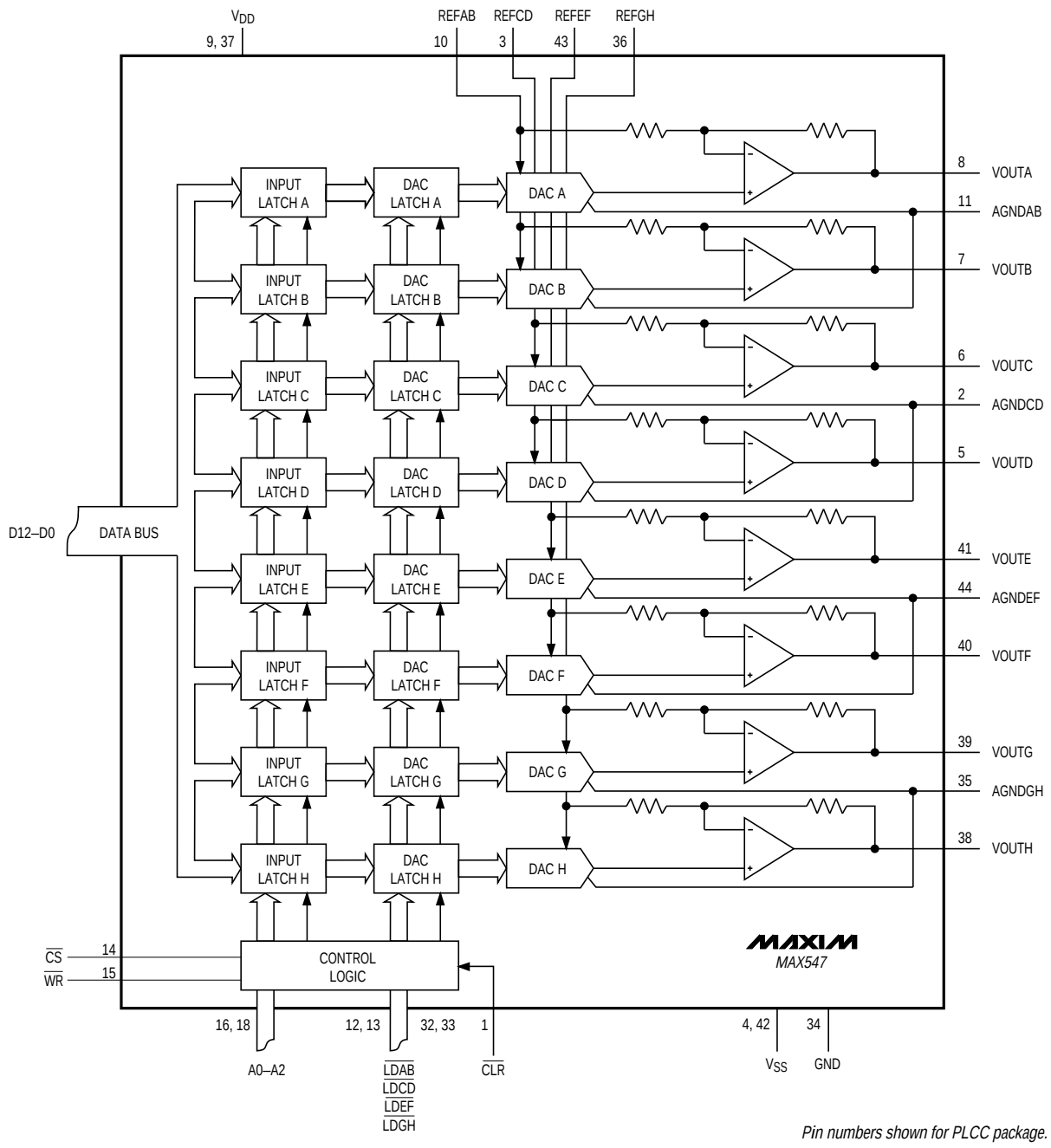
For optimum performance, use a multilayer PC board with an unbroken analog ground. For normal operation, when all AGND_ pins are at the same potential, connect the four AGND_ pins directly to the ground plane or connect them together in a “star” configuration. The center of this star point is a good location to connect the digital system ground with the analog ground.

If you are using a single common reference voltage, you can connect the reference inputs together using a “star” configuration. If you are using DC reference voltages, bypass each reference input with a 0.1µF to 1µF capacitor to AGND_.

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX547AEQH	-40°C to +85°C	44 PLCC	±2
MAX547BEQH	-40°C to +85°C	44 PLCC	±4
MAX547AEMH	-40°C to +85°C	44 Plastic FP	±2
MAX547BEMH	-40°C to +85°C	44 Plastic FP	±4

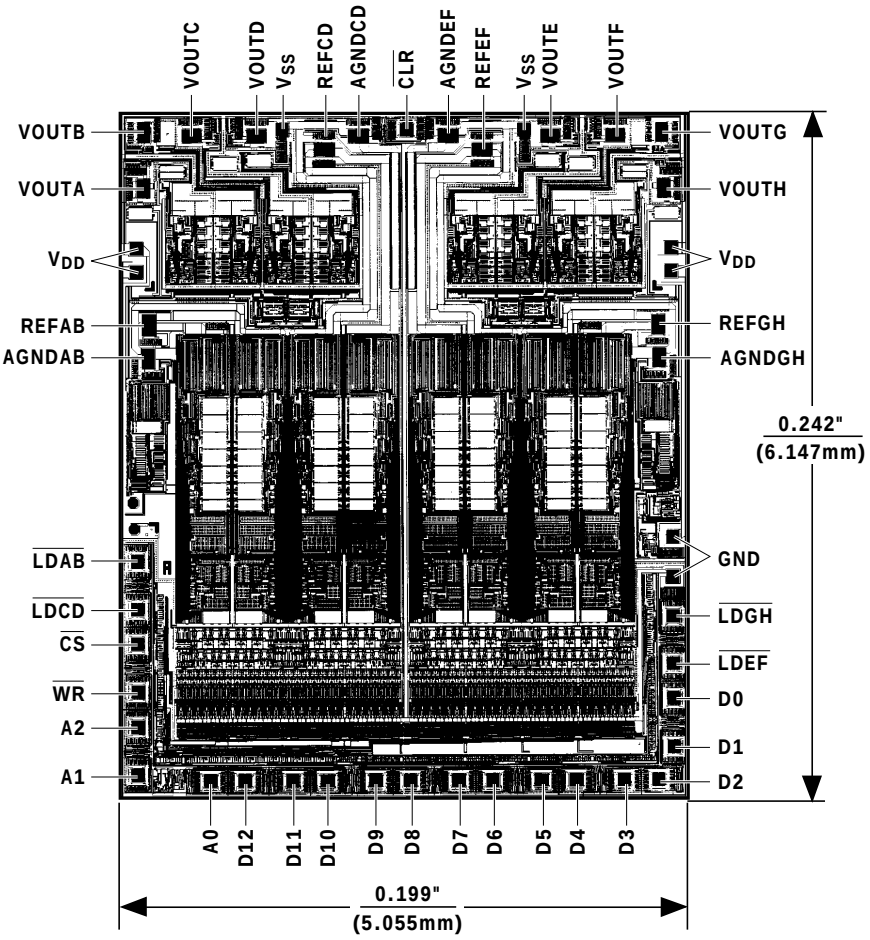
Functional Diagram



Pin numbers shown for PLCC package.

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

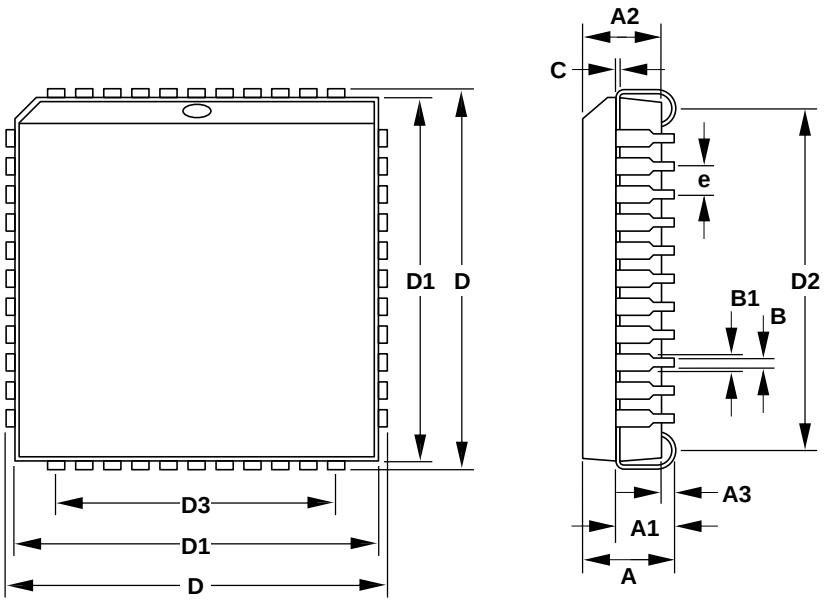
Chip Topography



TRANSISTOR COUNT: 8987

SUBSTRATE CONNECTED TO V_{DD}

Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.100	0.110	2.54	2.79
A2	0.145	0.156	3.68	3.96
A3	0.020	–	0.51	–
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
D	0.685	0.695	17.40	17.65
D1	0.650	0.655	16.51	16.64
D2	0.590	0.630	14.99	16.00
D3	0.500 REF		12.70 REF	
e	0.050 REF		1.27 REF	

21-350A

44-PIN PLASTIC LEADED CHIP CARRIER PACKAGE

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

4.11 MAX764

19-0176; Rev 0; 6/94

Evaluation Kit Available

-5V/-12V/-15V or Adjustable, High-Efficiency, Low IQ DC-DC Inverters

General Description

The MAX764/MAX765/MAX766 inverting switching regulators are highly efficient over a wide range of load currents, delivering up to 1.5W. A unique, current-limited, pulse-frequency-modulated (PFM) control scheme combines the benefits of traditional PFM converters with the benefits of pulse-width-modulated (PWM) converters. Like PWM converters, the MAX764/MAX765/MAX766 are highly efficient at heavy loads. Yet because they are PFM devices, they use less than 120µA of supply current (vs. 2mA to 10mA for a PWM device).

The input voltage range is 3V to 16V. The output voltage is preset at -5V (MAX764), -12V (MAX765), or -15V (MAX766); it can also be adjusted from -1V to -16V using two external resistors (Dual Mode™). The maximum operating V_{IN} - V_{OUT} differential is 20V.

These devices use miniature external components; their high switching frequencies (up to 300kHz) allow for less than 5mm diameter surface-mount magnetics. A standard 47µH inductor is ideal for most applications, so no magnetics design is necessary.

An internal power MOSFET makes the MAX764/MAX765/MAX766 ideal for minimum component count, low- and medium-power applications. For increased output drive capability or higher output voltages, use the MAX774/MAX775/MAX776 or MAX1774, which drive an external power P-channel MOSFET for loads up to 5W.

Applications

LCD-Bias Generators
Portable Instruments
LAN Adapters
Remote Data-Acquisition Systems
Battery-Powered Applications

Features

- **High Efficiency for a Wide Range of Load Currents**
- **250mA Output Current**
- **120µA Max Supply Current**
- **5µA Max Shutdown Current**
- **3V to 16V Input Voltage Range**
- **-5V (MAX764), -12V (MAX765), -15V (MAX766), or Adjustable Output from -1V to -16V**
- **Current-Limited PFM Control Scheme**
- **300kHz Switching Frequency**
- **Internal, P-Channel Power MOSFET**

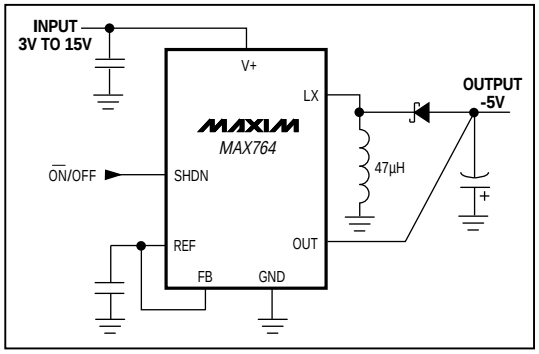
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX764CPA	0°C to +70°C	8 Plastic DIP
MAX764CSA	0°C to +70°C	8 SO
MAX764C/D	0°C to +70°C	Dice*
MAX764EPA	-40°C to +85°C	8 Plastic DIP
MAX764ESA	-40°C to +85°C	8 SO
MAX764MJA	-55°C to +125°C	8 CERDIP**
MAX765CPA	0°C to +70°C	8 Plastic DIP
MAX765CSA	0°C to +70°C	8 SO
MAX765C/D	0°C to +70°C	Dice*
MAX765EPA	-40°C to +85°C	8 Plastic DIP
MAX765ESA	-40°C to +85°C	8 SO
MAX765MJA	-55°C to +125°C	8 CERDIP**

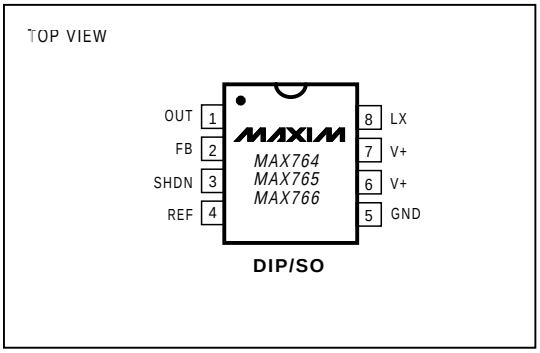
Ordering Information continued on last page.

** Dice are tested at T_A = +25°C, DC parameters only.*
***Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



Pin Configuration



-5V/-12V/-15V or Adjustable, High-Efficiency, Low IQ DC-DC Inverters

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +17V
OUT to GND .....+0.5V to -17V
Maximum Differential (V+ to OUT) .....+21V
REF, SHDN, FB to GND .....-0.3V to (V+ + 0.3V)
LX to V+ .....+0.3V to -21V
LX Peak Current 1.5A
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges
MAX76_C_A .....0°C to +70°C
MAX76_E_A .....-40°C to +85°C
MAX76_MJA .....-55°C to +125°C
Maximum Junction Temperatures
MAX76_C_A/E_A .....+150°C
MAX76_MJA .....+175°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, I_{LOAD} = 0mA, C_{REF} = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V+ Input Voltage Range	V+	MAX76_C/E		3.0		16.0	V
		MAX76_M		3.5			
Supply Current	I_S	V+ = 16V, SHDN < 0.4V			90	120	µA
Shutdown Current	I_{SHDN}	V+ = 16V, SHDN > 1.6V			2		
		V+ = 10V, SHDN > 1.6V			1	5	
FB Trip Point		3V ≤ V+ ≤ 16V		-10		10	mV
FB Input Current	I_{FB}	MAX76_C				±50	nA
		MAX76_E				±70	
		MAX76_M				±90	
Output Current and Voltage (Note 1)	I_{OUT}	MAX764, -4.8V ≤ V_{OUT} ≤ 5.2V		150	260		mA
		MAX765C/E, -11.52V ≤ V_{OUT} ≤ 12.48V		68	120		
		MAX765M, -11.52V ≤ V_{OUT} ≤ 12.48V		50	120		
		MAX766, -14.40V ≤ V_{OUT} ≤ -15.60V		35	105		
Reference Voltage	V_{REF}	MAX76_C		1.4700	1.5	1.5300	V
		MAX76_E		1.4625	1.5	1.5375	
		MAX76_M		1.4550	1.5	1.5450	
REF Load Regulation		0µA ≤ I_{REF} ≤ 100µA	MAX76_C/E		4	10	mV
			MAX76_M		4	15	
REF Line Regulation		3V ≤ V+ ≤ 16V			40	100	µV/V
Load Regulation (Note 2)		0mA ≤ I_{LOAD} ≤ 100mA			0.008		%/mA
Line Regulation (Note 2)		4V ≤ V+ ≤ 6V			0.12		%/V
Efficiency (Note 2)		10mA ≤ I_{LOAD} ≤ 100mA, V_{IN} = 5V	V_{OUT} = -5V		80		%
			V_{OUT} = -15V		82		
SHDN Leakage Current		V+ = 16V, SHDN = 0V or V+				±1	µA
SHDN Input Voltage High	V_{IH}	3V ≤ V+ ≤ 16V		1.6			V
SHDN Input Voltage Low	V_{IL}	3V ≤ V+ ≤ 16V				0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, I_{LOAD} = 0mA, C_{REF} = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LX Leakage Current		|LX| + (V+) ≤ 20V	MAX76_C			±5	µA
			MAX76_E			±10	
			MAX76_M			±30	
LX On-Resistance		$\|V_{OUT}\|$ + (V+) ≥ 10V			1.4	2.5	Ω
Peak Current at LX	I_{PEAK}	$\|V_{OUT}\|$ + (V+) ≥ 10V		0.5	0.75		A
Maximum Switch On-Time	t_{ON}			12	16	20	µs
Minimum Switch Off-Time	t_{OFF}			1.8	2.3	2.8	µs

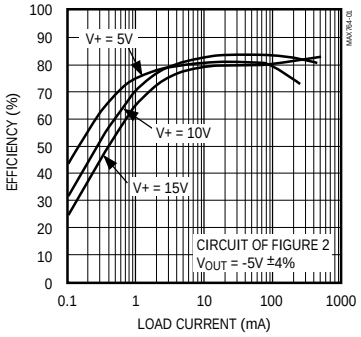
Note 1: See Maximum Output Current vs. Supply Voltage graph in the *Typical Operating Characteristics.* Guarantees are based on correlation to switch on-time, switch off-time, on-resistance, and peak current rating.

Note 2: Circuit of Figure 2.

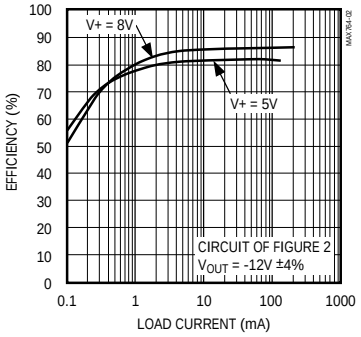
Typical Operating Characteristics

(V+ = 5V, V_{OUT} = -5V, T_A = +25°C, unless otherwise noted.)

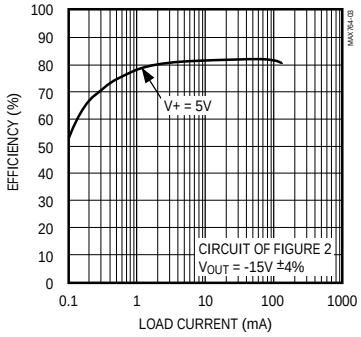
MAX764
EFFICIENCY vs. LOAD CURRENT



MAX765
EFFICIENCY vs. LOAD CURRENT



MAX766
EFFICIENCY vs. LOAD CURRENT

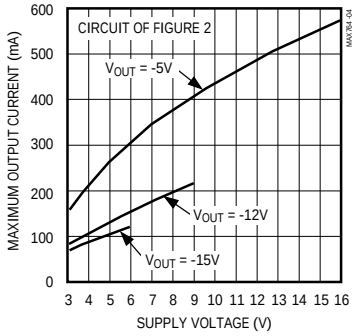


-5V/-12V/-15V or Adjustable, High-Efficiency, Low IQ DC-DC Inverters

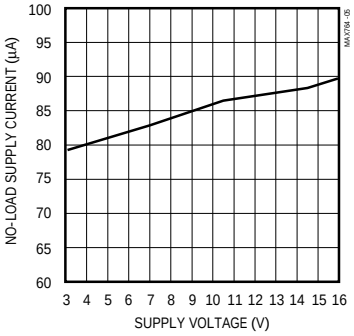
Typical Operating Characteristics (continued)

(V+ = 5V, V_{OUT} = -5V, T_A = +25°C, unless otherwise noted.)

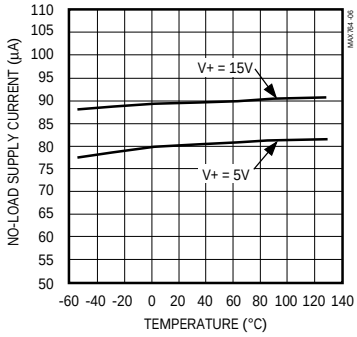
MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



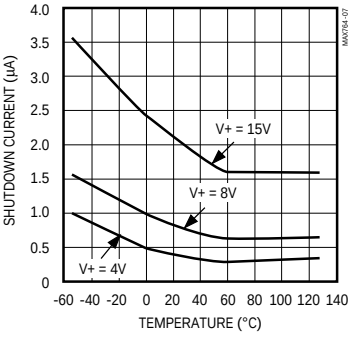
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



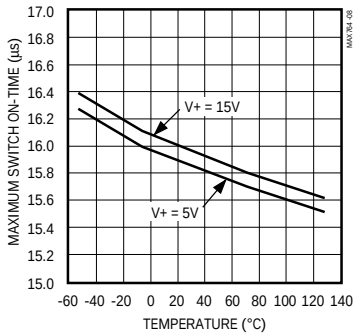
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



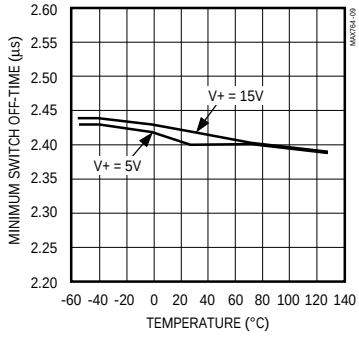
SHUTDOWN CURRENT vs. TEMPERATURE



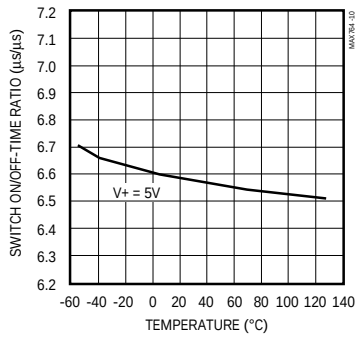
MAXIMUM SWITCH ON-TIME vs. TEMPERATURE



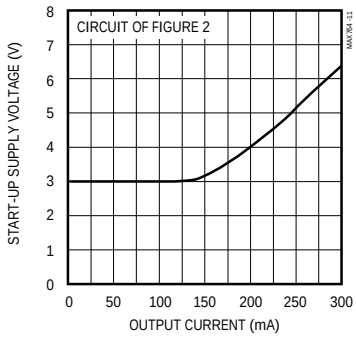
MINIMUM SWITCH OFF-TIME vs. TEMPERATURE



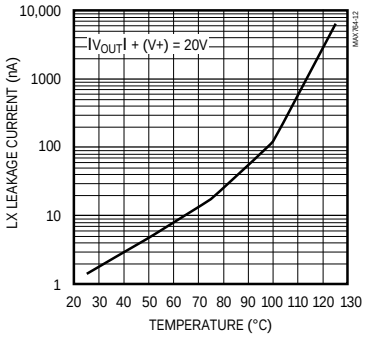
SWITCH ON/OFF-TIME RATIO vs. TEMPERATURE



START-UP SUPPLY VOLTAGE vs. OUTPUT CURRENT



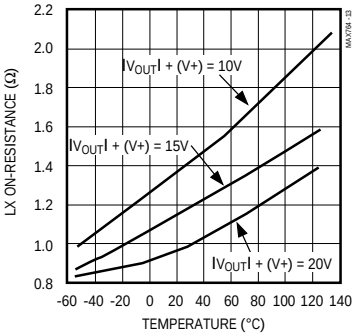
LX LEAKAGE CURRENT vs. TEMPERATURE



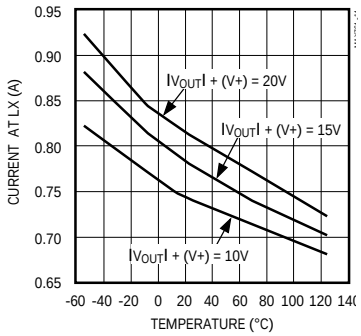
Typical Operating Characteristics (continued)

(V+ = 5V, V_{OUT} = -5V, T_A = +25°C, unless otherwise noted.)

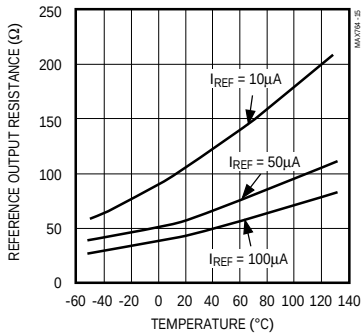
LX ON-RESISTANCE vs. TEMPERATURE



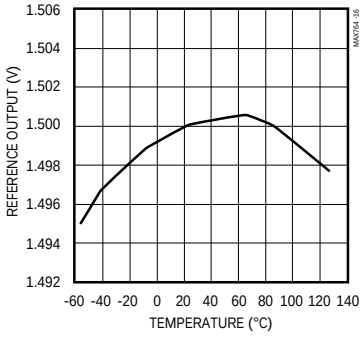
PEAK CURRENT AT LX vs. TEMPERATURE



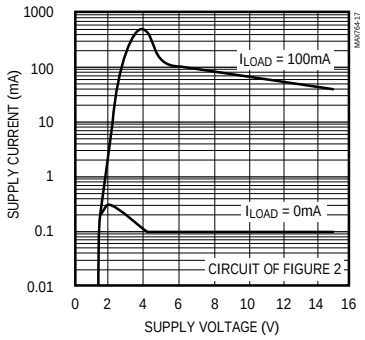
REFERENCE OUTPUT RESISTANCE vs. TEMPERATURE



REFERENCE OUTPUT vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE

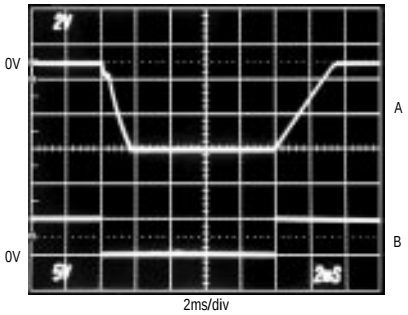


-5V/-12V/-15V or Adjustable, High-Efficiency, Low IQ DC-DC Inverters

Typical Operating Characteristics (continued)

(V+ = 5V, V_{OUT} = -5V, T_A = +25°C, unless otherwise noted.)

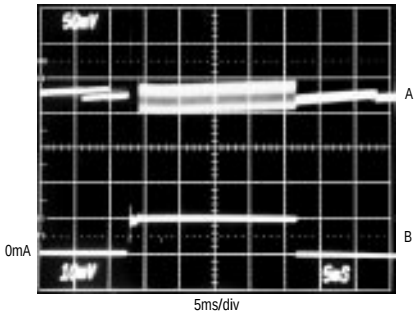
TIME TO ENTER/EXIT SHUTDOWN



2ms/div

CIRCUIT OF FIGURE 2, V+ = 5V, I_{LOAD} = 100mA, V_{OUT} = -5V
A: V_{OUT}, 2V/div
B: SHUTDOWN PULSE, 0V TO 5V, 5V/div

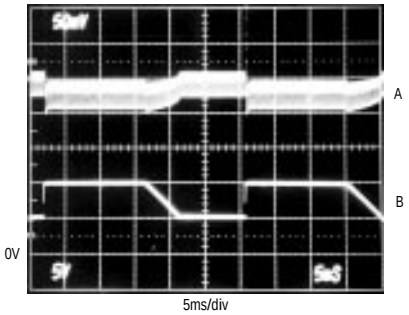
LOAD-TRANSIENT RESPONSE



5ms/div

CIRCUIT OF FIGURE 2, V+ = 5V, V_{OUT} = -5V
A: V_{OUT}, 50mV/div, AC-COUPLED
B: I_{LOAD}, 0mA TO 100mA, 100mA/div

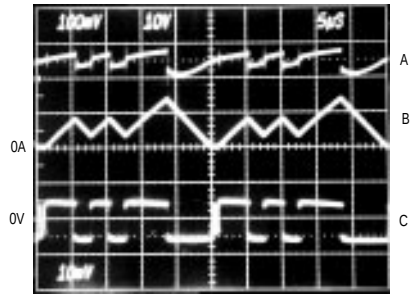
LINE-TRANSIENT RESPONSE



5ms/div

CIRCUIT OF FIGURE 2, V_{OUT} = -5V, I_{LOAD} = 100mA
A: V_{OUT}, 50mV/div, AC-COUPLED
B: V+, 5V TO 10V, 5V/div

DISCONTINUOUS CONDUCTION AT HALF AND FULL CURRENT LIMIT



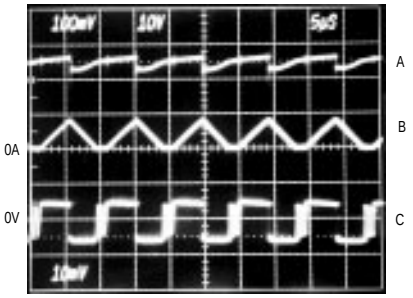
5µs/div

CIRCUIT OF FIGURE 2, V+ = 5V, V_{OUT} = -5V, I_{LOAD} = 140mA
A: OUTPUT RIPPLE, 100mV/div
B: INDUCTOR CURRENT, 500mA/div
C: LX WAVEFORM, 10V/div

Typical Operating Characteristics (continued)

(V+ = 5V, V_{OUT} = -5V, T_A = +25°C, unless otherwise noted.)

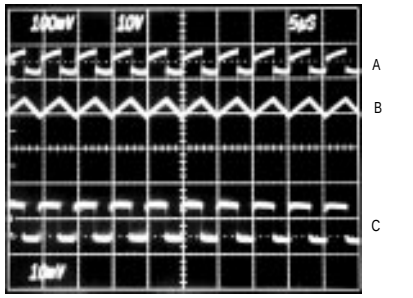
DISCONTINUOUS CONDUCTION AT HALF CURRENT LIMIT



5µs/div

CIRCUIT OF FIGURE 2, V+ = 5V, V_{OUT} = -5V, I_{LOAD} = 80mA
A: OUTPUT RIPPLE, 100mV/div
B: INDUCTOR CURRENT, 500mA/div
C: LX WAVEFORM, 10V/div

CONTINUOUS CONDUCTION AT FULL CURRENT LIMIT



5µs/div

CIRCUIT OF FIGURE 2, V+ = 5V, V_{OUT} = -5V, I_{LOAD} = 240mA
A: OUTPUT RIPPLE, 100mV/div
B: INDUCTOR CURRENT, 500mA/div
C: LX WAVEFORM, 10V/div

Pin Description

PIN	NAME	FUNCTION
1	OUT	Sense Input for Fixed-Output Operation (V_{FB} = V_{REF}). OUT must be connected to V_{OUT}.
2	FB	Feedback Input. Connect FB to REF to use the internal voltage divider for a preset output. For adjustable-output operation, use an external voltage divider, as described in the section *Setting the Output Voltage.*
3	SHDN	Active-High Shutdown Input. With SHDN high, the part is in shutdown mode and the supply current is less than 5µA. Connect to ground for normal operation.
4	REF	1.5V Reference Output that can source 100µA for external loads. Bypass to ground with a 0.1µF capacitor.
5	GND	Ground
6, 7	V+	Positive Power-Supply Input. Must be tied together. **Place a 0.1µF input bypass capacitor as close to the V+ and GND pins as possible.**
8	LX	Drain of the Internal P-Channel Power MOSFET. LX has a peak current limit of 0.75A.

-5V/-12V/-15V or Adjustable, High-Efficiency, Low IQ DC-DC Inverters

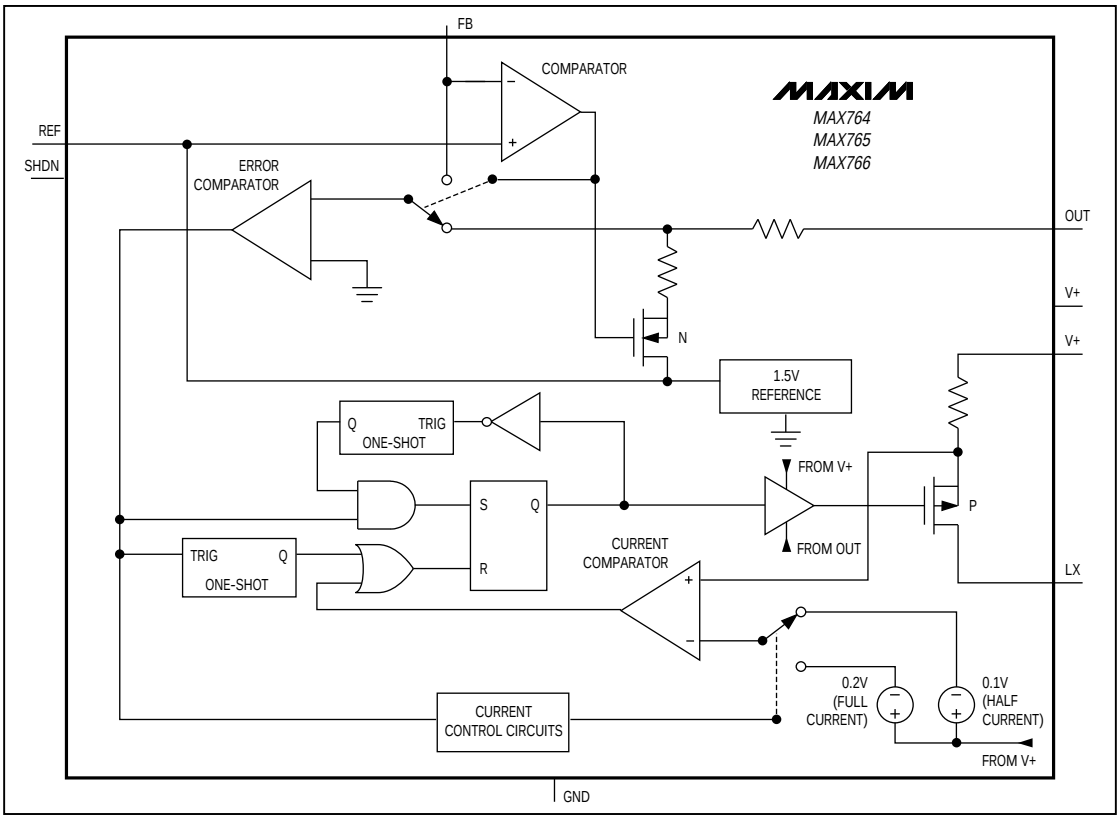


Figure 1. Block Diagram

Detailed Description

Operating Principle

The MAX764/MAX765/MAX766 are BiCMOS, inverting, switch-mode power supplies that provide fixed outputs of -5V, -12V, and -15V, respectively; they can also be set to any desired output voltage using an external resistor divider. Their unique control scheme combines the advantages of pulse-frequency modulation (pulse skipping) and pulse-width modulation (continuous pulsing). The internal P-channel power MOSFET allows peak currents of 0.75A, increasing the output current capability over previous pulse-frequency-modulation (PFM) devices. Figure 1 shows the MAX764/MAX765/MAX766 block diagram.

The MAX764/MAX765/MAX766 offer three main improvements over prior solutions:

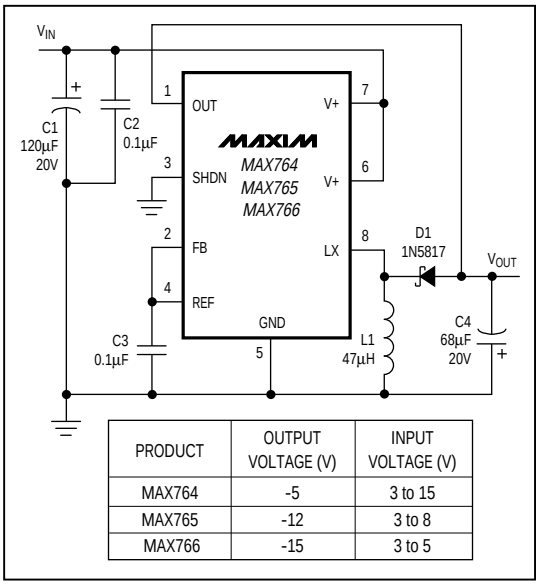
1) They can operate with miniature (less than 5mm diameter) surface-mount inductors, because of their 300kHz switching frequency.
2) The current-limited PFM control scheme allows efficiencies exceeding 80% over a wide range of load currents.
3) Maximum quiescent supply current is only 120µA.

Figures 2 and 3 show the standard application circuits for these devices. In these configurations, the IC is powered from the total differential voltage between the input (V+) and output (V_{OUT}). The principal benefit of this arrangement is that it applies the largest available signal to the gate of the internal P-channel power MOSFET. This increased gate drive lowers switch on-resistance and increases DC-DC converter efficiency.

Since the voltage on the LX pin swings from V+ (when the switch is ON) to $|V_{OUT}|$ plus a diode drop (when the

switch is OFF), the range of input and output voltages is limited to a 21V absolute maximum differential voltage.

When output voltages more negative than -16V are required, substitute the MAX764/MAX765/MAX766 with Maxim's MAX774/MAX775/MAX776 or MAX1774, which use an external switch.



PRODUCT	OUTPUT VOLTAGE (V)	INPUT VOLTAGE (V)
MAX764	-5	3 to 15
MAX765	-12	3 to 8
MAX766	-15	3 to 5

Figure 2. Fixed Output Voltage Operation

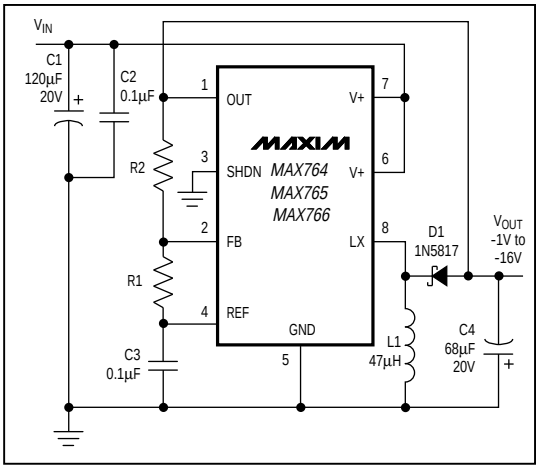


Figure 3. Adjustable Output Voltage Operation

PFM Control Scheme

The MAX764/MAX765/MAX766 use a proprietary, current-limited PFM control scheme that blends the best features of PFM and PWM devices. It combines the ultra-low supply currents of traditional pulse-skipping PFM converters with the high full-load efficiencies of current-mode pulse-width modulation (PWM) converters. This control scheme allows the devices to achieve high efficiencies over a wide range of loads, while the current-sense function and high operating frequency allow the use of miniature external components.

As with traditional PFM converters, the internal power MOSFET is turned on when the voltage comparator senses that the output is out of regulation (Figure 1). However, unlike traditional PFM converters, switching is accomplished through the combination of a peak current limit and a pair of one-shots that set the maximum on-time (16µs) and minimum off-time (2.3µs) for the switch. Once off, the minimum off-time one-shot holds the switch off for 2.3µs. After this minimum time, the switch either 1) stays off if the output is in regulation, or 2) turns on again if the output is out of regulation.

The MAX764/MAX765/MAX766 limit the peak inductor current, which allows them to run in continuous-conduction mode and maintain high efficiency with heavy loads. (See the photo Continuous Conduction at Full Current Limit in the *Typical Operating Characteristics*.) This current-limiting feature is a key component of the control circuitry. Once turned on, the switch stays on until either 1) the maximum on-time one shot turns it off (16µs later), or 2) the current limit is reached.

To increase light-load efficiency, the current limit is set to half the peak current limit for the first two pulses. If those pulses bring the output voltage into regulation, the voltage comparator holds the MOSFET off and the current limit remains at half the peak current limit. If the output voltage is still out of regulation after two pulses, the current limit is raised to its 0.75A peak for the next pulse. (See the photo Discontinuous Conduction at Half and Full Current Limit in the *Typical Operating Characteristics*.)

Shutdown Mode

When SHDN is high, the MAX764/MAX765/MAX766 enter a shutdown mode in which the supply current drops to less than 5µA. In this mode, the internal biasing circuitry (including the reference) is turned off and OUT discharges to ground. SHDN is a TTL/CMOS-logic level input. Connect SHDN to GND for normal operation. With a current-limited supply, power-up the device while unloaded or in shutdown mode (hold SHDN high until V+ exceeds 3.0V) to save power and reduce power-up current surges. (See the Supply Current vs. Supply Voltage graph in the *Typical Operating Characteristics*.)

Modes of Operation

When delivering high output currents, the MAX764/MAX765/MAX766 operate in continuous-conduction mode. In this mode, current always flows in the inductor, and the control circuit adjusts the duty-cycle of the switch on a cycle-by-cycle basis to maintain regulation without exceeding the switch-current capability. This provides excellent load-transient response and high efficiency.

In discontinuous-conduction mode, current through the inductor starts at zero, rises to a peak value, then ramps down to zero on each cycle. Although efficiency is still excellent, the output ripple may increase slightly.

Design Procedure

Setting the Output Voltage

The MAX764/MAX765/MAX766's output voltage can be adjusted from -1.0V to -16V using external resistors R1 and R2, configured as shown in Figure 3. For adjustable-output operation, select feedback resistor R1 = 150kΩ. R2 is given by:

$$R2 = (R1)\left|\frac{V_{OUT}}{V_{REF}}\right|$$

where V_{REF} = 1.5V.

For fixed-output operation, tie FB to REF.

Inductor Selection

In both continuous- and discontinuous-conduction modes, practical inductor values range from 22µH to 68µH. If the inductor value is too low, the current in the coil will ramp up to a high level before the current-limit comparator can turn off the switch, wasting power and reducing efficiency. The maximum inductor value is not critical. A 47µH inductor is ideal for most applications.

For highest efficiency, use a coil with low DC resistance, preferably under 100mΩ. To minimize radiated noise, use a toroid, pot core, or shielded coil. Inductors with a ferrite core or equivalent are recommended. The inductor's incremental saturation-current rating should be greater than the 0.75A peak current limit. It is generally acceptable to bias the inductor into saturation by approximately 20% (the point where the inductance is 20% below the nominal value).

Table 1 lists inductor types and suppliers for various applications. The listed surface-mount inductors' efficiencies are nearly equivalent to those of the larger-size through-hole inductors.

Diode Selection

The MAX764/MAX765/MAX766's high switching frequency demands a high-speed rectifier. Use a Schottky diode with a 0.75A average current rating, such as the 1N5817 or 1N5818. High leakage currents may make Schottky diodes inadequate for high-temperature and light-load applications. In these cases you can use high-speed silicon diodes, such as the MUR105 or the EC11FS1. At heavy loads and high temperatures, the benefits of a Schottky diode's low forward voltage may outweigh the disadvantages of its high leakage current.

Capacitor Selection

Output Filter Capacitor

The primary criterion for selecting the output filter capacitor (C4) is low effective series resistance (ESR). The product of the inductor-current variation and the output filter capacitor's ESR determines the amplitude of the high-frequency ripple seen on the output voltage. A 68µF, 20V Sanyo OS-CON capacitor with ESR = 45mΩ (SA series) typically provides 50mV ripple when converting from 5V to -5V at 150mA.

Output filter capacitor ESR also affects efficiency. To obtain optimum performance, use a 68µF or larger, low-ESR capacitor with a voltage rating of at least 20V. The smallest low-ESR surface-mount tantalum capacitors currently available are from the Sprague 595D series. Sanyo OS-CON series organic semiconductors and AVX TPS series tantalum capacitors also exhibit very low ESR. OS-CON capacitors are particularly useful at low temperatures. Table 1 lists some suppliers of low-ESR capacitors.

For best results when using capacitors other than those suggested in Table 1 (or their equivalents), increase the output filter capacitor's size or use capacitators in parallel to reduce ESR.

Input Bypass Capacitor

The input bypass capacitor, C1, reduces peak currents drawn from the voltage source and reduces the amount of noise at the voltage source caused by the switching action of the MAX764–MAX766. The input voltage source impedance determines the size of the capacitor required at the V+ input. As with the output filter capacitor, a low-ESR capacitor is highly recommended. For output currents up to 250mA, a 100µF to 120µF capacitor with a voltage rating of at least 20V (C1) in parallel with a 0.1µF capacitor (C2) is adequate in most applications. **C2 must be placed as close as possible to the V+ and GND pins.**

Reference Capacitor

Bypass REF with a 0.1µF capacitor (C3). The REF output can source up to 100µA for external loads.

Layout Considerations

Proper PC board layout is essential to reduce noise generated by high current levels and fast switching waveforms. Minimize ground noise by connecting GND, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point (star ground configuration). Also minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise. In particular, keep the traces connected to FB and LX short. **C2 must be placed as close as possible to the V+ and GND pins.** If an external resistor divider is used (Figure 3), the trace from FB to the resistors must be extremely short.

Table 1. Component Suppliers

PRODUCTION METHOD	INDUCTORS	CAPACITORS	DIODES
Surface Mount	Sumida CD75/105 series Coiltronics CTX series Coilcraft DT/D03316 series	Matsuo 267 series Sprague 595D/293D series AVX TPS series	Nihon EC10QS02L (Schottky) EC11FS1 (high-speed silicon)
Miniature Through-Hole	Sumida RCH895 series	Sanyo OS-CON series (very low ESR)	Motorola 1N5817, 1N5818, (Schottky) MUR105 (high-speed silicon)
Low-Cost Through-Hole	Renco RL1284 series	Nichicon PL series	

SUPPLIER	PHONE	FAX
AVX	USA: (803) 448-9411	(803) 448-1943
Coilcraft	USA: (708) 639-6400	(708) 639-1469
Coiltronics	USA: (407) 241-7876	(407) 241-9339
Matsuo	USA: (714) 969-2491 Japan: 81-6-337-6450	(714) 960-6492 81-6-337-6456
Motorola	USA: (800) 521-6274	(602) 952-4190
Nichicon	USA: (708) 843-7500 Japan: 81-7-5231-8461	(708) 843-2798 81-7-5256-4158
Nihon	USA: (805) 867-2555 Japan: 81-3-3494-7411	(805) 867-2556 81-3-3494-7414
Renco	USA: (516) 586-5566	(516) 586-5562
Sanyo OS-CON	USA: (619) 661-6835 Japan: 81-7-2070-1005	(619) 661-1055 81-7-2070-1174
Sprague Electric Co.	USA: (603) 224-1961	(603) 224-1430
Sumida	USA: (708) 956-0666 Japan: 81-3-3607-5111	(708) 956-0702 81-3-3607-5144

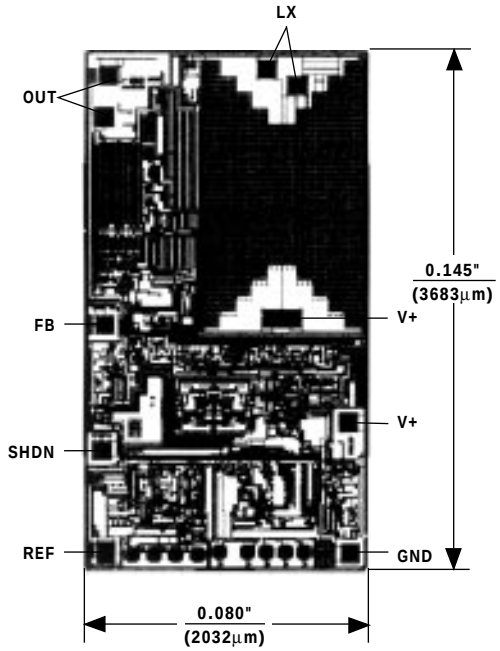
-5V/-12V/-15V or Adjustable, High-Efficiency, Low IQ DC-DC Inverters

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX766CPA	0°C to +70°C	8 Plastic DIP
MAX766CSA	0°C to +70°C	8 SO
MAX766C/D	0°C to +70°C	Dice*
MAX766EPA	-40°C to +85°C	8 Plastic DIP
MAX766ESA	-40°C to +85°C	8 SO
MAX766MJA	-55°C to +125°C	8 CERDIP**

** Dice are tested at T_A = +25°C, DC parameters only.*
***Contact factory for availability and processing to MIL-STD-883.*

_____Chip Topography



TRANSISTOR COUNT: 443
SUBSTRATE CONNECTED TO V+