iSHELL
ARRAY CONTROLLER

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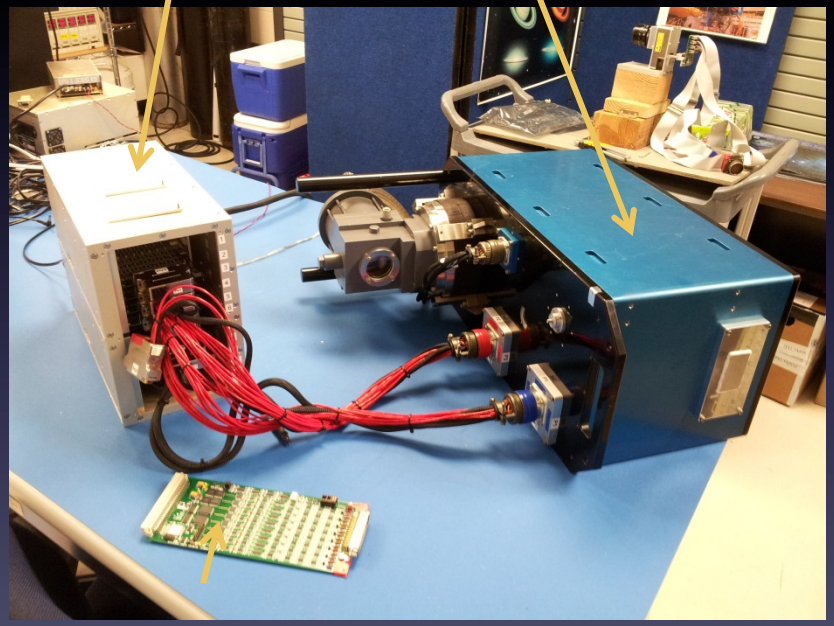
General Description

- The IARC controller is a customized version of the Astronomical Research Cameras (ARC) gen III controllers and software for H2RG (science) and Aladdin (guider) arrays
- IARC will be used for NSFCAM, SpeX, and iSHELL



For controller selection & evaluation details, see:
"Evaluation of the ARC Controller for the NASA IRTF.pdf"

H2RG Controller Requirements

- Support 2048x2048 array readouts with 32 channels
- Support full frame readouts at 300k pixel/sec
- Sum a minimum of 64K 16-bit readouts
- Adjustable Frame Rate: 300k, 200k, and 100k pixel/sec
- Well Depth > 50,000 e-.
- Noise Requirements:

Readout Mode	Noise Requirement / Goal (RMS)	NSFCAM Results	Conditions
Slow Readout, Overhead < 30s	< 5e- / 2e-	3.1 e-	NDR=16, Readout=13s
Standard Readout, Overhead < 1s	< 15e-	12.8 e-	NDR=1, Readout=0.8s
*Fast Readout, Overhead < 0.1s	< 100e- / 30e-	17.7 e-	NDR=1, Readout=0.43s

Aladdin Controller Requirements for Slit Viewer

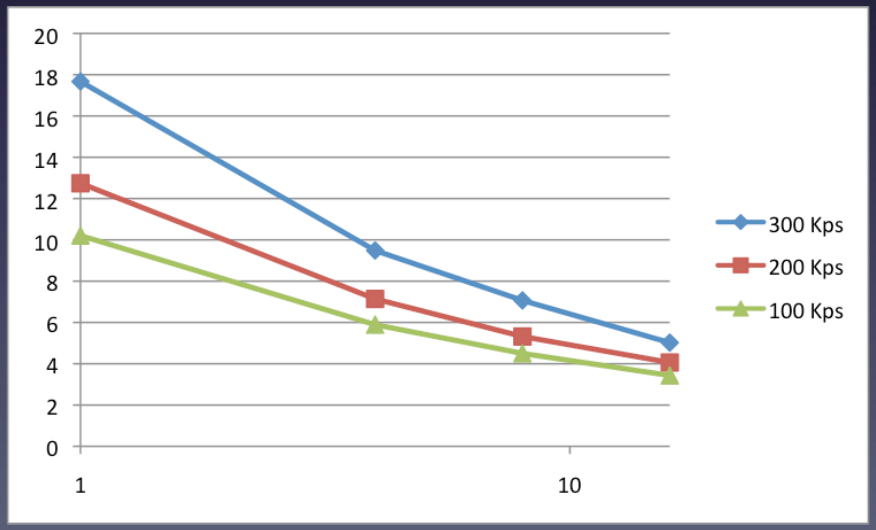
- Support 512x512, 8 channels, at 270k pixels/sec
- Summing a minimum of 64K 16-bit readouts
- Noise requirements less stringent that for H2RG

Readout Mode	Noise Requirement / Goal	Conditions
Slow Readout, Overhead < 5.0s	< 30e RMS, < 20e RMS goal	Coadd=1, FR=0.24s, NDR=20
Standard Readout, Overhead < 1.0s	< 70e RMS, < 20e RMS goal	Coadd=1FR=0.24s, NDR=4
Fast readout, Overhead < 0.1s	< 100e RMS, 30e RMS goal	Coadd=1, FR=0.1s, NDR=1

NSFCAM Performance, Readout Speed

Noise statistics from data taken with NSFCAM2,
values calculated by Don Hall's HXRG data pipeline

	NDR=1	NDR=4	NDR=8	NDR=16
100 kpixels/sec	10.2 e-	5.9 e-	4.5 e-	3.4 e-
200 kpixels/sec	12.7 e-	7.1 e-	5.3 e-	4.1 e-
300 kpixels/sec	17.7 e-	9.5 e-	7.1 e-	5.0 e-



Log 10 Plot of read noise at different readout speeds versus NDRs

NSFCAM Performance, Well Depth

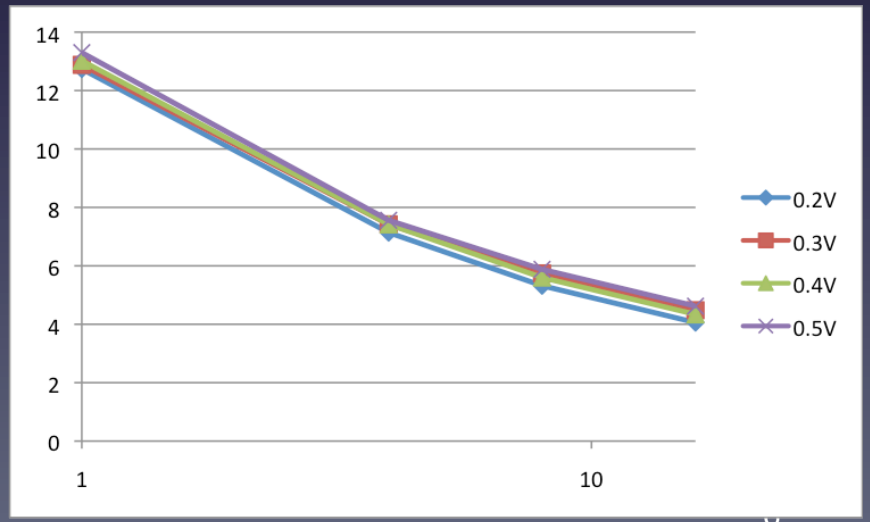
Measured well depth at different bias voltages (|VDSUB – VRESET|)

Bias	Well (ADU)	Conversion	Well (e-)	Notes
0.2 V Bias	~48 K	1.4 e-/ADU	~66 K	High Gain
0.3 V Bias	~16.7 K	5.6 e-/ADU	~93 K	Low Gain
0.4 V Bias	~20.7 K	5.6 e-/ADU	~116 K	Low Gain
0.5 V Bias	~24.2 K	5.6 e-/ADU	~135 K	Low Gain

Noise as a function of NDR for various bias voltages

	NDR=1	NDR=4	NDR=8	NDR=16
0.2V Bias	12.7 e-	7.1 e-	5.3 e-	4.1 e-
0.3V Bias	12.9 e-	7.4 e-	5.7 e-	4.5 e-
0.4 V Bias	13.0 e-	7.4 e-	5.6 e-	4.4 e-
0.5V Bias	13.3 e-	7.5e-	5.9 e-	4.6 e-

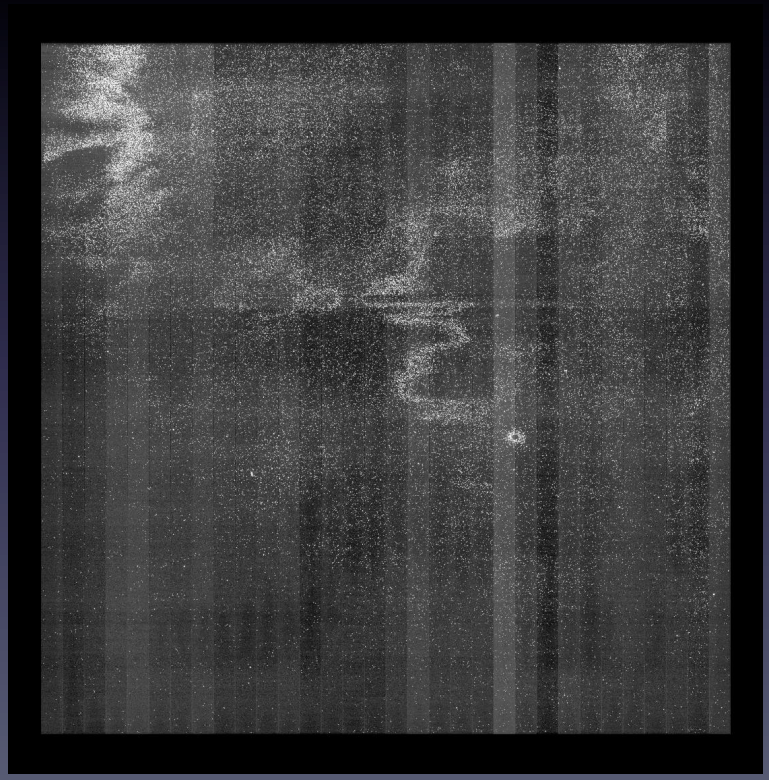
log 10 plot of noise at different bias levels vs. NDRs



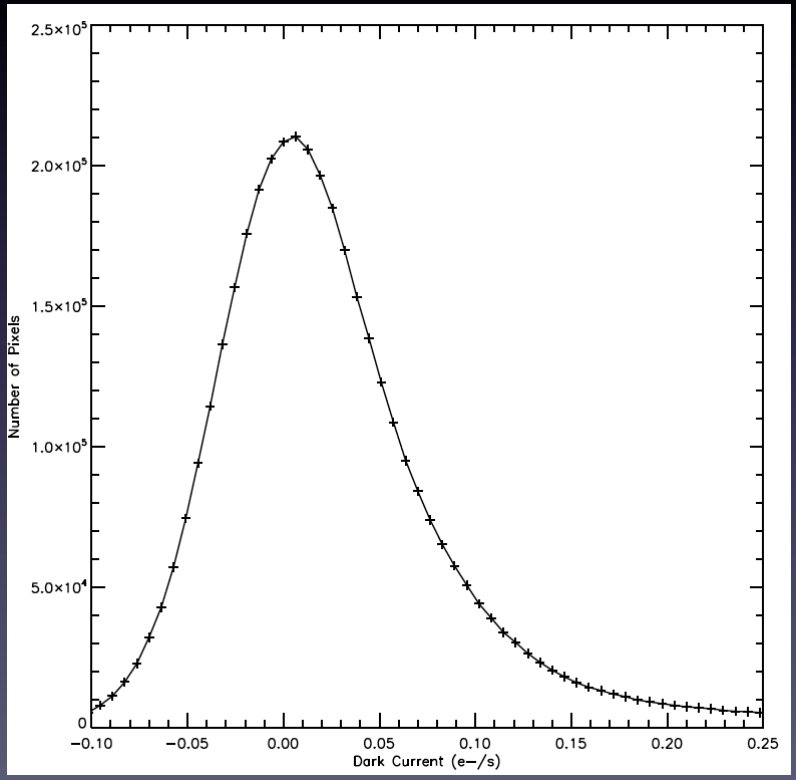
Dark Current

Dark current was measured to be ~0.02 e-/s with the NSFCAM array in the IRTF test dewar.

Dark current image from imaging in test dewar with NSFCAM array



Histogram of dark current pixels



NSFCAM Performance, Sensitivity

Calculated 5 sigma flux limits for 60s of itime

Filter	Magnitude Limit
J	19.5
H	18.1
K	17.6
L′	13.0
M′	10.9

HD129653 taken at M, itime=18s

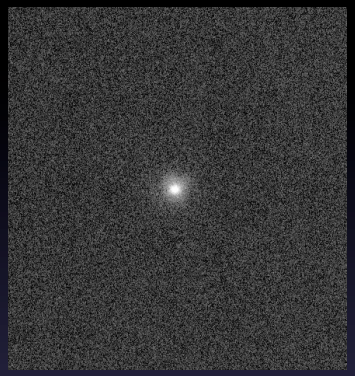
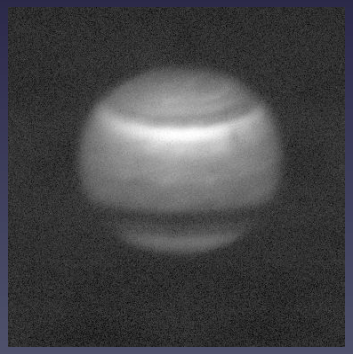


Image of Saturn taken at 5.1μm

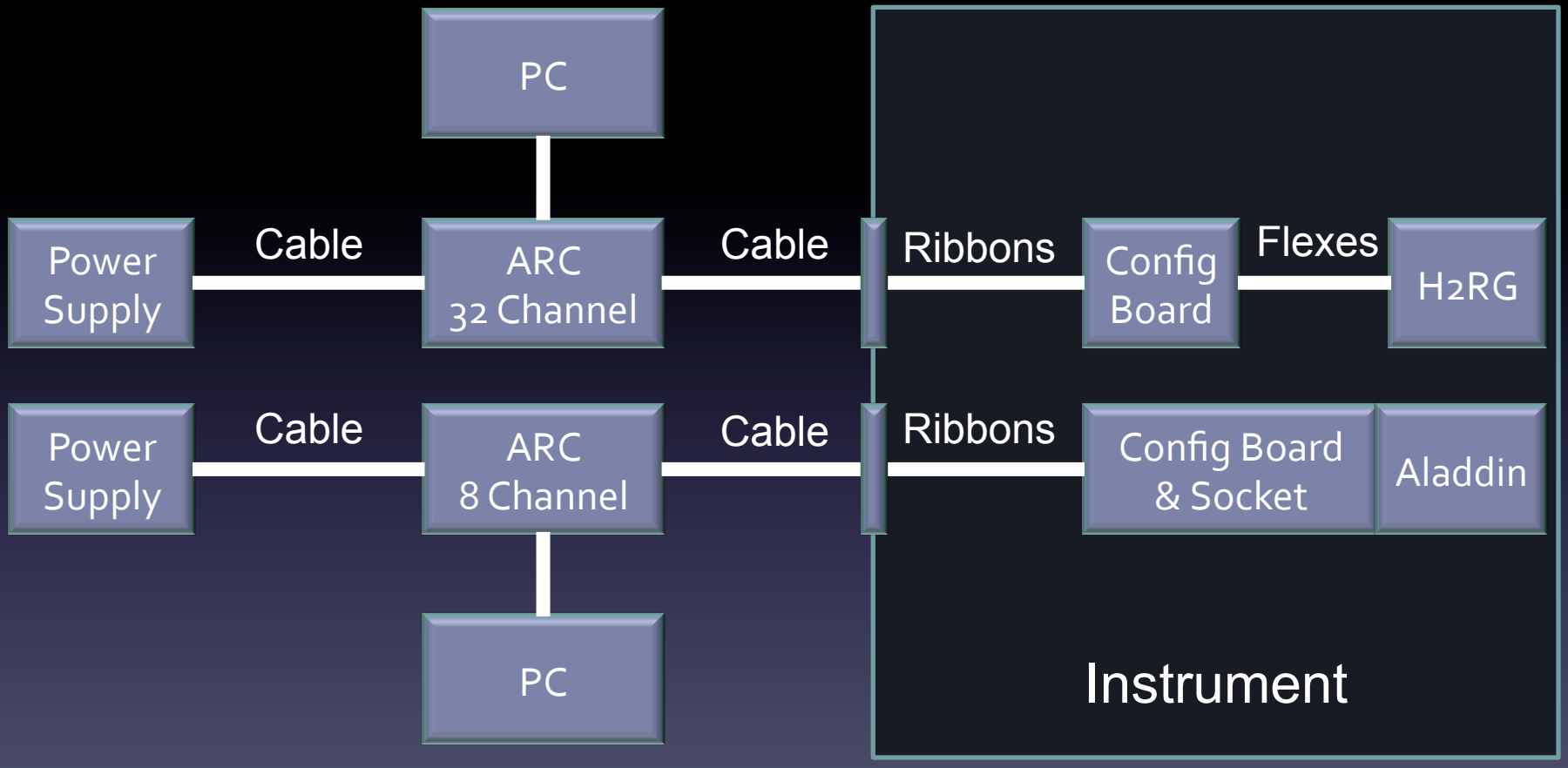


Exposure time necessary to be sky-noise limited

Filter	Itime
J	14s
H	1.5s
K	1.7s
L′	0.05s
M′	0.01s

The 5 sigma flux limit is how bright a star would have to be for its flux to be 5 times the sky noise.

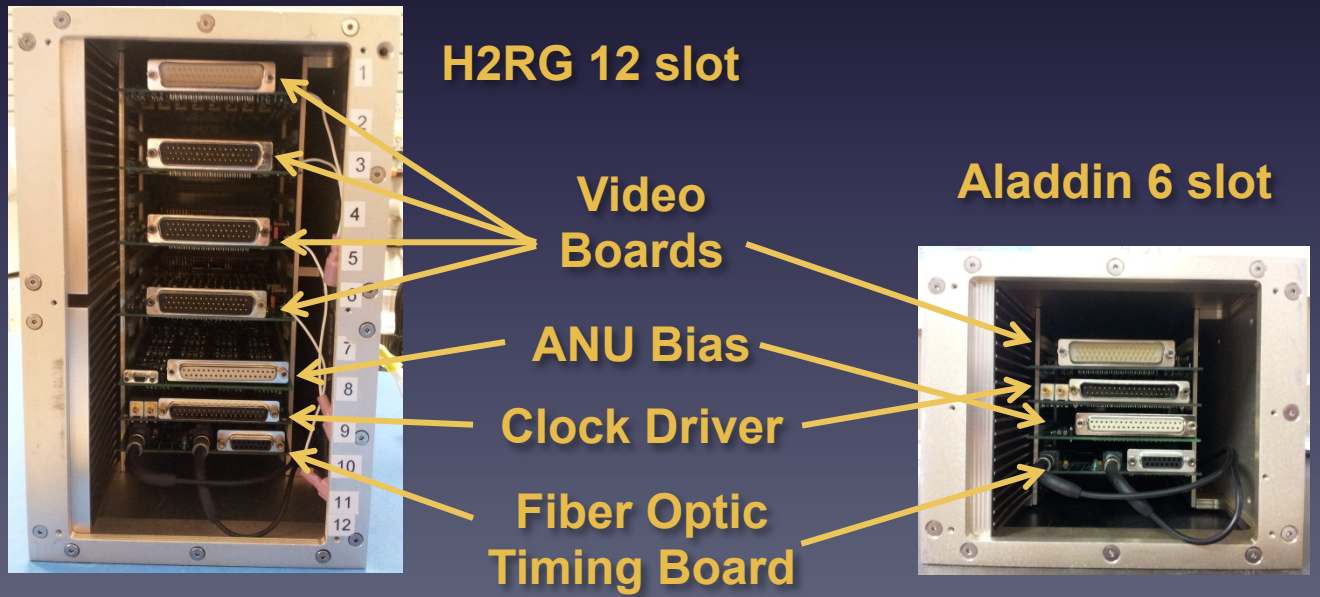
Array Controllers System Diagram



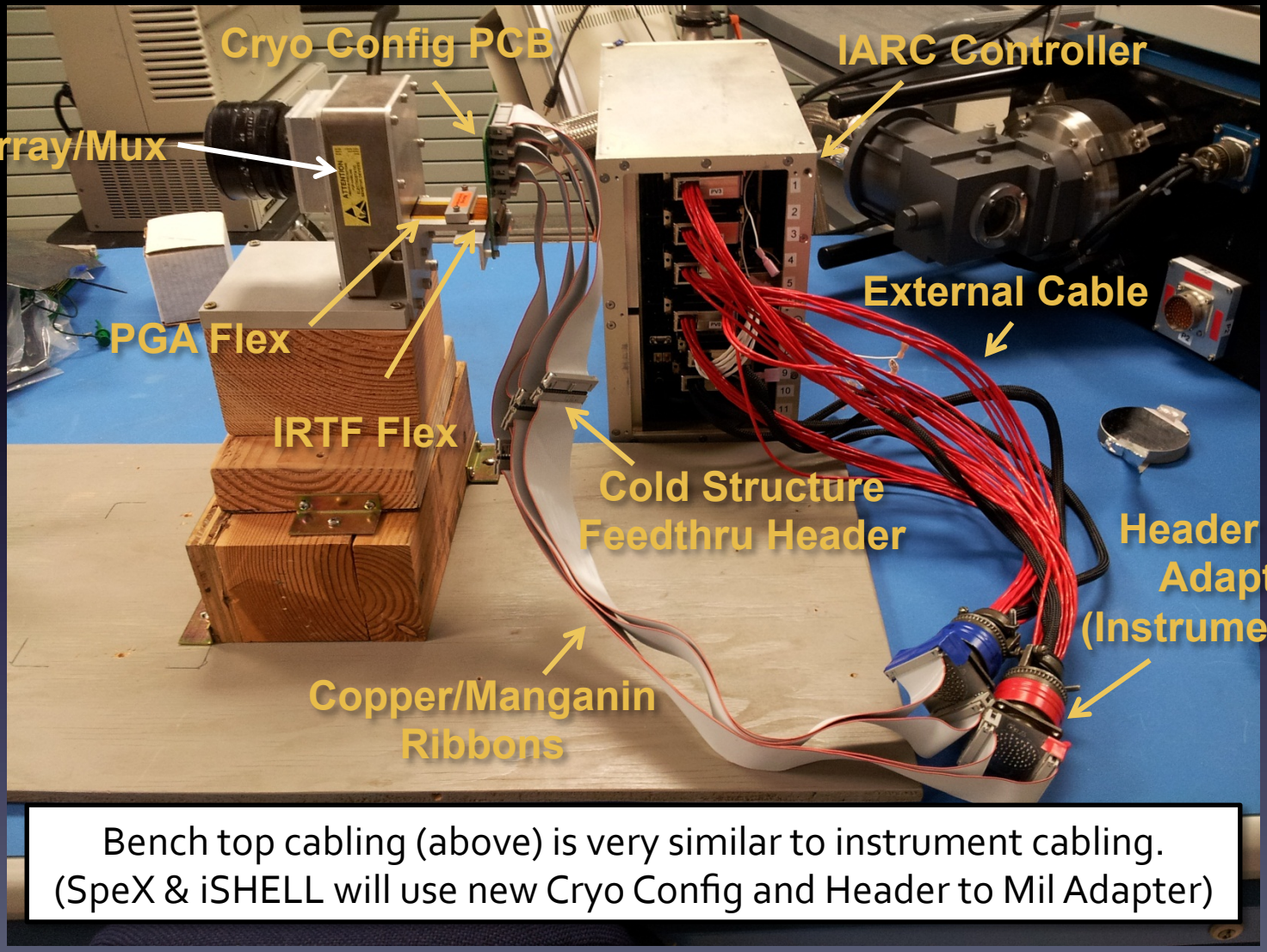
NOTE: No guider (Aladdin array) in NSFCAM

IARC Controller Electronics

- IARC controller electronics consist of:
  - Chassis (6 slot for Aladdin, 12 slot for H2RG)
    - Includes Power Control Board & Backplane
  - Fiber Optic Timing Board (connects to ARC PCI Card in PC)
  - Clock Driver Board
  - 8 Channel Videos Boards (1 for Aladdin, 4-5 for H2RG)
  - ANU Bias Board (modified and built by IRTF)
  - Power Supply (IRTF uses Agilent N6700B family)



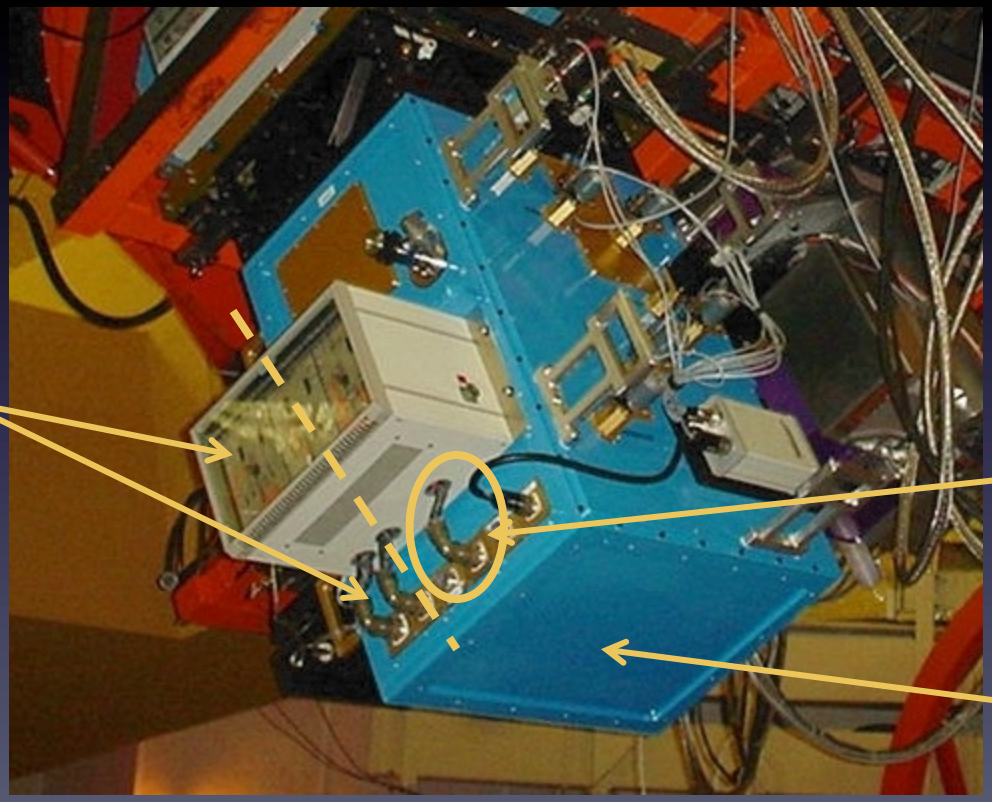
H2RG Cabling



Bench top cabling (above) is very similar to instrument cabling.
(SpeX & iSHELL will use new Cryo Config and Header to Mil Adapter)

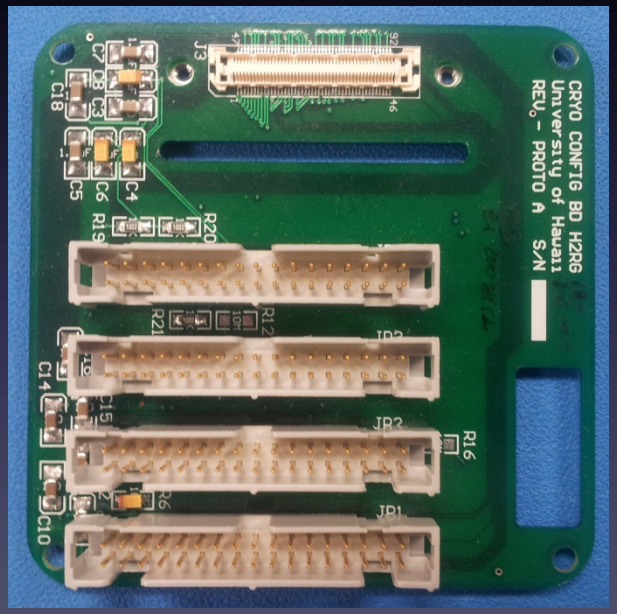
Aladdin Cabling

- SpeX guider Aladdin internal cabling unmodified
  - iSHELL will use SpeX cabling design
- Make external cable to connect ARC to 61 pin Mil Spec



Cryo Config Board

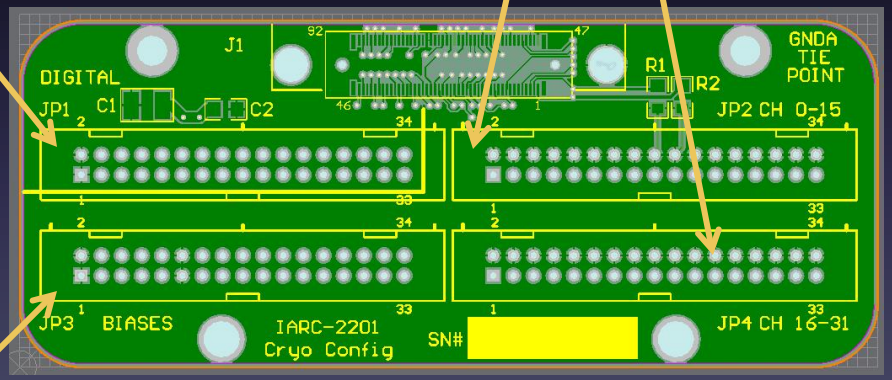
- The Cryo Config interfaces H2RG device to cabling
- Redesigned for SpeX and iSHELL
  - New form factor to support SpeX mount redesign
  - Better separation/grouping of analog and digital signals



Signal Types Mixed

Digital

Channels



Biases

(Designed & Ordered)

ANU Bias Voltage Board

- Peter Onaka found a study that indicated ARC controllers suffer from bias voltage drift
  - Bias drift will greatly reduce the effect of NDRs
- Australian National University (ANU) made a bias board to solve this issue
  - Main feature of this board is a higher performance DAC
  - IRTF built a copy of this board (with permission from ANU)
  - Rev2 will incorporate modifications and clean up layout
- Bias voltages are stable
  - NDRs resulted in lower noise as expected on NSFCAM
  - See results presented in “NSFCAM Performance” slide

Controller Software Design Requirements

- Same array controller software base for all instruments
- Software will interact with the array controller hardware to generate and gather data
- Software will provide user with data by
  - writing to disk as a FITS file
  - sending the data to DV
  - providing the data via shared memory to an external system (e.g. the instrument control software)

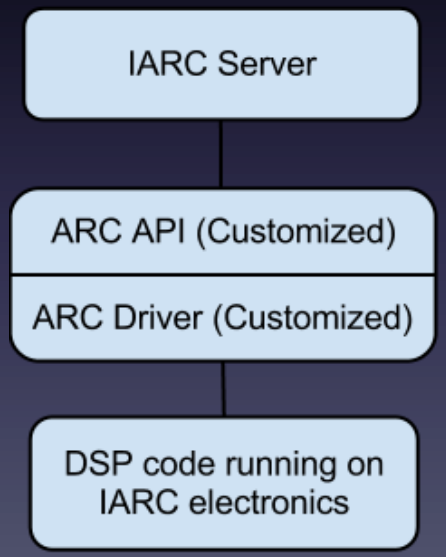
Software Functional Requirements

- Variable integration time, depending on the readout mode
- Coadds of integrations, up to 1,000
- Standard sampling modes: Fowler Single, Fowler Double, Ramp
- Non-destructive Reads, up to 128
- Variable frame rates – 100k, 200k, and 300k pixel/sec
- Background resets, appropriate for the readout speed
- Graceful aborts, allowing users to stop when required
- Image timestamping

Software Design Components

The IARC Software consists of three main components:

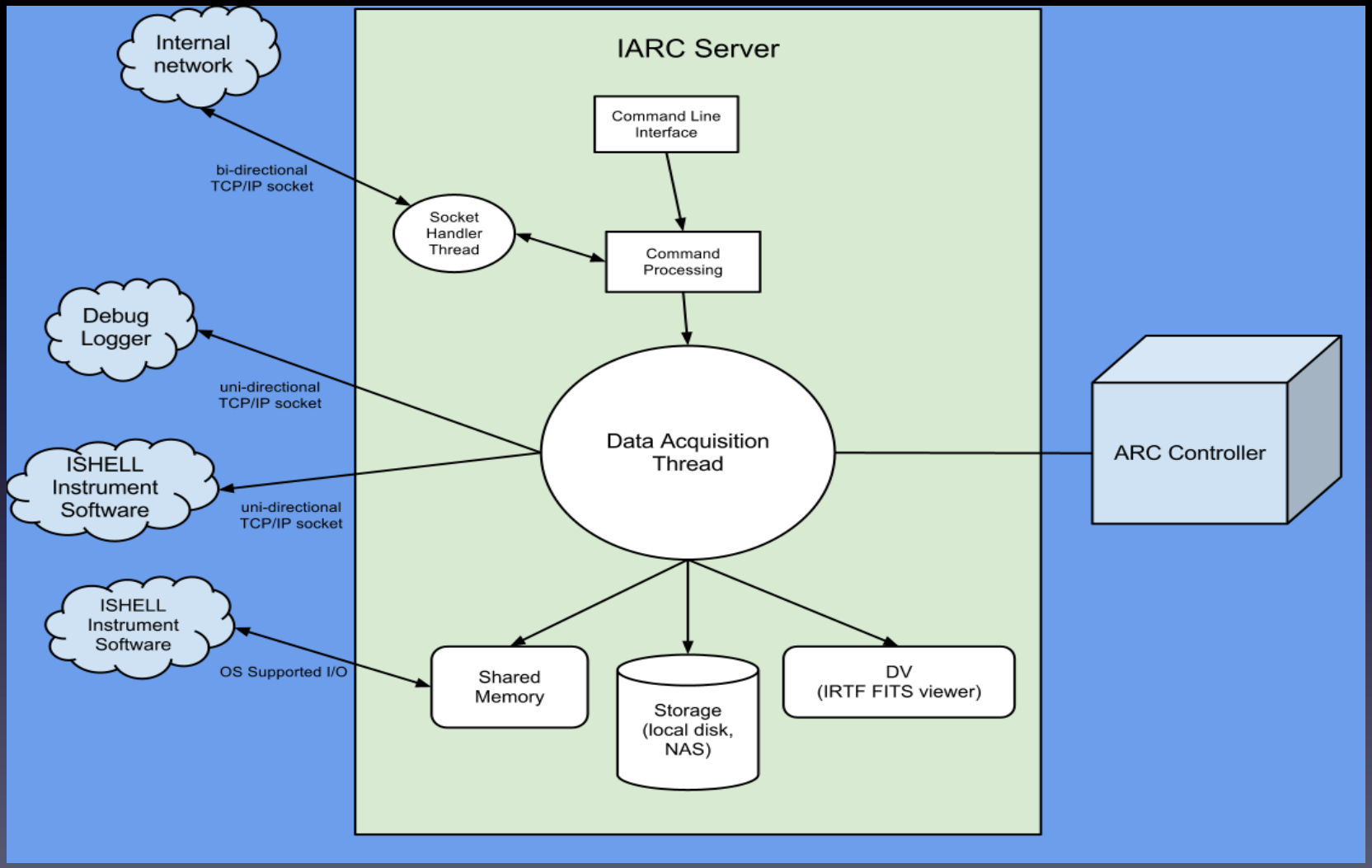
- IARC Server, running on the PC, provides interface to client, directs operations of controller, handles data
- ARC API and ARC Drivers, handle array controller interactions
- DSP Code running on ARC electronics, controls voltages, clocking, data transfer



IARC Server

- Runs on PC
- Provides interface to client, directs operations of controller, handles data
- Provides a TCP/IP socket based interface for client.
- Coordinates operations on the controller
- Processes data, supports basic math functions for Fowler Single, Fowler Double, and Ramp modes
- Handles data product, shares with external processes, writes to disk as a FITS file, sends to DV for viewing

IARC Server Diagram



IARC DSP

- Embedded software component in controller itself
- Different code for Aladdin and H2RG
- Sets bias voltages to array
- Controls clocking of the array
- Operates transmission of data to PC

IARC Component Pricing

Part Number	Type	Price per Unit
ARC-22	Gen 3 Fiber Optic Timing Board	$2,500
ARC-32	IR Clock Driver Board	$2,500
ARC-46	8 Channel IR Video Board	$6,000
ARC-64	Gen 3 PCIe Interface Board	$3,000
IARC-1800	Modified ANU Voltage Board	$1,500
	Agilent Power Supply System	$9,000

IARC System Costs

H2RG Based System, Total Cost: $42,500

Count	Type	Cost
1	Gen 3 Fiber Optic Timing Board	$2,500
1	IR Clock Driver Board	$2,500
4	8 Channel IR Video Board	$24,000
1	Gen 3 PCIe Interface Board	$3,000
1	Modified ANU Voltage Board	$1,500
1	Agilent Power Supply System	$9,000

Aladdin Based System, Total Cost: $24,500

Count	Type	Cost
1	Gen 3 Fiber Optic Timing Board	$2,500
1	IR Clock Driver Board	$2,500
1	8 Channel IR Video Board	$6,000
1	Gen 3 PCIe Interface Board	$3,000
1	Modified ANU Voltage Board	$1,500
1	Agilent Power Supply System	$9,000

Summary

- ARC controller system successfully tested on NSFCAM
  - Noise performance meets iSHELL and SPEX requirements
- Will use ARC controller for all devices
  - Aladdin noise requirements less stringent than H2RG
- Cryo Config, Mil Spec Adapter, and flex ordered
- ANU Bias Board (Rev 2) is all that needs to be designed
  - Incorporates modifications and cleans up layout
- Controller software needs further development for Aladdin device
- Instrument controller software development continuing