ADC8 700-155-01
8 CHANNEL 2 MHz 16bit ANALOG to DIGITAL CONVERTER BOARD

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4.1.1 ADC8 **700-155-01** 8 CHANNEL 2 MHz 16bit ANALOG to DIGITAL CONVERTER BOARD

4.1.1 Overview

The ADC8 is an 8 channel differential input Analog to Digital Converter board. Each channel uses an Analogic 2MHz 16 bit ADC4322. The multilayer printed circuit board construction employs multiple ground/power planes for shielding.

4.1.1.1 Technical Specifications 700-155-01 ADC8

- 8 Independent Channels
- 8 Analogic ADC4322s
- Altera MAX7128 CPLD
- Input range settings (+/-2.5V,+/-5.0V,0-10V)
- 6 layer PCB

Power Requirements
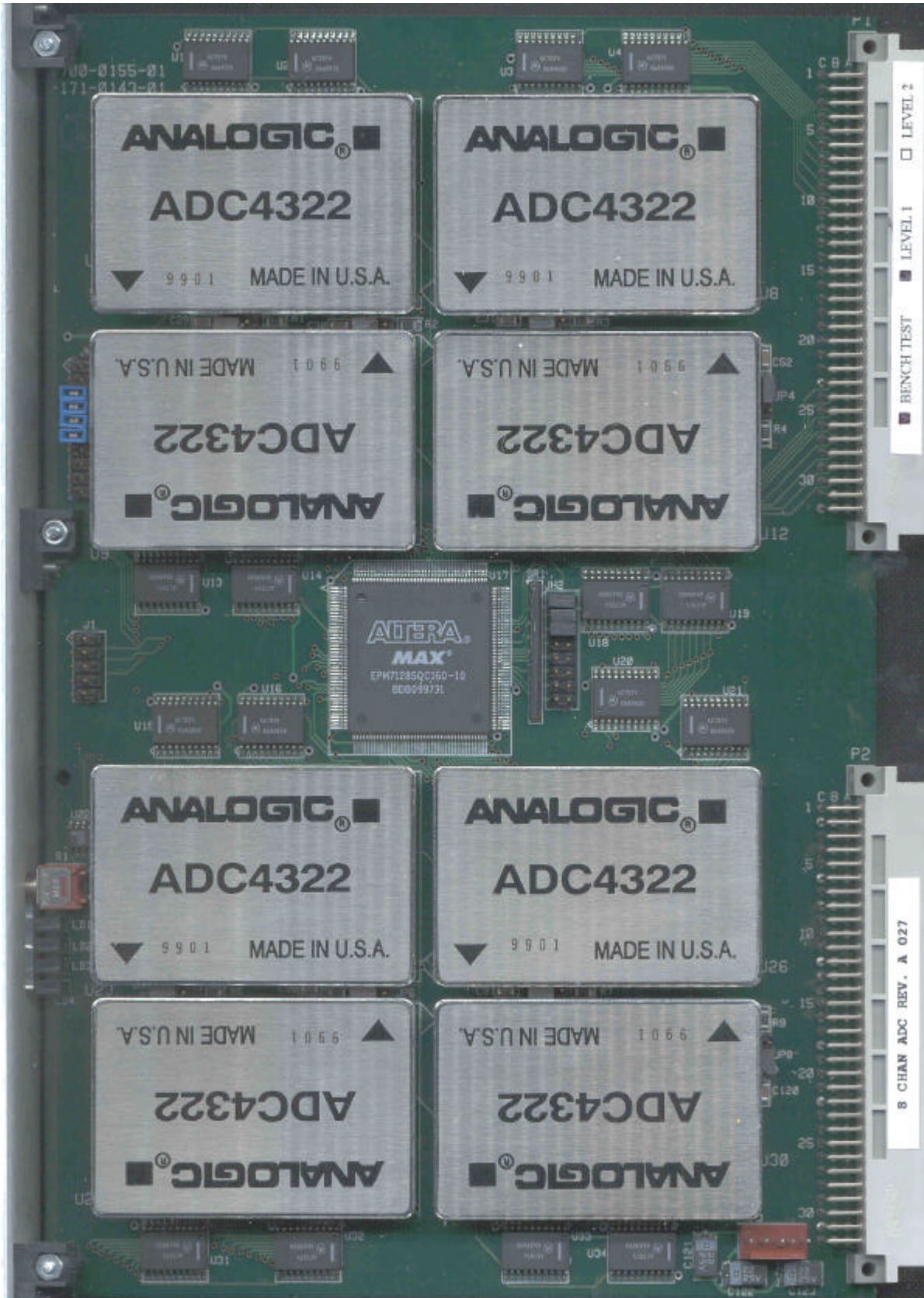
- +5V   696mA Typ.
- +15V   568mA Typ.
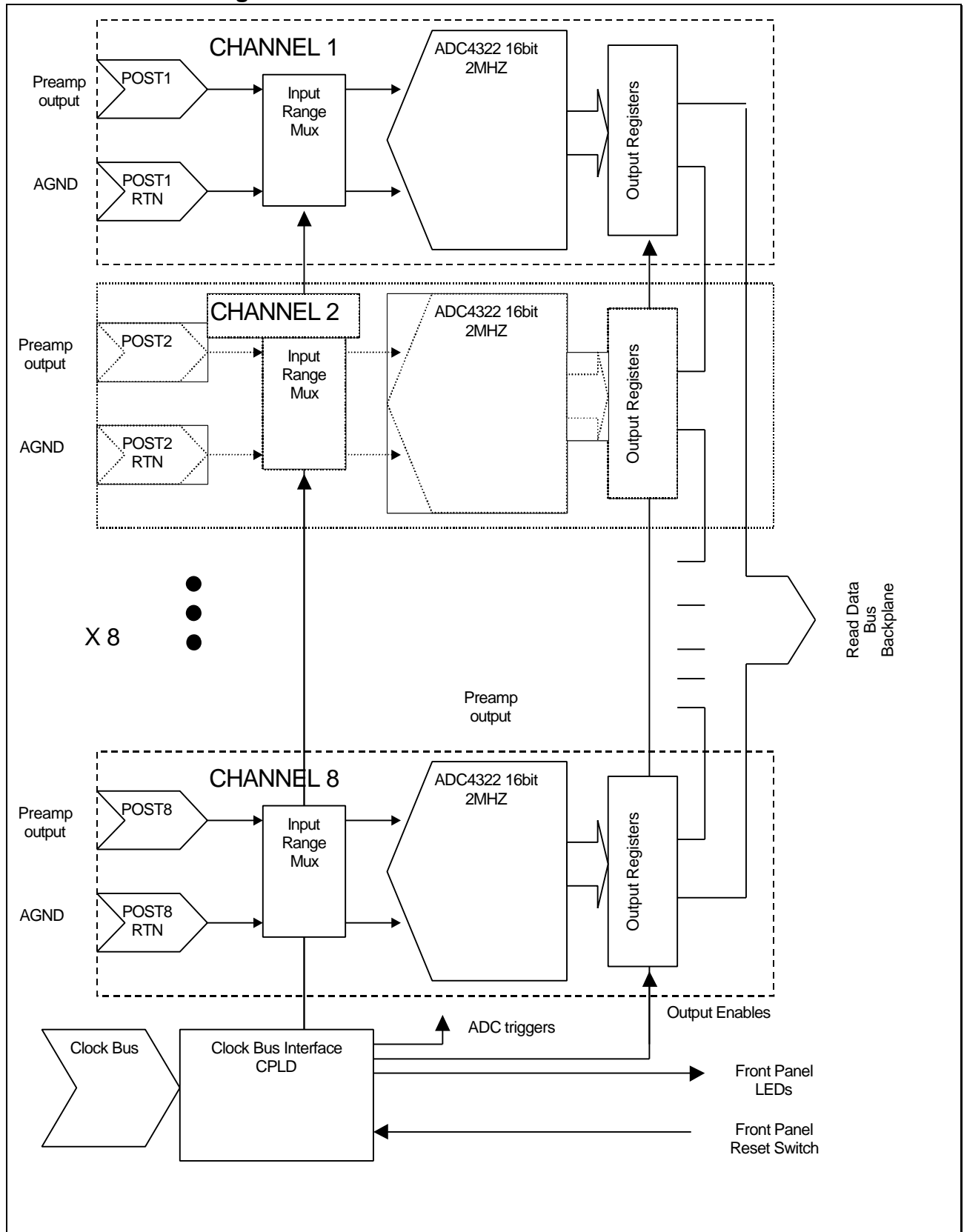- -15V   488mA Typ.

Mechanical Specifications

- Eurocard 6U (160mm x 233.35mm) Form Factor
- P1 96 pin DIN Connector,P2 DIN 41612, 96 Pin Connector
- 6 Layer PCB Construction with Internal Gnd & Power Layers

4.1.1.2 Component side photo

4.1.1.3 Block Diagram

## *4.1.1.4 Functional Description 700-155-01 ADC8*

4.1.1.4.1 Inputs

The outputs of the preamplifier are input (via a backplane ribbon cable) into the PCB via the P2 connector. The schematic signal names are 'POST#' (# =1-8) and the other return or reference signals are 'POST# RTN'. Refer to sheet 1 of the schematic for the pin assignments on P2.

4.1.1.4.2 Input Range Setting

An input range select analog multiplexer is configured by U17 an Altera MAX7128 CPLD for a +/- 2.5V range. Alternate settings on the Configuration Header can set the input range for +/-5V or 0-10V range.

4.1.1.4.3 Input Header

An Input Header either selects the normal signal path or analog ground AGND. The normal signal input configuration is pins 1 and 2 shunted.
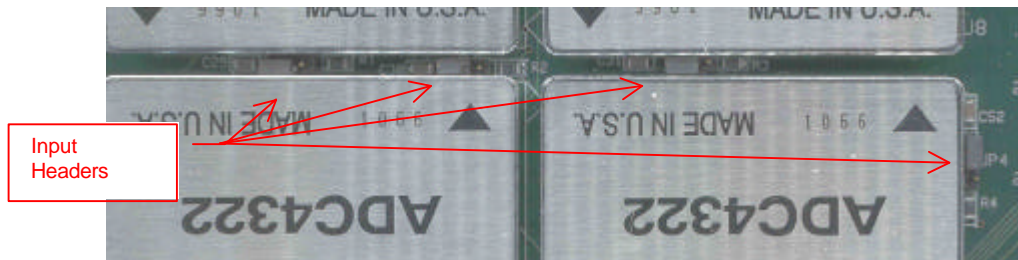
4.1.1.4.4 Analog to Digital Converter

Each of the ADC4322 analog to digital converters is triggered to convert with TRIG# (#=1-8) signals from U17 MAX7128. The TRIG# signals are derived from the Clock Bus signal CB_D5 (CONVERT). 500nsec after the rising edge of the TRIG# signal the ADC will complete its conversion and generate a pulse on its TRANSFER output. The rising edge of TRANSFER=XFER# (#=1-8) clocks the 16 bits of digital data present at the ADC outputs into the output registers (74ACT574s).

4.1.1.4.5 Output Sequencing

Each bank of output registers is sequentially enabled (OE#, #=1-8) out to the Read Data Bus based on a state machine design in U17. The Clock Bus signals, CONVERT (CB_D5) initializes the state machine and READ_DATA (CB_D4) enables a counter that sequentially generates the OE# signals on CB_WR! clock signal rising edges.

4.1.1.5 Configuration and Test Connectors

JH1 LED shunt/test point header

JH2 CPLD configuration header

JTAG header
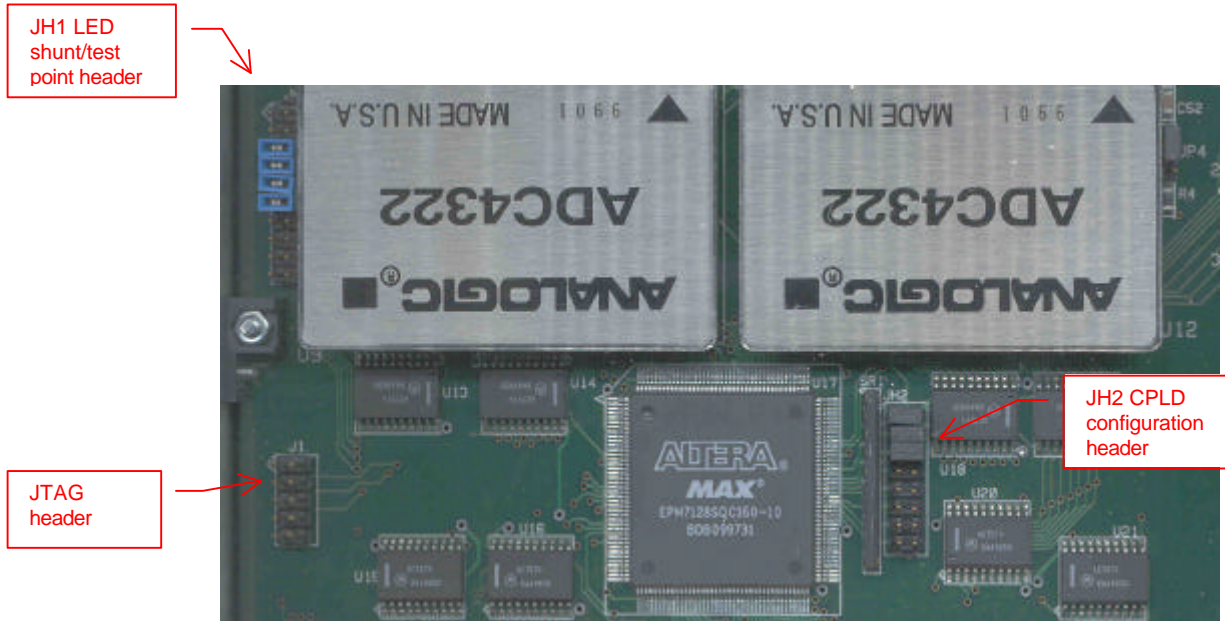
JH1 LED/Test Header
JH1 is a 20 pin header that serves the dual purpose of connecting the test signals to the front panel LEDS.
The four shunts connect the following signals from the CPLD U17 (Altera MAX7128) to the front panel LEDS:
Signal = front panel label
DIAG0 = ADDR0
DIAG1 = ADDR1
DIAG2 = OE
DIAG3 = CONVERT

JH2 CPLD Configuration Header
JH2 provides input configuration control for the CPLD U5. The default configuration is the only implemented mode.

JTAG Header
The JTAG header is used to program the MAX7128 CPLD.

ADC8_2
ADC8_2.SCH
POST1RTN
POST1
TRIG1
RB_D[0..15]
RNG_CTL
POST2RTN
POST2
TRIG2
OUFLOW[1..8]
OE[1..8]

ADC8_1
ADC8_1.SCH
CB_CW[O..7]
CB_D[0..15]
RB_SD[0..7]
CB_WR!

RB_RD!
RB_D[0..15]
POST1
POST1RTN
POST2
POST2RTN
POST3
POST3RTN
POST4
POST4RTN
POST5
POST5RTN
POST6
POST6RTN
POST7
POST7RTN
POST8
POST8RTN

ADC8_6
ADC8_6.SCH
CB_CW[0..7] OUFLOW[1..8]
CB_D[0..15]   OE[1..8]
RB_SD[0..7]   TRIG1
CB_WR!   TRIG2
                 TRIG3
RB_RD!   TRIG4
RB_D[0..15]   TRIG5
                 TRIG6
                 TRIG7
                 TRIG8

RNG_CTL

OUFLOW[1..8]

ADC8_3
ADC8_3.SCH
POST3RTN
POST3
TRIG3
RB_D[0..15]
RNG_CTL
POST4RTN
POST4
TRIG4
OUFLOW[1..8]
OE[1..8]

ADC8_4
ADC8_4.SCH
POST5RTN
POST5
TRIG5
RB_D[0..15]
RNG_CTL
POST6RTN
POST6
TRIG6
OUFLOW[1..8]
OE[5..8]

ADC8_5
ADC8_5.SCH
POST7RTN
POST7
TRIG7
RB_D[0..15]
RNG_CTL
POST8RTN
POST8
TRIG8
OUFLOW[1..8]
OE[5..8]

P1
C

READ DATA BUS

B

A

ECO MOVE
AGNDS/+15V
TO COL A

RB_D16
RB_D17
RB_D18
RB_D19
RB_D20
RB_D21
RB_D22

AGND

RB_D23
RB_D24
RB_D25
RB_D26
RB_D27
RB_D28
RB_D29
RB_D30
RB_D31

AGND

C1	C1
C2	C2
C3	C3
C4	C4
C5	C5
C6	C6
C7	C7
C8	C8
C9	C9
C10	C10
C11	C11
C12	C12
C13	C13
C14	C14
C15	C15
C16	C16
C17	C17
C18	C18
C19	C19
C20	C20
C21	C21
C22	C22
C23	C23
C24	C24
C25	C25
C26	C26
C27	C27
C28	C28
C29	C29
C30	C30
C31	C31
C32	C32

DIN96

+5V B1
DGND B2
RB_RD! B3
RB_D0 B4
RB_D1 B5
RB_D2 B6
RB_D3 B7
RB_D4 B8
RB_D5 B9
RB_D6 B10
RB_D7 B11
DGND B12
+5V B13
RB_D8 B14
RB_D9 B15
RB_D10 B16
RB_D11 B17
RB_D12 B18
RB_D13 B19
RB_D14 B20
RB_D15 B21
DGND B22
RB_SD0 B23
RB_SD1 B24
RB_SD2 B25
RB_SD3 B26
RB_SD4 B27
RB_SD5 B28
RB_SD6 B29
RB_SD7 B30
DGND B31
+5V B32

RB_RD!

RB_SD[0..7]
RB_D[0..15]

+15V A1
AGND A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
AGND A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
AGND A22
A23
A24
A25
A26
A27
A28
A29
A30
AGND A31
-15V A32

P3
+5V +5V 1
DGND DGND 2
+15V +15V 3
AGND AGND 4
-15V -15V 5
CON5

+5V +15V
+ C122 + C121
22uF 25V Ta 22uF 25V Ta
DGND AGND

+ C123
22uF 25V Ta
-15V

P2
C

CLOCK BUS

B

A

AGND C2
POST1 POST1 C3
AGND C4
POST2 POST2 C5
AGND C6
POST3 POST3 C7
AGND C8
POST4 POST4 C9
AGND C10
POST5 POST5 C11
AGND C12
POST6 POST6 C13
AGND C14
POST7 POST7 C15
AGND C16
POST8 POST8 C17
AGND C18

C1	C1
	C2
	C3
	C4
	C5
	C6
	C7
	C8
	C9
	C10
	C11
	C12
	C13
	C14
	C15
	C16
	C17
	C18
C19	C19
C20	C20
C21	C21
C22	C22
C23	C23
C24	C24
C25	C25
C26	C26
C27	C27
C28	C28
C29	C29
C30	C30
C31	C31
C32	C32

DIN96

+5V B1
DGND B2
CB_WR! B3
CB_D0 B4
CB_D1 B5
CB_D2 B6
CB_D3 B7
CB_D4 B8
CB_D5 B9
CB_D6 B10
CB_D7 B11
DGND B12
+5V B13
CB_D8 B14
CB_D9 B15
CB_D10 B16
CB_D11 B17
CB_D12 B18
CB_D13 B19
CB_D14 B20
CB_D15 B21
DGND B22
CB_CW0 B23
CB_CW1 B24
CB_CW2 B25
CB_CW3 B26
CB_CW4 B27
CB_CW5 B28
CB_CW6 B29
CB_CW7 B30
DGND B31
+5V B32

CB_WR!

CB_CW[0..7]
CB_D[0..15]

+15V A1
AGND A2
POST1RTN A3
AGND A4
POST2RTN A5
AGND A6
POST3RTN A7
AGND A8
POST4RTN A9
AGND A10
POST5RTN A11
AGND A12
POST6RTN A13
AGND A14
POST7RTN A15
AGND A16
POST8RTN A17
AGND A18
A19
A20
A21
AGND A22
A23
A24
A25
A26
A27
A28
A29
A30
AGND A31
-15V A32

POST1RTN
POST2RTN
POST3RTN
POST4RTN
POST5RTN
POST6RTN
POST7RTN
POST8RTN

BACK ANNOTATED

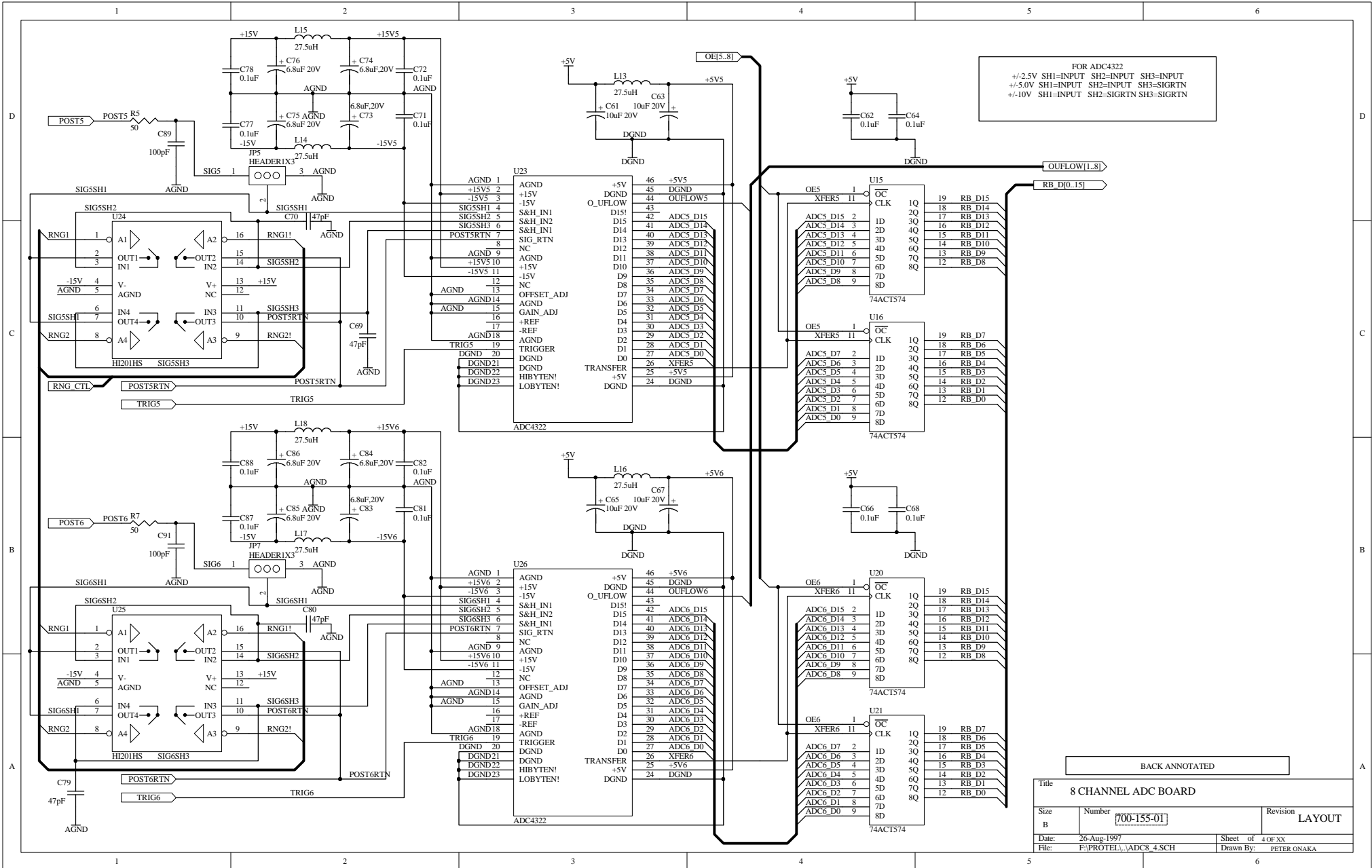| Title | | | |
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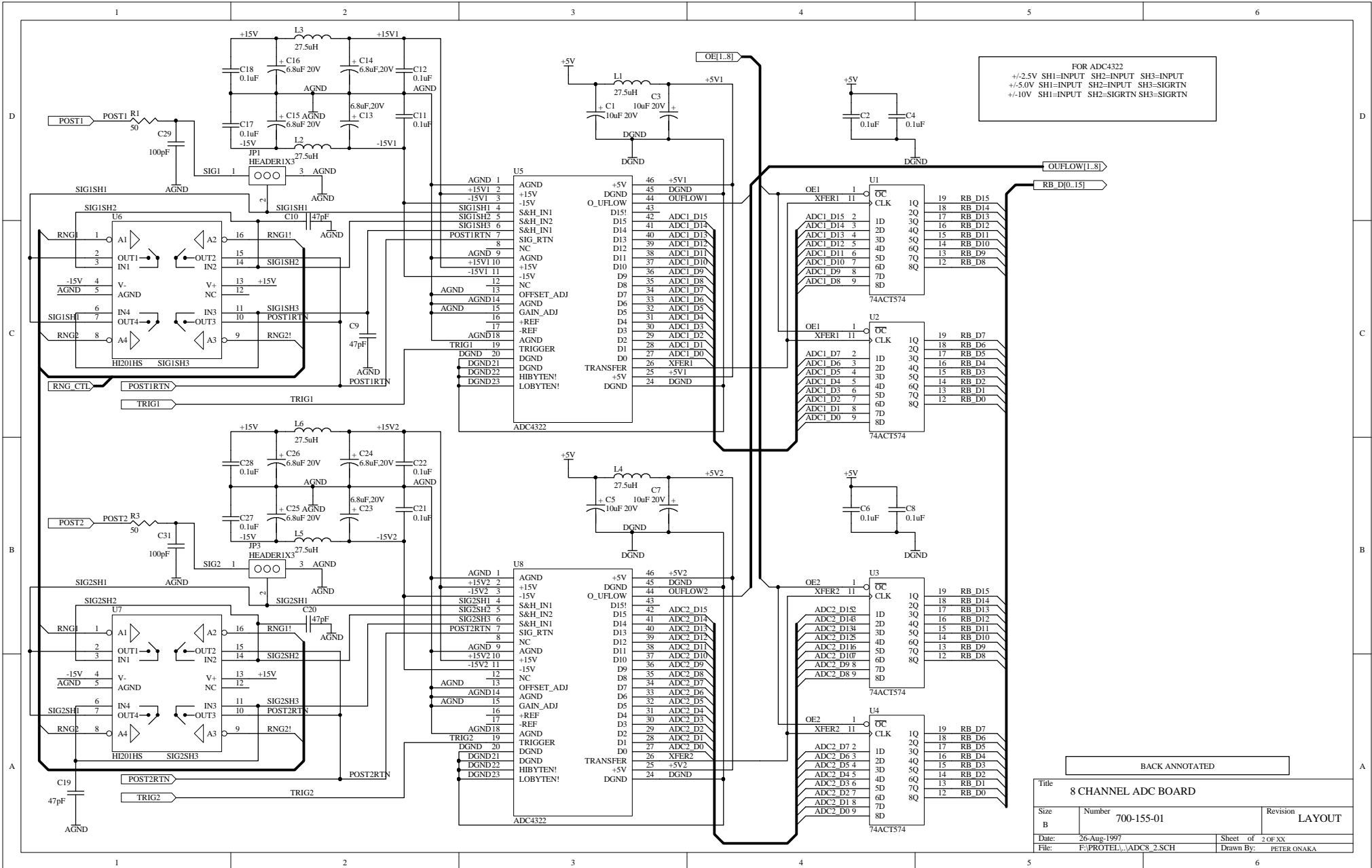
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+/-2.5V SH1=INPUT SH2=INPUT SH3=INPUT
+/-5.0V SH1=INPUT SH2=INPUT SH3=SIGRTN
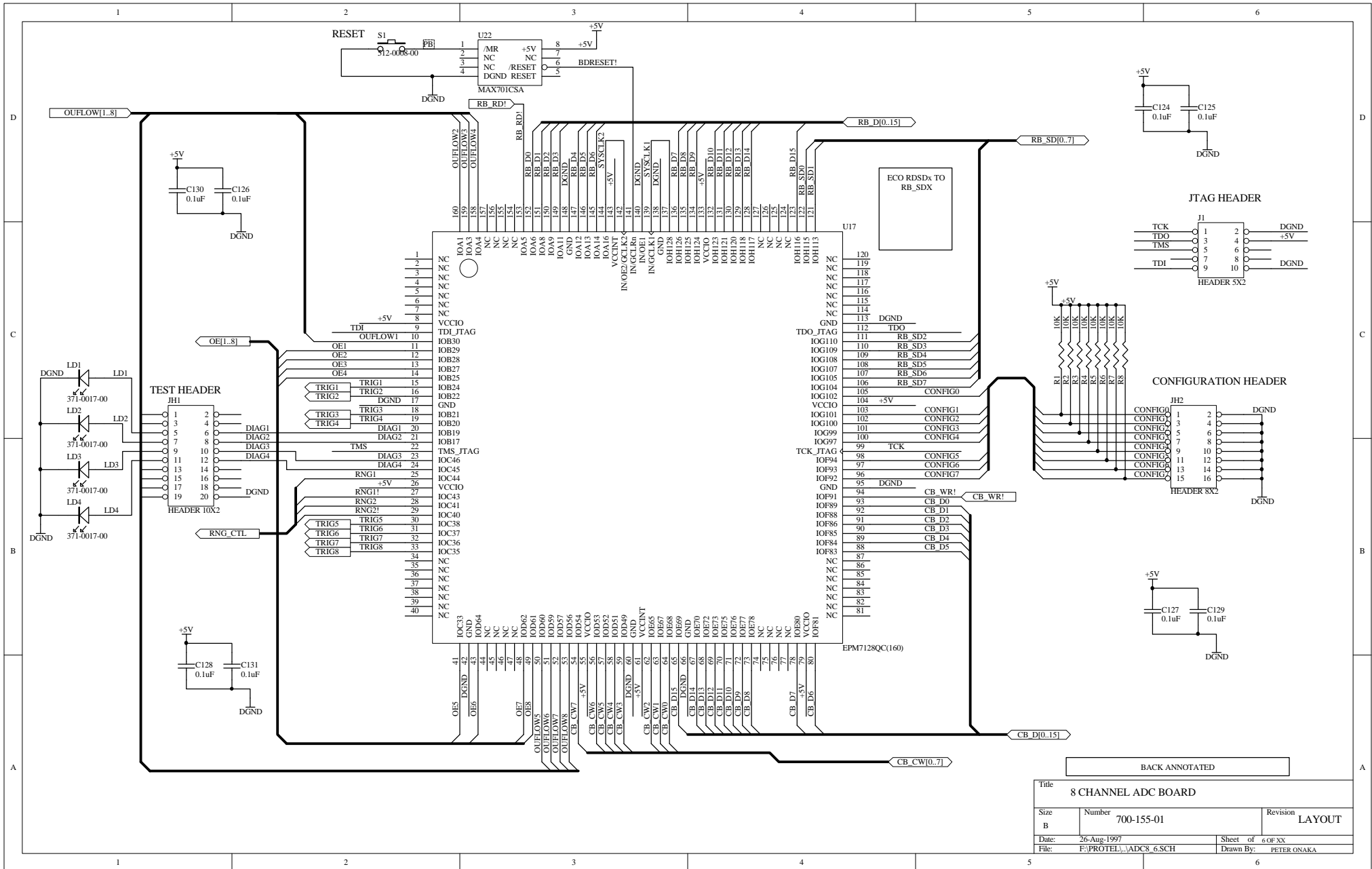+/-10V   SH1=INPUT SH2=SIGRTN SH3=SIGRTN

OE[1..8]
OUFLOW[1..8]
RB_D[0..15]

BACK ANNOTATED

Title			
8 CHANNEL ADC BOARD			
Size	Number		Revision
B	700-155-01		LAYOUT
Date:	26-Aug-1997	Sheet	of 2 OF XX
File:	F:\PROTEL\..\ADC8_2.SCH	Drawn By:	PETER ONAKA

FOR ADC4322
+/-2.5V SH1=INPUT SH2=INPUT SH3=INPUT
+/-5.0V SH1=INPUT SH2=INPUT SH3=SIGRTN
+/-10V   SH1=INPUT SH2=SIGRTN SH3=SIGRTN

OE[1..8]

OUFLOW[1..8]

RB_D[0..15]

POST3   R2 50   C30 100pF

+15V   L7 27.5uH   +15V3
C32 0.1uF   + C34 6.8uF 20V   + C36 6.8uF,20V   C38 0.1uF
AGND   AGND
C33 0.1uF   + C35 6.8uF 20V   AGND   6.8uF,20V + C37   C39 0.1uF
-15V   L8 27.5uH   -15V3
JP2 HEADER1X3
SIG3   1   3 AGND
AGND   AGND
SIG3SH1   2

+5V   L9 27.5uH   +5V3
C56 10uF 20V   C54 10uF 20V
DGND
DGND

+5V
C53 0.1uF   C55 0.1uF
DGND

SIG3SH1
SIG3SH2
U10 HI201HS
RNG1   1 A1   A2 16 RNG1!
2   OUT1   OUT2 15
3   IN1   IN2 14 SIG3SH2
-15V 4 V-   V+ 13 +15V
AGND 5   NC 12
6 IN4   IN3 11 SIG3SH3
SIG3SH1 7 OUT4   OUT3 10 POST3RTN
RNG2   8 A4   A3 9 RNG2!
SIG3SH3
C40 47pF   AGND
C41 47pF   AGND

U9 ADC4322
AGND 1   AGND   +5V 46 +5V3
+15V3 2 +15V   DGND 45 DGND
-15V3 3 -15V   O_UFLOW 44 OUFLOW3
SIG3SH1 4 S&H_IN1   D15! 43
SIG3SH2 5 S&H_IN2   D15 42 ADC3_D15
SIG3SH3 6 S&H_IN1   D14 41 ADC3_D14
POST3RTN 7 SIG_RTN   D13 40 ADC3_D13
8 NC   D12 39 ADC3_D12
AGND 9 AGND   D11 38 ADC3_D11
+15V3 10 +15V   D10 37 ADC3_D10
-15V3 11 -15V   D9 36 ADC3_D9
12 NC   D8 35 ADC3_D8
AGND 13 OFFSET_ADJ   D7 34 ADC3_D7
AGND 14 AGND   D6 33 ADC3_D6
15 GAIN_ADJ   D5 32 ADC3_D5
16 +REF   D4 31 ADC3_D4
17 -REF   D3 30 ADC3_D3
AGND 18 AGND   D2 29 ADC3_D2
TRIG3 19 TRIGGER   D1 28 ADC3_D1
DGND 20 DGND   D0 27 ADC3_D0
DGND 21 DGND   XFER3 26 XFER3
DGND 22 DGND   +5V 25 +5V3
DGND 23 HIBYTEN!   DGND 24 DGND
LOBYTEN!

U14 74ACT574
OE3   1 OC
XFER3 11 CLK
1Q 19 RB_D15
2Q 18 RB_D14
ADC3_D15 2 1D   3Q 17 RB_D13
ADC3_D14 3 2D   4Q 16 RB_D12
ADC3_D13 4 3D   5Q 15 RB_D11
ADC3_D12 5 4D   6Q 14 RB_D10
ADC3_D11 6 5D   7Q 13 RB_D9
ADC3_D10 7 6D   8Q 12 RB_D8
ADC3_D9 8 7D
ADC3_D8 9 8D

U13 74ACT574
OE3   1 OC
XFER3 11 CLK
1Q 19 RB_D7
2Q 18 RB_D6
ADC3_D7 2 1D   3Q 17 RB_D5
ADC3_D6 3 2D   4Q 16 RB_D4
ADC3_D5 4 3D   5Q 15 RB_D3
ADC3_D4 5 4D   6Q 14 RB_D2
ADC3_D3 6 5D   7Q 13 RB_D1
ADC3_D2 7 6D   8Q 12 RB_D0
ADC3_D1 8 7D
ADC3_D0 9 8D

POST3RTN
RNG_CTL
POST3RTN
TRIG3   TRIG3

POST4   R4 50   C52 100pF

+15V   L10 27.5uH   +15V4
C42 0.1uF   + C44 6.8uF 20V   + C46 6.8uF,20V   C48 0.1uF
AGND   AGND
C43 0.1uF   + C45 6.8uF 20V   AGND   6.8uF,20V + C47   C49 0.1uF
-15V   L11 27.5uH   -15V4
JP4 HEADER1X3
SIG4   1   3 AGND
AGND   AGND
SIG4SH1   2

+5V   L12 27.5uH   +5V4
C60 10uF 20V   C58 10uF 20V
DGND
DGND

+5V
C57 0.1uF   C59 0.1uF
DGND

SIG4SH1
SIG4SH2
U11 HI201HS
RNG1   1 A1   A2 16 RNG1!
2   OUT1   OUT2 15
3   IN1   IN2 14 SIG4SH2
-15V 4 V-   V+ 13 +15V
AGND 5   NC 12
6 IN4   IN3 11 SIG4SH3
SIG4SH1 7 OUT4   OUT3 10 POST4RTN
RNG2   8 A4   A3 9 RNG2!
SIG4SH3
C50 47pF   AGND

U12 ADC4322
AGND 1   AGND   +5V 46 +5V4
+15V4 2 +15V   DGND 45 DGND
-15V4 3 -15V   O_UFLOW 44 OUFLOW4
SIG4SH1 4 S&H_IN1   D15! 43
SIG4SH2 5 S&H_IN2   D15 42 ADC4_D15
SIG4SH3 6 S&H_IN1   D14 41 ADC4_D14
POST4RTN 7 SIG_RTN   D13 40 ADC4_D13
8 NC   D12 39 ADC4_D12
AGND 9 AGND   D11 38 ADC4_D11
+15V4 10 +15V   D10 37 ADC4_D10
-15V4 11 -15V   D9 36 ADC4_D9
12 NC   D8 35 ADC4_D8
AGND 13 OFFSET_ADJ   D7 34 ADC4_D7
AGND 14 AGND   D6 33 ADC4_D6
15 GAIN_ADJ   D5 32 ADC4_D5
16 +REF   D4 31 ADC4_D4
17 -REF   D3 30 ADC4_D3
AGND 18 AGND   D2 29 ADC4_D2
TRIG4 19 TRIGGER   D1 28 ADC4_D1
DGND 20 DGND   D0 27 ADC4_D0
DGND 21 DGND   XFER4 26 XFER4
DGND 22 DGND   +5V 25 +5V4
DGND 23 HIBYTEN!   DGND 24 DGND
LOBYTEN!

U19 74ACT574
OE4   1 OC
XFER4 11 CLK
1Q 19 RB_D15
2Q 18 RB_D14
ADC4_D15 2 1D   3Q 17 RB_D13
ADC4_D14 3 2D   4Q 16 RB_D12
ADC4_D13 4 3D   5Q 15 RB_D11
ADC4_D12 5 4D   6Q 14 RB_D10
ADC4_D11 6 5D   7Q 13 RB_D9
ADC4_D10 7 6D   8Q 12 RB_D8
ADC4_D9 8 7D
ADC4_D8 9 8D

U18 74ACT574
OE4   1 OC
XFER4 11 CLK
1Q 19 RB_D7
2Q 18 RB_D6
ADC4_D7 2 1D   3Q 17 RB_D5
ADC4_D6 3 2D   4Q 16 RB_D4
ADC4_D5 4 3D   5Q 15 RB_D3
ADC4_D4 5 4D   6Q 14 RB_D2
ADC4_D3 6 5D   7Q 13 RB_D1
ADC4_D2 7 6D   8Q 12 RB_D0
ADC4_D1 8 7D
ADC4_D0 9 8D

C51 47pF   AGND
POST4RTN
TRIG4   TRIG4

BACK ANNOTATED

Title: 8 CHANNEL ADC BOARD
Size B   Number 700-155-01   Revision LAYOUT
Date: 26-Aug-1997   Sheet of 3 OF XX
File: F:\PROTEL\..\ADC8_3.SCH   Drawn By: PETER ONAKA

FOR ADC4322
+/-2.5V SH1=INPUT SH2=INPUT SH3=INPUT
+/-5.0V SH1=INPUT SH2=INPUT SH3=SIGRTN
+/-10V   SH1=INPUT SH2=SIGRTN SH3=SIGRTN

OE[5..8]

OUFLOW[1..8]
RB_D[0..15]

U23 ADC4322
U26 ADC4322

U24 HI201HS
U25 HI201HS

U15 74ACT574
U16 74ACT574
U20 74ACT574
U21 74ACT574

BACK ANNOTATED

Title
8 CHANNEL ADC BOARD

Size	Number	Revision
B	700-155-01	LAYOUT

| Date: | 26-Aug-1997 | Sheet of | 4 OF XX |
| File: | F:\PROTEL\..\ADC8_4.SCH | Drawn By: | PETER ONAKA |

FOR ADC4322
+/-2.5V SH1=INPUT SH2=INPUT SH3=INPUT
+/-5.0V SH1=INPUT SH2=INPUT SH3=SIGRTN
+/-10V   SH1=INPUT SH2=SIGRTN SH3=SIGRTN

OE[5..8]

OUFLOW[1..8]
RB_D[0..15]

POST7 R6 50
C90 100pF

+15V L19 27.5uH +15V7
C92 0.1uF + C94 6.8uF 20V + C96 6.8uF,20V C98 0.1uF
AGND AGND
C93 0.1uF + C95 AGND 6.8uF 20V 6.8uF,20V + C97 C99 0.1uF
-15V L20 27.5uH -15V7
JP6 HEADER1X3

+5V L21 27.5uH +5V7
+ C115 10uF 20V C113 10uF 20V +
DGND DGND

+5V
C112 0.1uF C114 0.1uF
DGND

SIG7SH1
SIG7SH2
SIG7SH1
C100 47pF

U28 HI201HS
RNG1 1 A1
2 OUT1 A2 16 RNG1!
3 IN1 OUT2 15
14 IN2 SIG7SH2
-15V 4 V- V+ 13 +15V
AGND 5 AGND NC 12
SIG7SH1 6 IN4 IN3 11 SIG7SH3
7 OUT4 OUT3 10 POST7RTN
RNG2 8 A4 A3 9 RNG2!
SIG7SH3
C101 47pF
AGND

RNG_CTL
POST7RTN
TRIG7 TRIG7

U27 ADC4322
AGND 1 AGND +5V 46 +5V7
+15V7 2 +15V DGND 45 DGND
-15V7 3 -15V O_UFLOW 44 OUFLOW7
SIG7SH1 4 S&H_IN1 D15! 43
SIG7SH2 5 S&H_IN2 D15 42 ADC7_D15
SIG7SH3 6 S&H_IN1 D14 41 ADC7_D14
POST7RTN 7 SIG_RTN D13 40 ADC7_D13
8 NC D12 39 ADC7_D12
AGND 9 AGND D11 38 ADC7_D11
+15V7 10 +15V D10 37 ADC7_D10
-15V7 11 -15V D9 36 ADC7_D9
12 NC D8 35 ADC7_D8
AGND 13 OFFSET_ADJ D7 34 ADC7_D7
AGND14 AGND D6 33 ADC7_D6
AGND 15 GAIN_ADJ D5 32 ADC7_D5
16 +REF D4 31 ADC7_D4
17 -REF D3 30 ADC7_D3
AGND18 AGND D2 29 ADC7_D2
TRIG7 19 TRIGGER D1 28 ADC7_D1
DGND 20 DGND D0 27 ADC7_D0
DGND21 DGND XFER7 26 XFER7
DGND22 DGND +5V 25 +5V7
DGND23 HIBYTEN! DGND 24 DGND
LOBYTEN!

U32 74ACT574
OE7 1 OC
XFER7 11 CLK
1Q 19 RB_D15
2Q 18 RB_D14
ADC7_D15 2 1D 3Q 17 RB_D13
ADC7_D14 3 2D 4Q 16 RB_D12
ADC7_D13 4 3D 5Q 15 RB_D11
ADC7_D12 5 4D 6Q 14 RB_D10
ADC7_D11 6 5D 7Q 13 RB_D9
ADC7_D10 7 6D 8Q 12 RB_D8
ADC7_D9 8 7D
ADC7_D8 9 8D

U31 74ACT574
OE7 1 OC
XFER7 11 CLK
1Q 19 RB_D7
2Q 18 RB_D6
ADC7_D7 2 1D 3Q 17 RB_D5
ADC7_D6 3 2D 4Q 16 RB_D4
ADC7_D5 4 3D 5Q 15 RB_D3
ADC7_D4 5 4D 6Q 14 RB_D2
ADC7_D3 6 5D 7Q 13 RB_D1
ADC7_D2 7 6D 8Q 12 RB_D0
ADC7_D1 8 7D
ADC7_D0 9 8D

POST8 R8 50
C120 100pF

+15V L22 27.5uH +15V8
C102 0.1uF + C104 6.8uF 20V + C106 6.8uF,20V C108 0.1uF
AGND AGND
C103 0.1uF + C105 AGND 6.8uF 20V 6.8uF,20V + C107 C109 0.1uF
-15V L23 27.5uH -15V8
JP8 HEADER1X3

+5V L24 27.5uH +5V8
+ C119 10uF 20V C117 10uF 20V +
DGND DGND

+5V
C116 0.1uF C118 0.1uF
DGND

SIG8SH1
SIG8SH2
SIG8SH1
C110 47pF

U29 HI201HS
RNG1 1 A1
2 OUT1 A2 16 RNG1!
3 IN1 OUT2 15
14 IN2 SIG8SH2
-15V 4 V- V+ 13 +15V
AGND 5 AGND NC 12
SIG8SH1 6 IN4 IN3 11 SIG8SH3
7 OUT4 OUT3 10 POST8RTN
RNG2 8 A4 A3 9 RNG2!
SIG8SH3

C111 47pF
AGND

POST8RTN
TRIG8 TRIG8

U30 ADC4322
AGND 1 AGND +5V 46 +5V8
+15V8 2 +15V DGND 45 DGND
-15V8 3 -15V O_UFLOW 44 OUFLOW8
SIG8SH1 4 S&H_IN1 D15! 43
SIG8SH2 5 S&H_IN2 D15 42 ADC8_D15
SIG8SH3 6 S&H_IN1 D14 41 ADC8_D14
POST8RTN 7 SIG_RTN D13 40 ADC8_D13
8 NC D12 39 ADC8_D12
AGND 9 AGND D11 38 ADC8_D11
+15V8 10 +15V D10 37 ADC8_D10
-15V8 11 -15V D9 36 ADC8_D9
12 NC D8 35 ADC8_D8
AGND 13 OFFSET_ADJ D7 34 ADC8_D7
AGND14 AGND D6 33 ADC8_D6
AGND 15 GAIN_ADJ D5 32 ADC8_D5
16 +REF D4 31 ADC8_D4
17 -REF D3 30 ADC8_D3
AGND18 AGND D2 29 ADC8_D2
TRIG8 19 TRIGGER D1 28 ADC8_D1
DGND 20 DGND D0 27 ADC8_D0
DGND21 DGND XFER8 26 XFER8
DGND22 DGND +5V 25 +5V8
DGND23 HIBYTEN! DGND 24 DGND
LOBYTEN!

U34 74ACT574
OE8 1 OC
XFER8 11 CLK
1Q 19 RB_D15
2Q 18 RB_D14
ADC8_D15 2 1D 3Q 17 RB_D13
ADC8_D14 3 2D 4Q 16 RB_D12
ADC8_D13 4 3D 5Q 15 RB_D11
ADC8_D12 5 4D 6Q 14 RB_D10
ADC8_D11 6 5D 7Q 13 RB_D9
ADC8_D10 7 6D 8Q 12 RB_D8
ADC8_D9 8 7D
ADC8_D8 9 8D

U33 74ACT574
OE8 1 OC
XFER8 11 CLK
1Q 19 RB_D7
2Q 18 RB_D6
ADC8_D7 2 1D 3Q 17 RB_D5
ADC8_D6 3 2D 4Q 16 RB_D4
ADC8_D5 4 3D 5Q 15 RB_D3
ADC8_D4 5 4D 6Q 14 RB_D2
ADC8_D3 6 5D 7Q 13 RB_D1
ADC8_D2 7 6D 8Q 12 RB_D0
ADC8_D1 8 7D
ADC8_D0 9 8D

BACK ANNOTATED

Title: 8 CHANNEL ADC BOARD
Size: B
Number: 700-155-01
Revision: LAYOUT
Date: 26-Aug-1997
File: F:\PROTEL\..\ADC8_5.SCH
Sheet of 5 OF XX
Drawn By: PETER ONAKA

RESET S1

U22
/MR +5V
NC NC
NC /RESET
DGND RESET
MAX701CSA

PB 512-0008-00

BDRESET!

+5V

C124 0.1uF   C125 0.1uF
DGND

RB_RD!
RB_D[0..15]
RB_SD[0..7]

+5V
C130 0.1uF   C126 0.1uF
DGND

ECO RDSDx TO RB_SDX

JTAG HEADER
J1
TCK   1 2   DGND
TDO   3 4   +5V
TMS   5 6
          7 8
TDI   9 10 DGND
HEADER 5X2

+5V
10K R1 R2 R3 R4 R5 R6 R7 R8

U17
EPM7128QC(160)

NC, VCCIO, TDI_JTAG, IOB30, IOB29, IOB28, IOB27, IOB25, IOB24, IOB23, IOB22, GND, IOB21, IOB20, IOB19, IOB17, TMS_JTAG, IOC46, IOC45, IOC44, VCCIO, IOC43, IOC41, IOC40, IOC38, IOC37, IOC36, IOC35, NC...

TDO_JTAG, IOG110, IOG109, IOG108, IOG107, IOG105, IOG104, IOG102, VCCIO, IOG101, IOG100, IOG99, IOG97, TCK_JTAG, IOF94, IOF93, IOF92, GND, IOF91, IOF89, IOF88, IOF86, IOF85, IOF84, IOF83, NC...

TDI, OUFLOW1, OE1, OE2, OE3, OE4, TRIG1, TRIG2, DGND, TRIG3, TRIG4, DIAG1, DIAG2, TMS, DIAG3, DIAG4, RNG1, +5V, RNG1!, RNG2, RNG2!, TRIG5, TRIG6, TRIG7, TRIG8

DGND, TDO, RB_SD2, RB_SD3, RB_SD4, RB_SD5, RB_SD6, RB_SD7, CONFIG0, +5V, CONFIG1, CONFIG2, CONFIG3, CONFIG4, TCK, CONFIG5, CONFIG6, CONFIG7, DGND, CB_WR!, CB_D0, CB_D1, CB_D2, CB_D3, CB_D4, CB_D5

TEST HEADER
JH1
1 2
3 4   DIAG1
5 6   DIAG2
7 8
9 10 DIAG3
11 12 DIAG4
13 14
15 16
17 18
19 20 DGND
HEADER 10X2

LD1 371-0017-00
LD2 371-0017-00
LD3 371-0017-00
LD4 371-0017-00
DGND

OE[1..8]
OUFLOW[1..8]
RNG_CTL

CONFIGURATION HEADER
JH2
CONFIG0 1 2   DGND
CONFIG1 3 4
CONFIG2 5 6
CONFIG3 7 8
CONFIG4 9 10
CONFIG5 11 12
CONFIG6 13 14
CONFIG7 15 16
HEADER 8X2
DGND

+5V
C127 0.1uF   C129 0.1uF
DGND

+5V
C128 0.1uF   C131 0.1uF
DGND

CB_WR!
CB_D[0..15]
CB_CW[0..7]

BACK ANNOTATED

Title: 8 CHANNEL ADC BOARD
Size: B
Number: 700-155-01
Revision: LAYOUT
Date: 26-Aug-1997
File: F:\PROTEL\..\ADC8_6.SCH
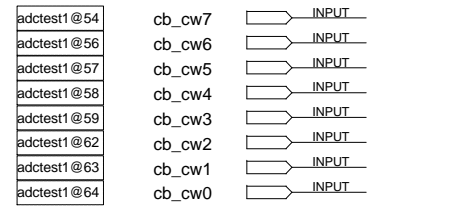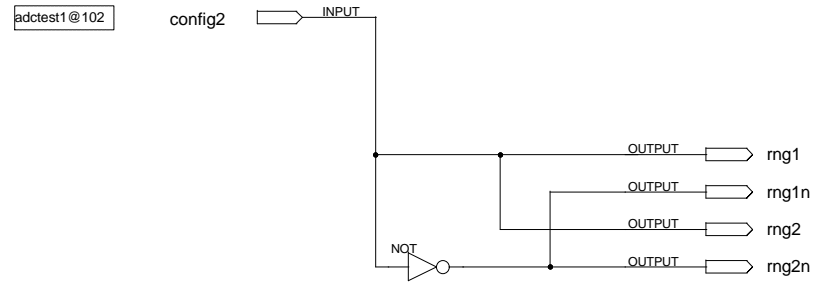Sheet of 6 OF XX
Drawn By: PETER ONAKA

ADVANCED DESIGN SYSTEMS--BILL OF MATERIALS
700-0155-01 / 171-0143-01
8-CHANNEL A-to-D CONVERTER BOARD
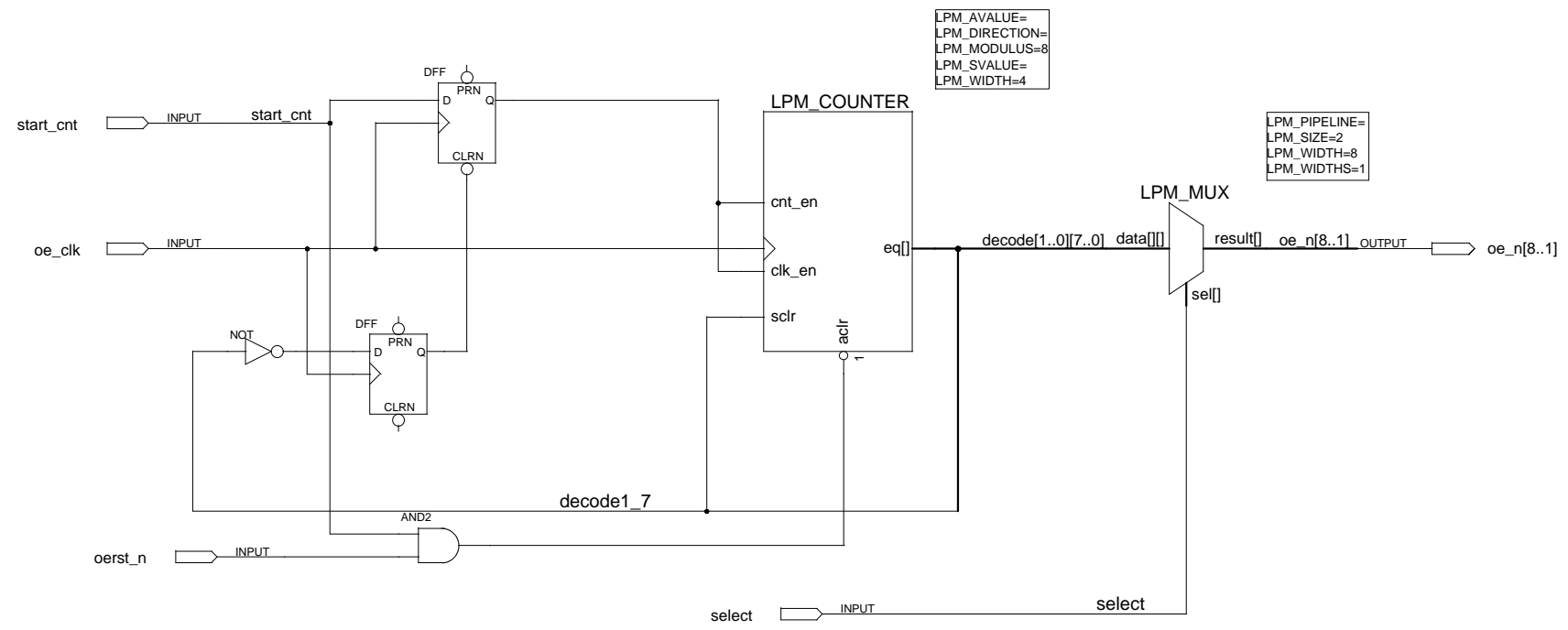
Note 1: Substitute part for P/N 185-0010-00 is P/N 185-0010-01 which is Inductor, 33 uH,Q=50@2.52MHz
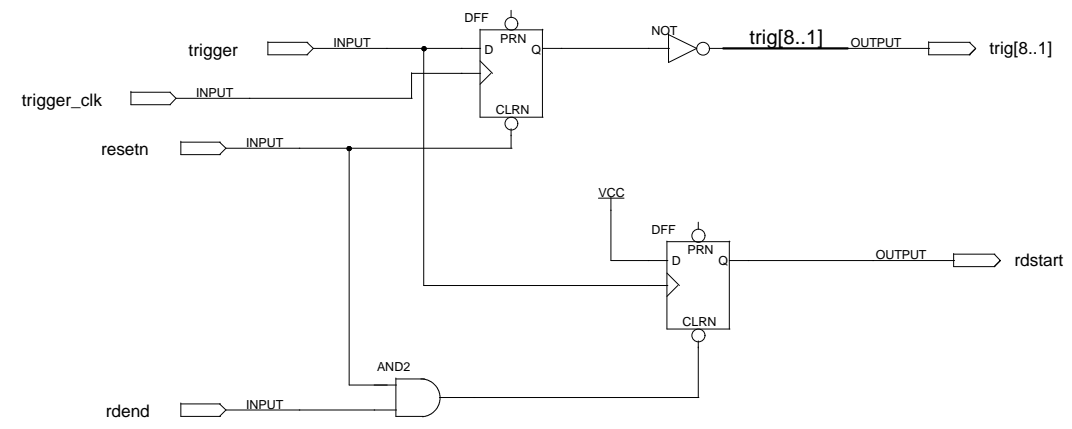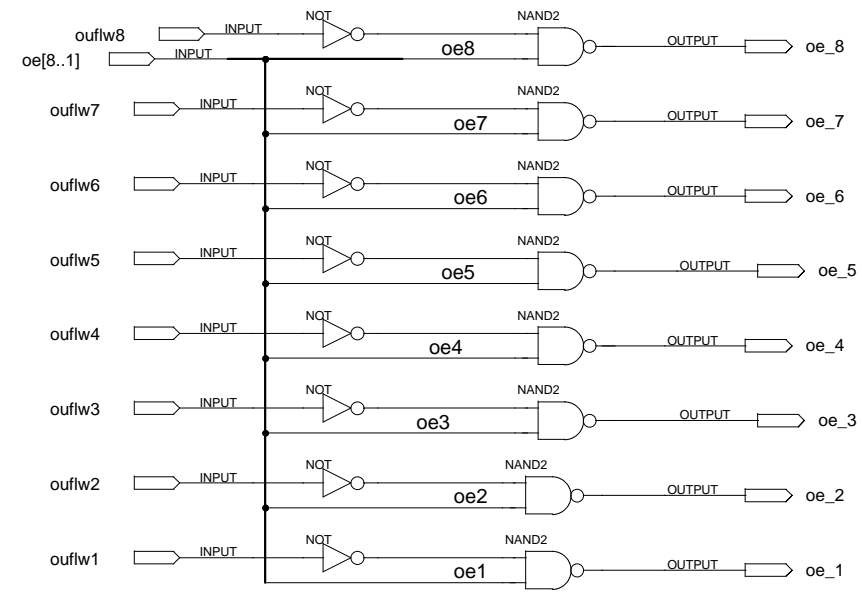
Part Number	Part Description	U/M	QTY	Vendor #1	Vendor1 PN	Vendor #2	Vendor2 PN	Reference Designator
130-0002-00	Pot'd ADC,16-bit,2MHz Smp-Rate,1.5X2.4X0.23	EA	8	Analogic	ADC4322	Analogic	ADC4322	U5,U8,U9,U12,U23,U26,U27,U30
141-0008-00	Front Panel for Vortec 2-Height VME Boards	EA	1	Zero(Scanbe)	32027	RoseElectric	32027	FP1
157-0014-02	Cap,SMD,M-lyr,npo,Cer,47pF,50V,5%,ADS1206	EA	16	Panasonic	ECU-V1H470JCM	DigiKey282n	PCC470CCT-ND	C9,C10,C19,C20,C40,C41,C50,
157-0014-02	Cap,SMD,M-lyr,npo,Cer,47pF,50V,5%,ADS1206	EA	0	Panasonic	ECU-V1H470JCM	DigiKey282n	PCC470CCT-ND	C51,C69,C70,C79,C80,C100,
157-0014-02	Cap,SMD,M-lyr,npo,Cer,47pF,50V,5%,ADS1206	EA	0	Panasonic	ECU-V1H470JCM	DigiKey282n	PCC470CCT-ND	C101,C110,C111
157-0017-02	Cap,SMD,M-lyr,npo,Cer,100pF,50V,5%,ADS1206	EA	8	Panasonic	ECU-V1H101JCM	DigiKey282n	PCC100VCT-ND	C29,C30,C31,C52,C89,C90,C91
157-0017-02	Cap,SMD,M-lyr,npo,Cer,100pF,50V,5%,ADS1206	EA	0	Panasonic	ECU-V1H101JCM	DigiKey282n	PCC100VCT-ND	C120
157-0044-02	Cap,SMD,M-lyr,Ceram,0.1uF,50V,10%,ADS1206	EA	56	Panasonic	ECU-V1H104KBW	DigiKey282n	PCC104BCT-ND	C2,C4,C6,C8,C11,C12,C17,C18,
157-0044-02	Cap,SMD,M-lyr,Ceram,0.1uF,50V,10%,ADS1206	EA	0	Panasonic	ECU-V1H104KBW	DigiKey282n	PCC104BCT-ND	C21,C22,C27,C28,C32,C33,C38,
157-0044-02	Cap,SMD,M-lyr,Ceram,0.1uF,50V,10%,ADS1206	EA	0	Panasonic	ECU-V1H104KBW	DigiKey282n	PCC104BCT-ND	C39,C42,C43,C48,C49,C53,C55,
157-0044-02	Cap,SMD,M-lyr,Ceram,0.1uF,50V,10%,ADS1206	EA	0	Panasonic	ECU-V1H104KBW	DigiKey282n	PCC104BCT-ND	C57,C59,C62,C64,C66,C68,C71,
157-0044-02	Cap,SMD,M-lyr,Ceram,0.1uF,50V,10%,ADS1206	EA	0	Panasonic	ECU-V1H104KBW	DigiKey282n	PCC104BCT-ND	C72,C77,C78,C81,C82,C87,C88,
157-0044-02	Cap,SMD,M-lyr,Ceram,0.1uF,50V,10%,ADS1206	EA	0	Panasonic	ECU-V1H104KBW	DigiKey282n	PCC104BCT-ND	C92,C93,C98,C99,C102,C103,
157-0044-02	Cap,SMD,M-lyr,Ceram,0.1uF,50V,10%,ADS1206	EA	0	Panasonic	ECU-V1H104KBW	DigiKey282n	PCC104BCT-ND	C108,C109,C112,C114,C116,
157-0044-02	Cap,SMD,M-lyr,Ceram,0.1uF,50V,10%,ADS1206	EA	0	Panasonic	ECU-V1H104KBW	DigiKey282n	PCC104BCT-ND	C118,C124,C125,C126,C127,
157-0044-02	Cap,SMD,M-lyr,Ceram,0.1uF,50V,10%,ADS1206	EA	0	Panasonic	ECU-V1H104KBW	DigiKey282n	PCC104BCT-ND	C128,C129,C130,C131
158-0042-00	Cap,SMD,Tantalum, 6.8uF,20V,20%,ADS6032P	EA	32	Panasonic	ECS-T1DC685R	DigiKey261n	PCS4685CT-ND	C13,C14,C15,C16,C23,C24,C25,
158-0042-00	Cap,SMD,Tantalum, 6.8uF,20V,20%,ADS6032P	EA	0	Panasonic	ECS-T1DC685R	DigiKey261n	PCS4685CT-ND	C26,C34,C35,C36,C37,C44,C45.
158-0042-00	Cap,SMD,Tantalum, 6.8uF,20V,20%,ADS6032P	EA	0	Panasonic	ECS-T1DC685R	DigiKey261n	PCS4685CT-ND	C46,C47,C73,C74,C75,C76,C83,
158-0042-00	Cap,SMD,Tantalum, 6.8uF,20V,20%,ADS6032P	EA	0	Panasonic	ECS-T1DC685R	DigiKey261n	PCS4685CT-ND	C84,C85,C86,C94,C95,C96,C97,
158-0042-00	Cap,SMD,Tantalum, 6.8uF,20V,20%,ADS6032P	EA	0	Panasonic	ECS-T1DC685R	DigiKey261n	PCS4685CT-ND	C104,C105,C106,C107
158-0043-00	Cap,SMD,Tantalum, 10uF,20V,20%,ADS6032P	EA	16	Panasonic	ECS-T1DC106R	DigiKey261n	PCS4106CT-ND	C1,C3,C5,C7,C54,C56,C58,C60,
158-0043-00	Cap,SMD,Tantalum, 10uF,20V,20%,ADS6032P	EA	0	Panasonic	ECS-T1DC106R	DigiKey261n	PCS4106CT-ND	C61,C63,C65,C67,C113,C115,
158-0043-00	Cap,SMD,Tantalum, 10uF,20V,20%,ADS6032P	EA	0	Panasonic	ECS-T1DC106R	DigiKey261n	PCS4106CT-ND	C117,C119
158-0049-00	Cap,SMD,Tantalum, 22uF,25V,20%,ADS1600	EA	3	Panasonic	ECS-T1ED226R	DigiKey261n	PCS5226CT-ND	C121,C122,C123
171-0143-01	PCB, 8-Channnel A-to-D Board, 8-Lyr	EA	1	Adv Circuits	171-0143-01	Adv Circuits	171-0143-01	PCB1
185-0010-00	Indtr,27uH,Q=50@2.52MHz,43FS type, ind27sm1	EA	24	TOKO	300LS-270K	Digikey222n	TKS1230CT-ND	L1,L2,L3,L4,L5,L6,L7,L8,L9,
185-0010-00	Indtr,27uH,Q=50@2.52MHz,43FS type, ind27sm1	EA	0	TOKO	300LS-270K	Digikey222n	TKS1230CT-ND	L10,L11,L12,L13,L14,L15,
185-0010-00	Indtr,27uH,Q=50@2.52MHz,43FS type, ind27sm1	EA	0	TOKO	300LS-270K	Digikey222n	TKS1230CT-ND	L16,L17,L18,L19,L20,L21,
185-0010-00	Indtr,27uH,Q=50@2.52MHz,43FS type, ind27sm1	EA	0	TOKO	300LS-270K	Digikey222n	TKS1230CT-ND	L22,L23,L24, Note 1
213-0001-00	Socket Strip, 64-Pin,Solder Tail,1 Amp	EA	0	Preci-Dip,(M-M)	310-93-164-41-001	DigiKey93n	ED7064-ND	USE BELOW
213-0001-03	Skt Strip,3-Pin,Solder Tail--Cut Fm 213-0001-00	EA	8	AD Systems	M/F 213-0001-00	AD Systems	M/F 213-0001-00	JP1,JP2,JP3,JP4,JP5,JP6,
213-0001-03	Skt Strip,3-Pin,Solder Tail--Cut Fm 213-0001-00	EA	0	AD Systems	M/F 213-0001-00	AD Systems	M/F 213-0001-00	JP7,JP8
213-0005-00	CNX,Hdr,Brk,Male,36pin/Row,2-row,Gold-Pl,.23"Ext.	EA	0	3M	929665–09–36	Mouser135n	517-665-09-36	USE BELOW
213-0005-05	CNX,Hdr,Brk,Male,5-pin/Row,2-row,PCB,.235"Ext.	EA	1	AD Systems	M/F 213–0005-00	AD Systems	M/F 213-0005-00	J1
213-0005-08	CNX,Hdr,Brk,Male,8-pin/Row,2-row,PCB,.235"Ext.	EA	1	AD Systems	M/F 213–0005-00	AD Systems	M/F 213-0005-00	JH2
213-0005-10	CNX,Hdr,Brk,Male,10-pin/Row,2-row,PCB,.235"Ext.	EA	1	AD Systems	M/F 213–0005-00	AD Systems	M/F 213-0005-00	JH1
213-0007-01	CNX,DIN,Male,96-Pin,Rt-Ang,3-Row X 32,PCB	EA	2	Hirose Electric	PCN10-96P-2.54DS	DigiKey86n	H 5096-ND	P1,P2
213-0031-00	CNX,Hdr,Male,0.1",1 x 5-pin,FrictionLock,Strait	EA	1	Molex/Waldom	22-23-2051(pkg10)	Mouser143H	538-22-23-2051	P3
213-0330-00	CNX-strip,0.1",24 pins/row,1row,0.175"Hi,Strait	EA	16	Samtec	SS-124-G-2	Samtec	SS-124-G-2	U5,U8,U9,U12,U23,U26,U27,U30
312-0083-08	74ACT574,IC,3-State Oct D F/F,EdgTrig,Soic20	EA	16	Motorola	MC74ACT574DW	Newark46n	MC74ACT574DW	U1,U2,U3,U4,U13,U14,U15,U16,
312-0083-08	74ACT574,IC,3-State Oct D F/F,EdgTrig,Soic20	EA	0	Motorola	MC74ACT574DW	Newark46n	MC74ACT574DW	U18,U19,U20,U21,U31,U32,U33,
312-0083-08	74ACT574,IC,3-State Oct D F/F,EdgTrig,Soic20	EA	0	Motorola	MC74ACT574DW	Newark46n	MC74ACT574DW	U34

ADVANCED DESIGN SYSTEMS--BILL OF MATERIALS
700-0155-01 / 171-0143-01
8-CHANNEL A-to-D CONVERTER BOARD

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Date: 10/26/1999
6:15:55 PM

Note 1: Substitute part for P/N 185-0010-00 is P/N 185-0010-01 which is Inductor, 33 uH,Q=50@2.52MHz

Part Number	Part Description	U/M	QTY	Vendor #1	Vendor1 PN	Vendor #2	Vendor2 PN	Reference Designator
314-0060-00	ADG201HSKR,HiSpeed Quad SPST Sw,Soic16	EA	8	AnalogDevices	ADG201HSKR	ADC-Lawrie	ADG201HSKR	U6,U7,U10,U11,U24,U25,U28,
314-0060-00	ADG201HSKR,HiSpeed Quad SPST Sw,Soic16	EA	0	AnalogDevices	ADG201HSKR	ADC-Lawrie	ADG201HSKR	U29
314-0060-01	HI6-0201 HS-5,HiSpeed Quad SPST Sw,Soic16	EA	8	Maxim	HI6-0201 HS-5	DigiKey144n	H I 6-020 I HS-5-ND	U6,U7,U10,U11,U24,U25,U28,
314-0063-00	MAX701CSA, Pwr/Supply Monitor w/reset,Soic8	EA	1	Maxim	MAX701CSA	DigiKey147n	MAX701CSA-ND	U22
315-0004-01	EPM7128,CmplexProgLogDev,100ns,Qfp160sm	EA	1	Altera	EPM7128S QCI 6 O-10	ArrowAdvant	EPM7128SQCI 6 O-10	U17
371-0017-00	LED, Red,Submin,Rt-Ang,>1"spac,5V,Sgl,3ma	EA	4	Dialight	555-2007	Newark210	25F893	LD1,LD2,LD3,LD4
477-0011-02	10-Pin Sip Termination,9ea,10K Resistors,2% Tol.	EA	1	Panasonic	EXB-F10E103G	DigiKey297n	Q9103-ND	SR1
478-0510-82	Res,SM,200pkg, 51 ohm,1/8W,5%,ADS1206	EA	8	Panasonic	ERJ-8GCYJ510M	DigiKey290n	P 51 EMG-ND	R1,R2,R3,R4,R5,R6,R7,R8
512-0003-00	Sw,Mom,Rt-Ang,50ma@20VDC,SPST,PCB Mt.	EA	1	C&K Comp'nts	TP11SH8ABE	DigiKey333n	CKN4002-ND	S1

start_cnt   INPUT   start_cnt

DFF
PRN
D   Q
CLRN

LPM_AVALUE=
LPM_DIRECTION=
LPM_MODULUS=8
LPM_SVALUE=
LPM_WIDTH=4

LPM_COUNTER

LPM_PIPELINE=
LPM_SIZE=2
LPM_WIDTH=8
LPM_WIDTHS=1

cnt_en

oe_clk   INPUT

clk_en

LPM_MUX

sclr   aclr   eq[]   decode[1..0][7..0]   data[][]   result[]   oe_n[8..1]   OUTPUT   oe_n[8..1]

1

NOT
DFF
PRN
D   Q
CLRN

sel[]

decode1_7

AND2
oerst_n   INPUT

select   INPUT   select
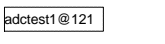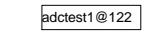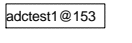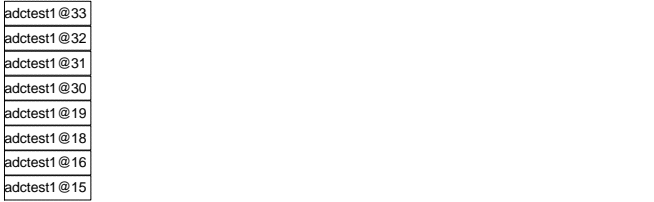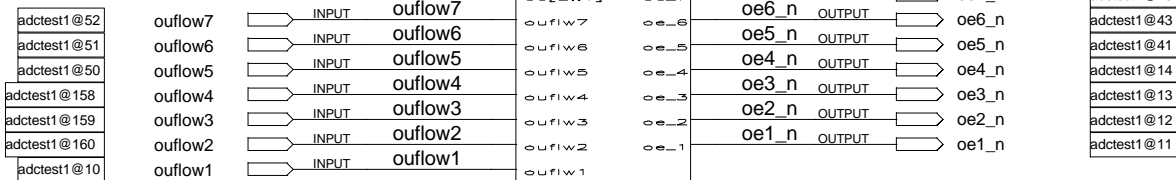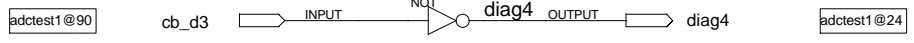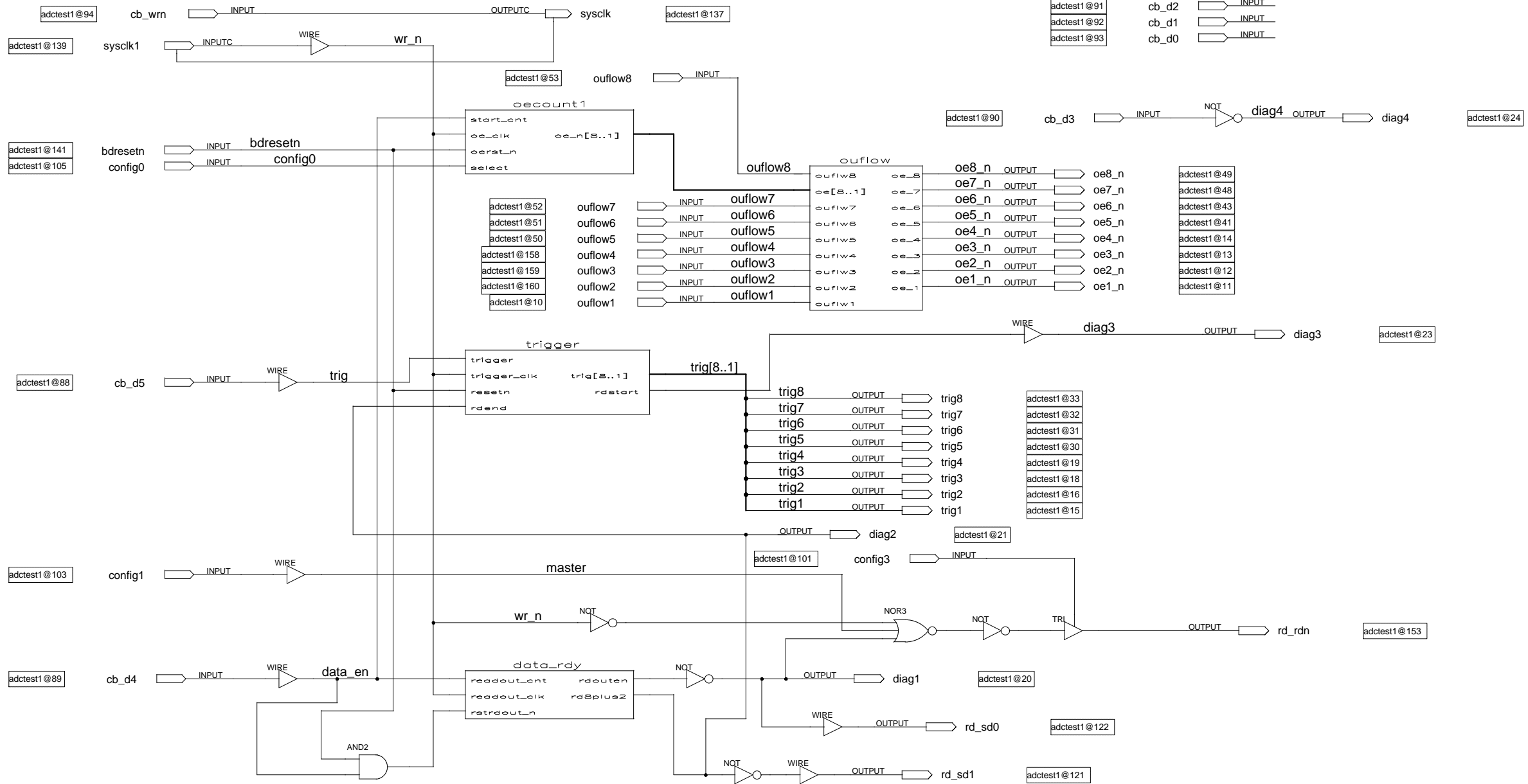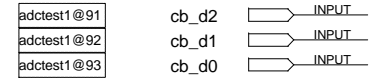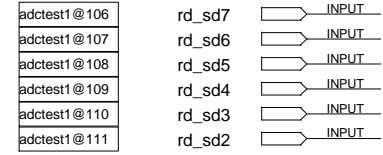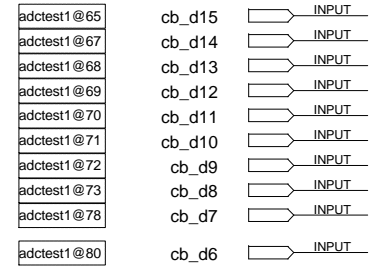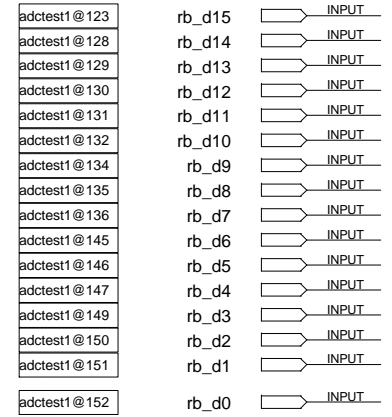
Very High Speed 16-Bit, Sampling A/D Converters

in a Space-Saving 46-Pin Hybrid Package

Introduction

The ADC4320, ADC4322, and ADC4325 are complete 16-bit, 1 MHz, 2 MHz, and 500 kHz A/D converter subsystems with a built-in sample-and-hold amplifier in a space-saving 46-pin hybrid package. They offer pin-programmable input voltage ranges of ±2.5V, ±5V, ±10V and 0 to +10V, and have been designed for use in applications, such as ATE, digital oscilloscopes, medical imaging, radar, sonar, and analytical instrumentation, requiring high speed and high resolution front ends. The ADC4322 is capable of digitizing a 1 MHz signal at a 2 MHz sampling rate with a guarantee of no missing codes from 0°C to +70°C, or in an extended temperature range version, from –25°C to +85°C. Equally impressive in frequency domain applications, the ADC4325 features 91 dB minimum signal-to-noise ratio with input signals from DC to 100 kHz.

The ADC432X Series utilizes the latest semiconductor technologies to produce a cost-effective, high performance part in a 46-pin hybrid package. They are designed around a two-pass, sub-ranging architecture that integrates a low distortion sample-and-hold amplifier, precision voltage reference, ultra-stable 16-bit linear reference D/A converter, all necessary timing circuitry, and tri-state CMOS/TTL compatible output lines for ease of system integration.

Superior performance and ease-of-use make the ADC432X Series the ideal solution for those applications requiring a sample-and-hold amplifier directly at the input to the A/D converter. Having the S/H amplifier integrated with the A/D converter benefits the system designer in two ways. First, the S/H has been designed specifically to complement the performance of the A/D converter; for example, the acquisition time, hold mode settling and droop rate have been optimized for the A/D converter, resulting in exceptional overall performance. Second, the designer achieves

Features

- ❏ 2 MHz, 1 MHz, and 500 kHz Conversion Rates
- ❏ 16-Bit Resolution
- ❏ 0.003% Maximum Integral Nonlinearity
- ❏ No Missing Codes
- ❏ Peak Distortion: –92 dB Max. (100 kHz Input)
- ❏ Signal to Noise Ratio:
  86 dB (ADC4322) Min.
  89 dB (ADC4320) Min.
  91 dB (ADC4325) Min.
- ❏ Total Harmonic Distortion: (100 kHz Input)
  –86 dB (ADC4320) Max.
  –90 dB (ADC4325) Max.
- ❏ TTL/CMOS Compatibility
- ❏ Low Noise
- ❏ Electromagnetic/Electrostatic Shielding

Applications

- ❏ Digital Signal Processing
- ❏ Sampling Oscilloscopes
- ❏ Automatic Test Equipment
- ❏ High-Resolution Imaging
- ❏ Analytical Instrumentation
- ❏ Medical Instrumentation
- ❏ CCD Detectors
- ❏ IR Imaging
- ❏ Sonar/Radar
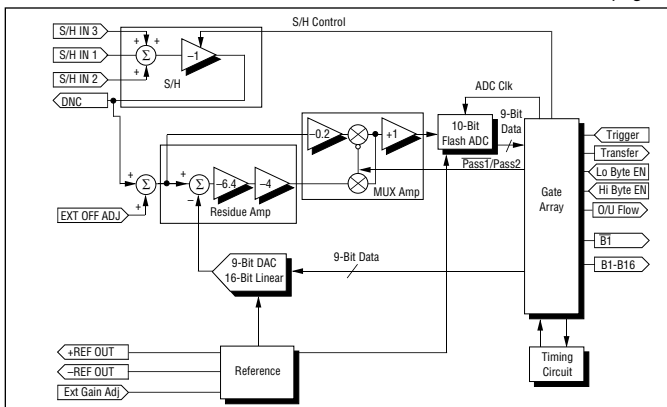
Figure 1. Functional Block Diagram.

ADC4320/ADC4322/ADC4325

Specifications[1]

SPECIFICATION	ADC4325	ADC4320	ADC4322
ANALOG INPUT			
Input Voltage Range			
Bipolar	±2.5V, ±5V, ±10V	±2.5V, ±5V, ±10V	±2.5V, ±5V, ±10V
Unipolar	0 to +10V	0 to +10V	0 to +10V
Max. Input Without Damage	±15.5V	±15.5V	±15.5V
Input Impedance			
±2.5V	750Ω	750Ω	750 Ω
±5.0V, 0-10V	1.5 KΩ	1.5 KΩ	1.5 KΩ
±10V	3 kΩ	3 kΩ	3 kΩ
Offset/Gain Adj. Sensitivity	300 ppm FSR/V	300 ppm FSR/V	300 ppm FSR/V
DIGITAL INPUTS			
Compatibility	TTL, HCT, and ACT	TTL, HCT, and ACT	TTL, HCT, and ACT
Logic "0"	+0.8V Max.	+0.8V Max.	+0.8V Max.
Logic "1"	+2.0V Min.	+2.0V Min.	+2.0V Min.
Trigger	Negative Edge Triggered	Negative Edge Triggered	Negative Edge Triggered
Loading	2 HCT Loads	2 HCT Loads	2 HCT Loads
TriggerPulse Width	100 ns Min.	100 ns Min.	50 ns Min.
High Byte Enable	Active Low, B1-B8, $\overline{B1}$	Active Low, B1-B8, $\overline{B1}$	Active Low, B1-B8, $\overline{B1}$
Low Byte Enable	Active Low, B9-B16	Active Low, B9-B16	Active Low, B9-B16
DIGITAL OUTPUTS			
Fan-Out	1 TTL Load	1 TTL Load	1 TTL Load
Logic "0"	+0.4V	+0.4V	+0.4V
Logic "1"	+2.4V	+2.4V	+2.4V
Output Coding	Binary, Offset Binary, Two's Complement	Binary, Offset Binary, Two's Complement	Binary, Offset Binary, Two's Complement
Transfer Pulse	Data valid on positive edge	Data valid on positive edge	Data valid on positive edge
Over/Under Flow	Valid = logic "0" (occurs only when ±FS have been exc'd.)	Valid = logic "0" (occurs only when ±FS have been exc'd)	Valid = logic "0" (occurs only when ±FS have been exc'd)
DYNAMIC CHARACTERISTICS[2]			
Maximum Throughput Rate	500 kHz	1.0 MHz	2.0 MHz
A/D Conversion Time	1.1 µs Typ.	620 ns Typ.	300 ns Typ.
S/H Acquisition Time	900 ns Typ.	380 ns Typ.	200 ns Typ.
S/H Aperture Delay	15 ns Max.	15 ns Max.	15 ns Max.
S/H Aperture Jitter	5 ps RMS Max.	5 ps RMS Max.	5 ps RMS Max.
S/H Feedthrough[3]	−90 dB Max.; −96 dB Typ.	−90 dB Max.; −96 dB Typ.	−90 dB Max.; −96 dB Typ.
Full Power Bandwidth	2.6 MHz Min.	3 MHz Min.	6 MHz Min.
Small Signal Bandwidth	2.6 MHz Min.	6 MHz Min.	8 MHz Min.
Signal to Noise Ratio[4]			
100 kHz Input @ 0 dB	91 dB Min.;93 dB Typ.	89 dB Min.; 92 dB Typ.	86 dB Min.; 88 dB Typ.
495 kHz Input @ −10 dB	–	79 dB Min.; 82 dB Typ.	76 dB Min.; 78 dB Typ.
980 kHz Input @ −10 dB	–	–	75 dB Min.; 78 dB Typ.
Peak Distortion[4]			
100 kHz Input @ 0 dB	−92 dB Max.; −97 dB Typ.	−92 dB Max.; −97 dB Typ.	−92 dB Max.; 97 dB Typ.
495 kHz Input @ −10 dB	–	−84 dB Max.; −95 dB Typ.	−84 dB Max.; −95 dB Typ.
980 kHz Input @ −10 dB	–	–	−81 dB Max.; −88 dB Typ.
Total Harmonic Distortion[4]			
100 kHz Input @ 0 dB	−90 dB Max.; −95 dB Typ.	−86 dB Max.; −94 dB Typ.	−86 dB Max. −94 dB Typ.
495 kHz Input @ −10 dB	–	−79 dB Max.; −86 dB Typ.	−80 dB Max.; −88 dB Typ.
980 kHz Input @ −10 dB	–	–	−80 dB Max.; −85 dB Typ.
THD + Noise[5]			
100 kHz Input @ 0 dB	88 dB Min.; 91 dB Typ.	84 dB Min.; 91 dB Typ.	83 dB Min.; 87 dB Typ.
495 kHz Input @ −10 dB	–	76 dB Min.; 81 dB Typ.	75 dB Min.; 77 dB Typ.
980 kHz Input @ −10 dB	–	–	74 dB Min.; 77dB Typ.

SPECIFICATION (CONT.)	ADC4325	ADC4320	ADC4322
Step Response[6]	800 ns Max. to 1 LSB	500 ns Max. to 1 LSB	250 ns Max. to 2 LSBs
INTERNAL REFERENCE[9]			
Voltage	+5V, ±0.5% Max.	+5V, ±0.5% Max.	+5V, ±0.5% Max.
Stability	15 ppm/°C Max.	15 ppm/°C Max.	15 ppm/°C Max.
Available Current[7]	1.0 mA Max.	1.0 mA Max.	1.0 mA Max.
TRANSFER CHARACTERISTICS			
Resolution	16 bits	16 bits	16 bits
Integral Nonlinearity	±0.003% FSR Max.; ±0.001% Typ.	±0.003% FSR Max.; ±0.001% Typ.	±0.003% FSR Max.; ±0.001% Typ
Differential Nonlinearity	±0.75 LSB; ±0.5 LSB Typ.	±0.75 LSB; ±0.5 LSB Typ.	±0.75 LSB Max.; ±0.5 LSB Typ.
Monotonicity	Guaranteed	Guaranteed	Guaranteed
No Missing Codes	Guaranteed over the Specified Temperature Range	Guaranteed over the Specified Temperature Range	Guaranteed over the Specified Temperature Range
Offset Error	±0.1% FSR Max. (Adj. to Zero)	±0.1% FSR Max. (Adj. to Zero)	±0.1% FSR Max. (Adj. to Zero)
Gain Error	±0.1% FSR Max. (Adj. to Zero)	±0.1% FSR Max. (Adj. to Zero)	±0.1% FSR Max. (Adj. to Zero)
Noise[8]			
10V p-p FSR	55 µV RMS Typ.; 70 µV RMS Max.	65 µV RMS Typ.; 80 µV RMS Max.	90 µV RMS Typ.; 110 µV Max.
5V p-p FSR	45 µV RMS Typ.; 55 µV RMS Max.	50 µV RMS Typ.; 60 µV RMS Max.	65 µV RMS Typ., 80 µV Max.
STABILITY			
Differential Nonlinearity TC	±1 PPM/°C MAX.	±1 PPM/°C MAX	.±1 PPM/°C MAX.
Offset TC	±15 ppm/°C Max.	±15 ppm/°C Max.	±15 ppm/°C Max.
Gain TC	±15 ppm/°C Max.	±15 ppm/°C Max.	±15 ppm/°C Max.
Warm-Up Time	5 Min. Max.	5 Min. Max.	5 Min. Max.
Supply Rejection per % change in any supply Offset & Gain	±10 ppm/% Max.	±10 ppm/% Max.	±10 ppm/% Max.
POWER REQUIREMENTS			
±15V Supplies[9]	14.55V Min., 15.45V Max.	14.55V Min., 15.45V Max.	14.55V Min., 15.45V Max.
+5V Supplies	+4.75V Min., +5.25V Max.	+4.75V Min., +5.25V Max.	+4.75V Min., +5.25V Max.
+15V Current Drain	63 mA Typ.	63 mA Typ.	71 mA Typ.
−15V Current Drain	54 mA Typ.	54 mA Typ.	61 mA Typ.
+5V Current Drain	67 mA Typ.	67 mA Typ.	67 mA Typ.
Total Power Consumption	2.1W Typ.	2.1W Typ.	2.3W Typ.
ENVIRONMENTAL & MECHANICAL			
Specified Temp. Range[10]			
A Version	0°C to +70°C	0°C to +70°C	0°C to +70°C
B Version	−25°C to +85°C	−25°C to +85°C	−25°C to +85°C
Storage Temp. Range	−25°C to 125°C	−25°C to 125°C	−25°C to 125°C
Dimensions	1.58" x 2.38" x 0.225" (40.13 mm x 60.45 mm x 5.7 mm)	1.58" x 2.38" x 0.225" (40.13 mm x 60.45 mm x 5.7 mm)	1.58" x 2.38" x 0.225" (40.13 mm x 60.45 mm x 5.7 mm)
Case Potential	Ground	Ground	Ground

NOTES:

1. All specifications guaranteed at 25°C unless otherwise noted and supplies at ±15V and +5V.

2. All dynamic characteristics measured on the ±5V input range except the 980 kHz distortion test are performed at the ±2.5V input range.

3. Measured with a full scale step input.

4. See performance testing.

5. THD + noise represents the ratio of the RMS value of the signal to the total RMS noise below the Nyquist plus the total harmonic distortion up to the 100th harmonic with an analysis bandwidth of DC to the converters' Nyquist frequency.

6. Step response represents the time required to achieve the specified accuracies after an input full scale step change.

7. Reference Load to remain stable.

8. Includes noise from S/H and A/D converter.

9. Both ±15V analog supply voltages and both ±reference voltages, Pins 2, 3, 16, and 17 must be by-passed with low ESR tantalum capacitors (see Figure 20).

10. The specified temperature range is guaranteed for the case temperature.

Specifications subject to change without notice.

TYPICAL PERFORMANCE CHARACTERISTICS
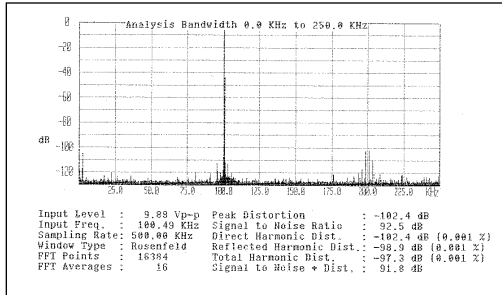
Fig. 2. ADC4325 Dynamic Characteristics at 100 kHz and 0 dB
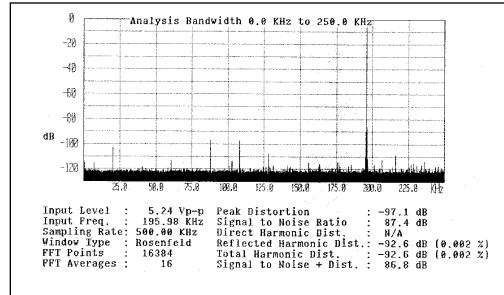
Fig. 6. ADC4325 Dynamic Characteristics at 195 kHz and –6 dB (±5V Range)
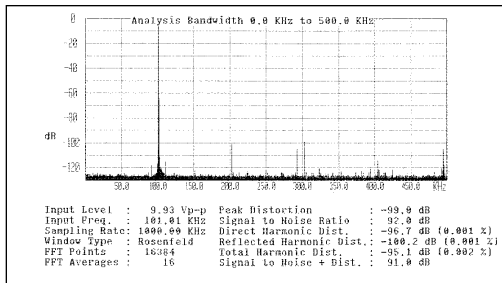
Fig. 3. ADC4320 Dynamic Characteristics at 100 kHz and 0 dB
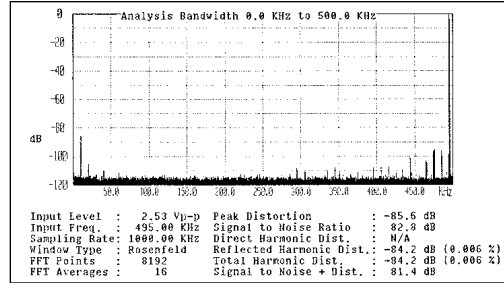
Fig. 7. ADC4320 Dynamic Characteristics at 495 kHz and –6 dB Range.
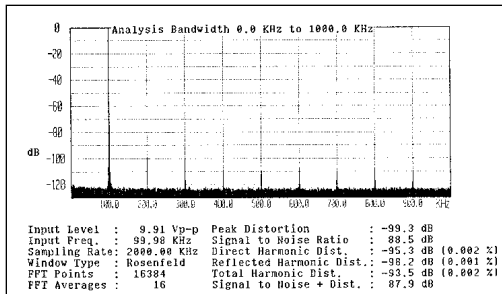
Fig. 4. ADC4322 Dynamic Characteristics at 100 kHz and 0 dB
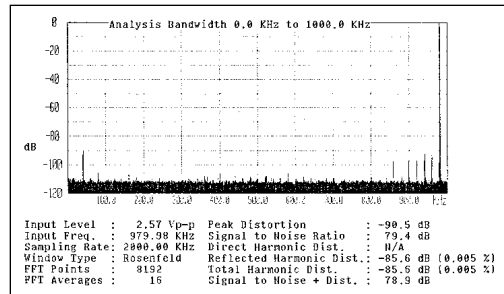
Fig. 8. ADC4322 Dynamic Characteristics at 980 kHz and –6 dB (±2.5V Range)
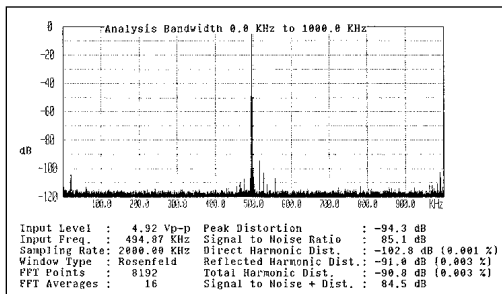
Fig. 5. ADC4322 Dynamic Characteristics at 495 kHz and 0 dB (±2.5V Range)
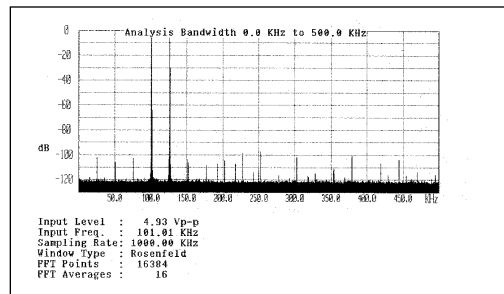
Fig. 9. ADC4320 Intermodulation Distortion at 100 kHz, 125 kHz and –6 dB

SPECIFICATIONS
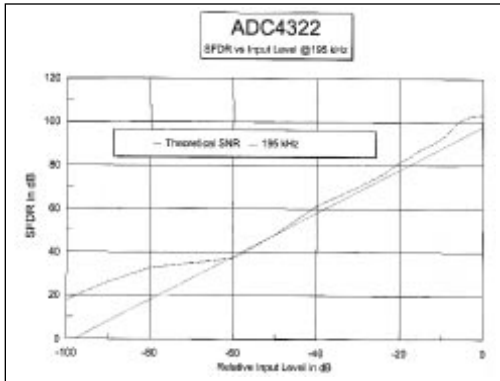
Figure 10. ADC4322 SFDR vs Input Level @ 195 kHz ±2.5V Range
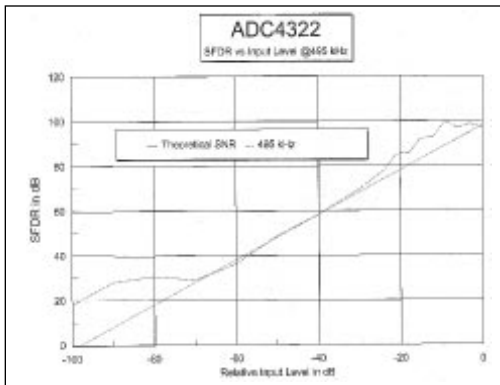
Figure 11. ADC4322 SFDR vs Input Level @ 495 kHz ±2.5V Range
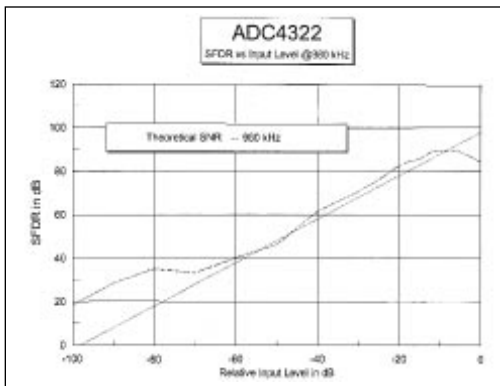
Figure 12. ADC4322 SFDR vs Input Level @ 980 kHz ±2.5V Range

PIN #	4	5	6
RANGE	S/H IN 1	S/H IN2	S/H IN 3
0V to +10V	Input	Input	–5V Ref
±5V	Input	Input	SIG RTN
±2.5V	Input	Input	Input
±10V	Input	SIG RTN	SIG RTN

Figure 13. Input Scaling Connections.

true 16-bit performance, avoiding degradation due to ground loops, signal coupling, jitter and digital noise introduced when separate S/H and A/D converters are interconnected. Furthermore, the accuracy, speed, and quality of the ADC432X Series are fully ensured by thorough, computer-controlled factory tests of each unit.

INTERFACING

Input Scaling

The converters can be configured for four input voltage ranges: 0 to +10V; ±2.5V; ±5V; and ±10V. The analog input range should be scaled as close as possible to the maximum input to utilize the full dynamic range of the converter. Figure 13 describes the input connections.

Coding and Trim Procedure

Figure 15 shows the output coding and trim calibration voltages of the converter. For two's complement operation, simply use the available $\overline{B1}$ ($\overline{MSB}$) instead of B1 (MSB). Refer to Figure 14 for use of external offset and gain trim potentiometers. Voltage DACs with a ±5V output can be utilized easily when digital control is required. The input sensitivity of the external offset and gain control pins is 300 ppm FSR/V. If Offset and Gain adjusts are not used, connect them to Pin 14, Analog Returns.

To trim the offset of the converter, apply the offset voltage shown in Figure 15 for the appropriate voltage range. Adjust the offset trim potentiometer such that the 15 MSBs are "0" and the LSB alternates equally between "0" and "1" for the unipolar ranges or all 16 bits are in transition for the bipolar ranges.

To trim the gain of the converter, apply the range (+FS) voltage shown in Figure 15 for the appropriate range. Adjust the gain trim potentiometer such that the 15 MSBs are "1" and the LSB alternates equally between "0" and "1".
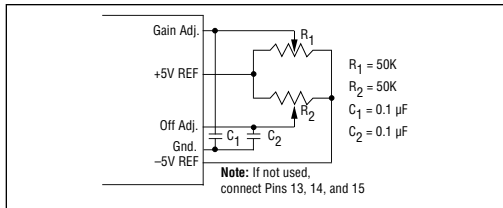
Figure 14. Offset and Gain Adjustment Circuit.

$R_1 = 50K$
$R_2 = 50K$
$C_1 = 0.1 \mu F$
$C_2 = 0.1 \mu F$

Note: If not used, connect Pins 13, 14, and 15

UNIPOLAR BINARY		0V TO +10V	
	MSB LSB		
+FS	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 *	= +9.99977V	
1/2 FS	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	= +5.00000V	
Offset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 *	= +0.00000V	
OFFSET BINARY		**±2.5V Input**	**±5V Input**
	MSB LSB		
+FS	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 *	= +2.49989V	+4.99977V
Offset	* * * * * * * * * * * * * * * *	= −0.00004V	−0.00008V
−FS	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 *	= −2.49996V	−4.99992V
2'S COMPLEMENT		**±2.5V Input**	**±5V Input**
	MSB LSB		
+FS	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 *	= +2.49989V	+4.99977V
Offset	* * * * * * * * * * * * * * * *	= −0.00004V	−0.00008V
−FS	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 *	= −2.49996V	−4.99992V

* denotes a 0/1 or 1/0 transition

Figure 15. Coding and Trim Calibration Table.
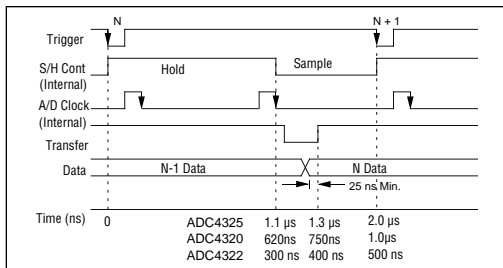
Figure 16. Timing Diagram.

	ADC4325		
ADC4325	1.1 µs	1.3 µs	2.0 µs
ADC4320	620ns	750ns	1.0µs
ADC4322	300 ns	400 ns	500 ns
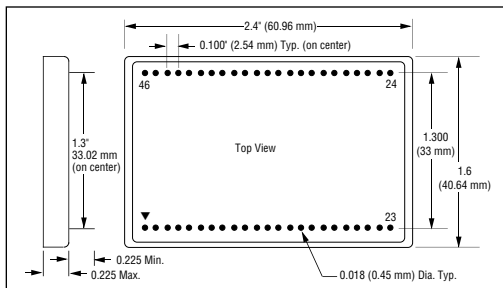
Figure 17. ADC432X Series Mechanical Diagram.

PIN #		PIN#	
1	ANA RTN	46	+5V
2	+15V	45	DIG RTN
3	−15V	44	O/U FLOW
4	S/H IN 1	43	BIT 1N
5	S/H IN 2	42	BIT 1
6	S/H IN 3	41	BIT 2
7	SIG RTN	40	BIT 3
8	DNC*	39	BIT 4
9	ANA RTN	38	BIT 5
10	+15V	37	BIT 6
11	−15V	36	BIT 7
12	DNC	35	BIT 8
13	EXT OFFSET ADJ	34	BIT 9
14	ANA RTN	33	BIT 10
15	EXT GAIN ADJ	32	BIT 11
16	+REF OUT	31	BIT 12
17	−REF OUT	30	BIT 13
18	ANA RTN	29	BIT 14
19	TRIGGER	28	BIT 15
20	DIG RTN	27	BIT 16
21	DIG RTN	26	TRANSFER
22	HI BYTE EN	25	+5V
23	LO BYTE EN	24	DIG RTN

* DNC– Do Not Connect

Figure 18. Pin Assignment.

To check the trim procedure, apply 1/2 full scale voltage for a unipolar range or –full scale voltage for the bipolar ranges and check that the digital code is ±1 LSB of the stated code.

PRINCIPLE OF OPERATION

The ADC432X Series converters are 16-bit sampling A/D converters with throughput rates of up to 2 MHz. These converters are available in three externally configured full scale ranges of 5V p-p, 10V p-p and 20V p-p. Options are externally or user-programmable for bipolar and unipolar inputs of ±2.5V, ±5V, ±10V and 0 to +10V. Two's complement format can be obtained by utilizing $\overline{B1}$ instead of B1.
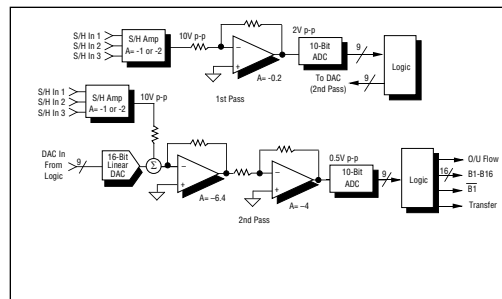
Figure 19. Operating Principle.

To understand the operating principles of the A/D converters, refer to the timing diagram of Figure 16 and the simplified block diagram of Figure 19. The simplified block diagram illustrates the two successive passes in the sub-ranging scheme of the converters.

The A/D converter is factory-trimmed and optimized to operate with a 10V p-p input voltage range. Scaling resistors at the S/H inputs configure the three input ranges and provide a S/H output voltage to the A/D converter of 10V p-p.

The first pass starts with a high-to-low transition of the trigger pulse. This signal places the S/H into the Hold mode and starts the timing logic. The path of the 10V p-p input signal during the first pass is through a 5:1 attenuator circuit to the 10-bit ADC with an input range of 2V p-p. At 35 ns, the ADC converts the signal and the 9 bits are latched both into the logic as the MSBs and into the 16-bit accurate DAC for the second pass.

The second pass subtracts the S/H output and the 9-bit, 16-bit accurate DAC output with the result equal to the 9-bit quantization error of the DAC, or 19.5 mV p-p. The "error" voltage is then amplified by a gain of 25.6 and is now 0.5V p-p or 1/4 the full scale range of the ADC, allowing a 2-bit overlap safety margin. When the DAC and the "error" amplifier have had sufficient time to settle to 16-bit accuracy, the amplified "error" voltage is then digitized by the ADC with the 9-bit second pass result latched into the logic. At this time the S/H returns to the sample mode to begin acquiring the next sample.

The 1/4 full scale range in the second pass produces a 2-bit overlap of the two passes. This provides an output word that is accurate and linear to 16 bits. This method corrects for any gain and linearity errors in the amplifying circuitry, as well as the 10-bit flash A/D converter. Without the use of this overlapping correction scheme, it would be necessary that all the components in the converters be accurate to the 16-bit level. While such a design might be possible to realize on a laboratory benchtop, it would be clearly impractical to achieve on a production basis. The key to the conversion technique used in the converters is the 16-bit accurate and 16-bit linear D/A converter which serves as the reference element for the conversion's second pass. The use of proprietary sub-ranging architecture in the converters results in a sampling A/D converter that offers unprecedented speed and transfer characteristics at the 16-bit level.

The converter has a 3-state output structure. Users can enable the eight MSBs and B1 with $\overline{\text{HIBYTEN}}$ and the eight LSBs with $\overline{\text{LOBYTEN}}$ (both are active low). This feature makes it possible to transfer data from the converter to an 8-bit microprocessor bus. However, to prevent the coupling of high frequency noise from the microprocessor bus into the A/D converter, the output data must be buffered.

Layout Considerations

Because of the high resolution of the A/D converters, it is necessary to pay careful attention to the printed-circuit layout for the device. It is, for example, important to keep analog and digital grounds separate at the power supplies. Digital grounds are often noisy or "glitchy," and these glitches can have adverse effects on the performance of the converters if they are introduced to the analog portions of the A/D converter's circuitry. At 16-bit resolution, the size of the voltage step between one code transition and the succeeding one for a 5V full scale range is only 76 µV. It is evident that any noise in the analog ground return can result in erroneous or missing codes. It is important in the design of the PC board to configure a low-impedance ground-plane return on the printed-circuit board. It is only at this point where the analog and digital power returns should be made common.

The Analogic ADC4322 EB-1 evaluation board has been designed and laid out for optimum performance with the converter series. The board layout and schematic are shown in figures 20-22 as examples of decoupling and layout techniques.
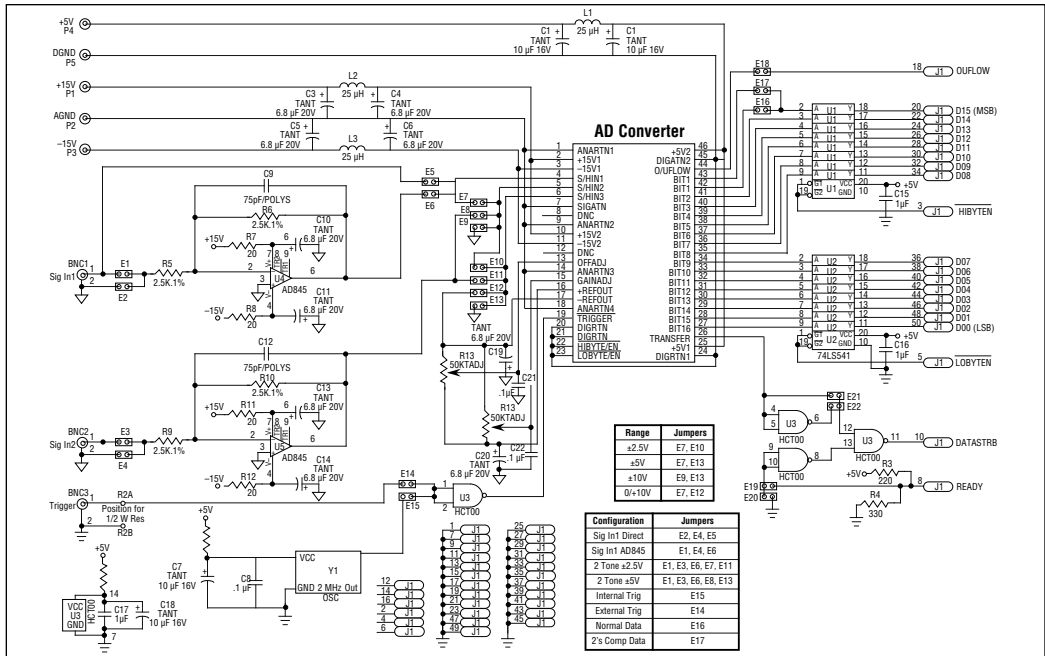
Figure 20. ADC4322-EB1 Block Diagram
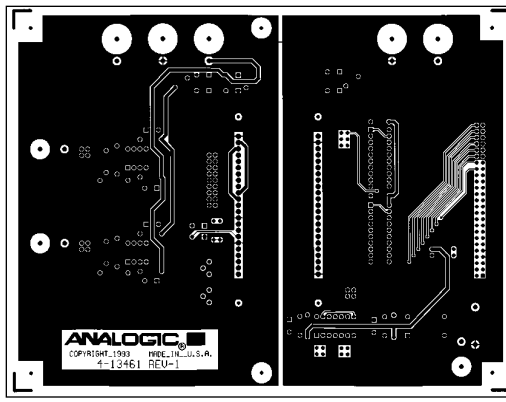
Figure 21. Primary Side
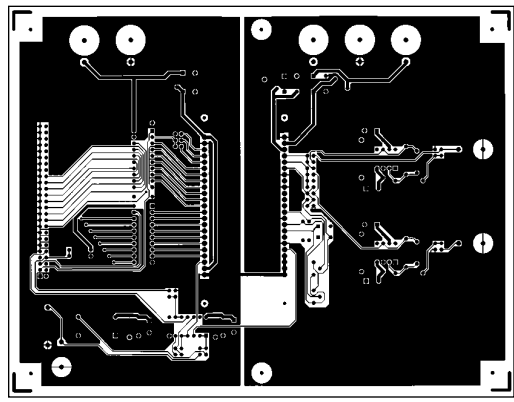
Figure 22. Secondary Side

Ordering Guide

Model	Sampling Rate
Specified Temperature Range: 0°C to +70°C	
ADC4325A	500 kHz
ADC4320A	1 MHz
ADC4322A	2 MHz
Specified Temperature Range: −25°C to +85°C	
ADC4325B	500 kHz
ADC4320B	1 MHz
ADC4322B	2 MHz
Evaluation Board	
ADC4322 EB-1	

ANALOG DEVICES

LC²MOS
High Speed, Quad SPST Switch

ADG201HS

FEATURES
50ns max Switching Time Over Full Temperature Range
Low R$_{ON}$ (30Ω typ)
Single Supply Specifications for +10.8V to +16.5V Operation
Extended Plastic Temperature Range (−40°C to +85°C)
Break-Before-Make Switching
Low Leakage (100pA typ)
44V Supply max Rating
Available in 16-Lead DIP/SOIC and 20-Lead LCCC/PLCC Packages
ADG201HS (K, B, T) Replaces HI-201HS
ADG201HS (J, A, S) Replaces DG271

GENERAL DESCRIPTION
The ADG201HS is a monolithic CMOS device comprising four independently selectable SPST switches. It is designed on an enhanced LC²MOS process which gives very fast switching speeds and low R$_{ON}$.

The switches also feature break-before-make switching action for use in multiplexer applications and low charge injection for minimum transients on the output when switching the digital inputs.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG201HSJN	−40°C to +85°C	N-16
ADG201HSKN	−40°C to +85°C	N-16
ADG201HSKR	−40°C to +85°C	R-16
ADG201HSAQ	−40°C to +85°C	Q-16
ADG201HSBQ	−40°C to +85°C	Q-16
ADG201HSJP	−40°C to +85°C	P-20A
ADG201HSKP	−40°C to +85°C	P-20A
ADG201HSSQ	−55°C to +125°C	Q-16
ADG201HSTQ[3]	−55°C to +125°C	Q-16
ADG201HSTE[3]	−55°C to +125°C	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers. See the Analog Devices Military Products Databook (1994) for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = 0.15" Small Outline IC (SOIC).
[3]Standard Military Drawing (SMD) approved by DESC. SMD numbers are
5962-86716012X (ADG201HSTE/883B)
5962-8671601EX (ADG201HSTQ/883B)

FUNCTIONAL BLOCK DIAGRAM
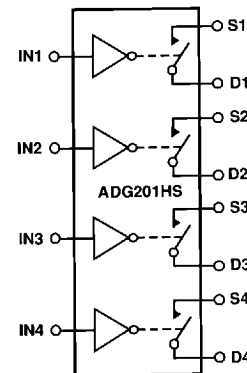
PRODUCT HIGHLIGHTS
1. **50ns max t$_{ON}$ and t$_{OFF}$:**
The ADG201HS top grades (K, B, T) have guaranteed 50ns max turn-on and turn-off times over the full operating temperature range. The lower grades (J,A,S) have guaranteed 75ns switching times over the full operating temperature range.

2. **Single Supply Specifications:**
The ADG201HS is fully specified for applications which require a single positive power supply in the +10.8V to +16.5V range.

3. **Low Leakage:**
Leakage currents in the range of 100pA make these switches suitable for high precision circuits. The added feature of break-before-make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

IN	Switch Condition
0	ON
1	OFF

Truth Table

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700   Fax: 617/326-8703

ADG201HS—SPECIFICATIONS

DUAL SUPPLY
(V_{DD} = +13.5V to +16.5V, = −13.5V to −16.5V, GND = 0V, V_{IN} 3V [Logic High Level] or 0.8 V [Logic Low Level] unless otherwise noted)

Parameter	Version	+25°C	$T_{min}-T_{max}$[1]	Units	Comments
ANALOG SWITCH					
Analog Signal Range	All	V_{SS}	V_{SS}	V min	
	All	V_{DD}	V_{DD}	V max	
R_{ON}	All	30	–	Ω typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA; Test Circuit 1
	All	50	75	Ω max	
R_{ON} Drift	All	0.5	–	%/°C typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA
R_{ON} Match	All	3	–	% typ	$-10V \leq V_S \leq +10V$, I_{DS} = 1mA
I_S (OFF), Off Input Leakage[2]	All	0.1		nA typ	V_D = ±14V; V_S = ∓14V; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (OFF), Off Output Leakage[2]	All	0.1		nA typ	V_D = ±14V; V_S = ∓14V; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (ON), On Channel Leakage[2]	All	0.1		nA typ	$V_D = V_S$ = ±14V; Test Circuit 3
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
DIGITAL CONTROL					
V_{INH}, Input High Voltage	All	2.4	2.4	V min	
V_{INL}, Input Low Voltage	All	0.8	0.8	V max	
I_{INL} or I_{INH}	All	1	1	µA max	
C_{IN}	All	8	8	pF max	
DYNAMIC CHARACTERISTICS					
t_{ON}	K, B, T	50	50	ns max	Test Circuit 4
	J, A, S	75	75	ns max	
t_{OFF1}	K, B, T	50	50	ns max	Test Circuit 4
	J, A, S	75	75	ns max	
t_{OFF2}	All	150	–	ns typ	Test Circuit 4
t_{OPEN}	All	5	5	ns typ	$t_{ON}-t_{OFF1}$; Test Circuit 4
Output Settling Time to 0.1%	All	180	–	ns typ	V_{IN} = 3V to 0V; Test Circuit 4
OFF Isolation	All	72	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 5
Channel-to-Channel Crosstalk	All	86	–	dB typ	V_S = 3V rms, f = 100kHz, R_L = 1kΩ; C_L = 10pF; Test Circuit 6
Q_{INJ}, Charge Injection	All	10	–	pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 7
C_S (OFF)	All	10	–	pF typ	
C_D (OFF)	All	10	–	pF typ	
C_D, C_S (ON)	All	30	–	pF typ	
C_{DS} (OFF)	All	0.5	–	pF typ	
POWER SUPPLY					
I_{DD}	All	10	10	mA max	
I_{SS}	All	6	6	mA max	
Power Dissipation	All	240	240	mW max	V_{DD} = +15V, V_{SS} = −15V

NOTES
[1]Temperature ranges are as follows: ADG201HSJ, K; −40°C to +85°C
ADG201HSA, B; −40°C to +85°C
ADG201HSS, T; −55°C to +125°C
[2]Leakage specifications apply with a V_D (V_S) of ±14V or with a V_D (V_S) of 0.5V within the supply voltages (V_{DD}, V_{SS}), whichever is the minimum.
Specifications subject to change without notice.

SINGLE SUPPLY ($V_{DD} = +10.8V$ to $+16.5V$, $V_{SS} =$ GND $= 0V$, $V_{IN} = 3V$ [Logic High Level] or 0.8V [Logic Low Level] unless otherwise noted)

Parameter	Version	+25°C	$T_{min} - T_{max}$	Units	Comments
ANALOG SWITCH					
Analog Signal Range	All	V_{SS}	V_{SS}	V min	
	All	V_{DD}	V_{DD}	V max	
R_{ON}	All	65	–	Ω typ	$0V \le V_S \le +10V$, $I_{DS} = 1mA$; Test Circuit 1
	All	90	120	Ω max	
R_{ON} Drift	All	0.5	–	%/°C typ	$0V \le V_S \le +10V$, $I_{DS} = 1mA$
R_{ON} Match	All	3	–	% typ	$0V \le V_S \le +10V$, $I_{DS} = 1mA$
I_S (OFF), Off Input Leakage[1]	All	0.1		nA typ	$V_D = +10V/+0.5V$; $V_S = +0.5V/+10V$; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (OFF), Off Output Leakage[1]	All	0.1		nA typ	$V_D = +10V/+0.5V$; $V_S = +0.5V/+10V$; Test Circuit 2
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
I_D (ON), On Channel Leakage[1]	All	0.1		nA typ	$V_D = V_S = +10V/+0.5V$; Test Circuit 3
	J, K, A, B	1	20	nA max	
	S, T	1	60	nA max	
DIGITAL CONTROL					
V_{INH}, Input High Voltage	All	2.4	2.4	V min	
V_{INL}, Input Low Voltage	All	0.8	0.8	V max	
I_{INL} or I_{INH}	All	1	1	μA max	
C_{IN}	All	8	8	pF max	
DYNAMIC CHARACTERISTICS					
t_{ON}	K, B, T	50	70	ns max	Test Circuit 4
	J, A, S	75	90	ns max	
t_{OFF1}	K, B, T	50	70	ns max	Test Circuit 4
	J, A, S	75	90	ns max	
t_{OFF2}	All	150	–	ns typ	Test Circuit 4
t_{OPEN}	All	5	5	ns typ	$t_{ON} - t_{OFF1}$; Test Circuit 4
Output Settling Time to 0.1%	All	180	–	ns typ	$V_{IN} = 3V$ to $0V$; Test Circuit 4
OFF Isolation	All	72	–	dB typ	$V_S = 3V$ rms, $f = 100kHz$, $R_L = 1k\Omega$; $C_L = 10pF$; Test Circuit 5
Channel-to-Channel Crosstalk	All	86	–	dB typ	$V_S = 3V$ rms, $f = 100kHz$, $R_L = 1k\Omega$; $C_L = 10pF$; Test Circuit 6
Q_{INJ}, Charge Injection	All	10	–	pC typ	$R_S = 0\Omega$, $V_S = 0V$; Test Circuit 7
C_S (OFF)	All	10	–	pF typ	
C_D (OFF)	All	10	–	pF typ	
C_D, C_S (ON)	All	30	–	pF typ	
C_{DS} (OFF)	All	0.5	–	pF typ	
POWER SUPPLY					
I_{DD}	All	10	10	mA max	
Power Dissipation	All	150	150	mW max	$V_{DD} = +15V$

NOTE
[1]The leakage specifications degrade marginally (typically 1nA at 25°C) with $V_D (V_S) = V_{SS}$.

Specifications subject to change without notice.

ADG201HS

ABSOLUTE MAXIMUM RATINGS*
($T_A = 25°C$ unless otherwise noted)

V_{DD} to V_{SS} 44V
V_{DD} to GND . . . . −0.3V, 25V
V_{SS} to GND[1] . . . . +0.3V, −25V
Analog Inputs[2]
    Voltage at S, D . . . . V_{SS} −2V to
                                  V_{DD} + 2V or
              20mA, Whichever Occurs First
Continuous Current, S or D 20mA
Pulsed Current S or D
    1ms Duration, 10% Duty Cycle 70mA
Digital Inputs[2]
    Voltage at IN . . . . V_{SS} −4V to
                                    V_{DD} + 4V or
              20mA, Whichever Occurs First

Power Dissipation (Any Package)
    Up to +75°C 470mW
    Derates above +75°C by . . . . 6mW/°C
Operating Temperature
    Commerical (J, K Version) . . . . −40°C to +85°C
    Industrial (A, B Version) . . . . −40°C to +85°C
    Extended (S, T Version) . . . . −55°C to +125°C
Storage Temperature Range . . . . −65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . +300°C

NOTES
[1]If V_{SS} is open circuited with V_{DD} and GND applied, the V_{SS} pin will be pulled positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode from V_{SS} to GND (cathode end to GND) ensures that the Absolute Maximum Ratings will be observed.
[2]Overvoltage at IN, S or D, will be clamped by diodes. Current should be limited to the maximum rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

WARNING!
ESD SENSITIVE DEVICE

PIN CONFIGURATIONS

DIP, SOIC

```
IN1  1 •        16  IN2
D1   2          15  D2
S1   3          14  S2
VSS  4  ADG201HS 13  VDD
GND  5  TOP VIEW 12  NC
        (Not to Scale)
S4   6          11  S3
D4   7          10  D3
IN4  8           9  IN3
```
NC = NO CONNECT

LCCC

```
        D1  IN1  NC  IN2  D2
         3   2    1   20  19
S1  4                      18  S2
VSS 5                      17  VDD
NC  6   ADG201HS           16  NC
GND 7   TOP VIEW           15  NC
        (Not to Scale)
S4  8                      14  S3
         9  10  11  12  13
        D4  IN4  NC  IN3  D3
```
NC = NO CONNECT

PLCC

```
        D1  IN1  NC  IN2  D2
         3   2    1   20  19
S1  4                      18  S2
VSS 5                      17  VDD
NC  6   ADG201HS           16  NC
GND 7   TOP VIEW           15  NC
        (Not to Scale)
S4  8                      14  S3
         9  10  11  12  13
        D4  IN4  NC  IN3  D3
```
NC = NO CONNECT
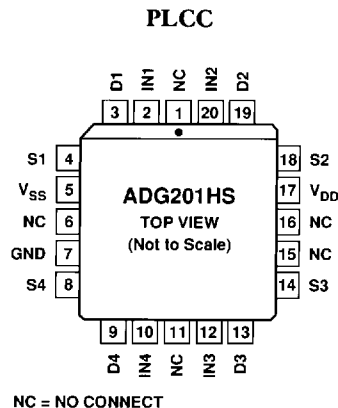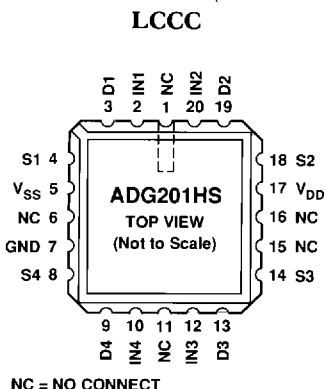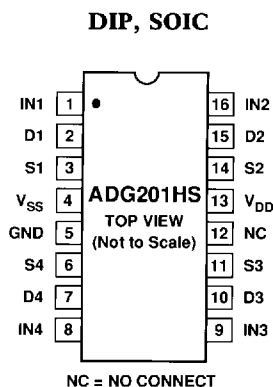
The switches are guaranteed functional with reduced single or dual supplies down to 4.5V.
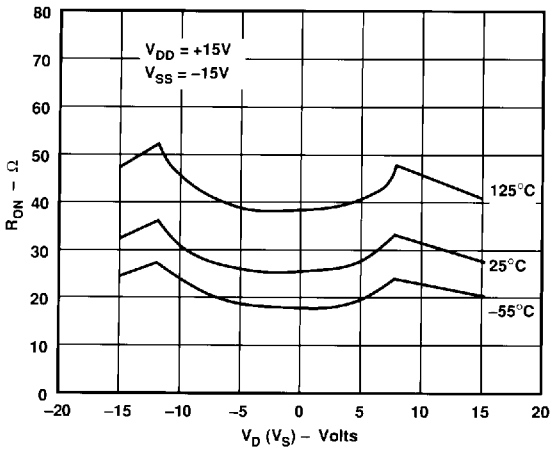
R_{ON} as a Function of V_D (V_S): Dual Supply Voltage
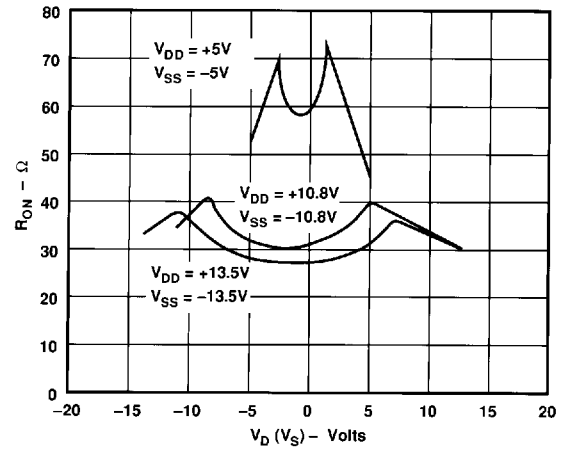
R_{ON} as a Function of V_D (V_S): Dual Supply Voltage, $T_A = +25°C$
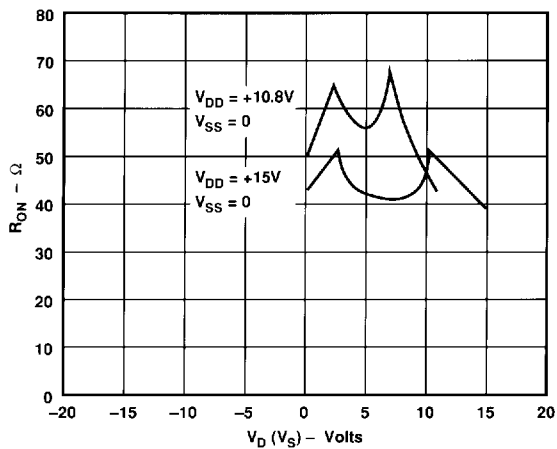
R_{ON} as a Function of V_D (V_S): Single Supply Voltage, $T_A = +25°C$
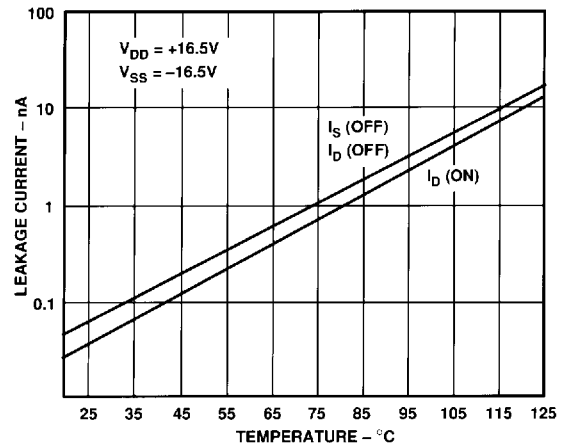
Leakage Current as a Function of Temperature Dual Supply Voltage. (Note: Leakage Currents Reduce as the Supply Voltages Reduce)
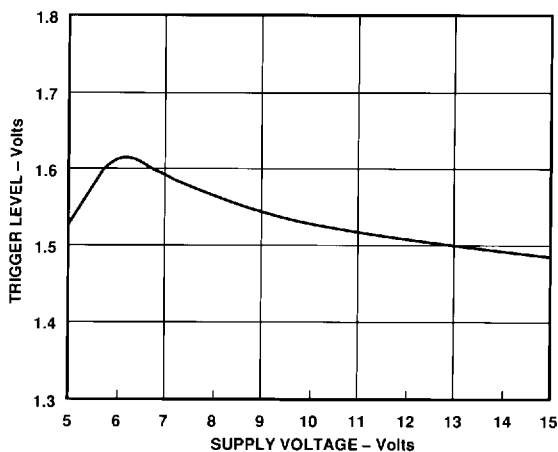
Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, $T_A = +25°C$
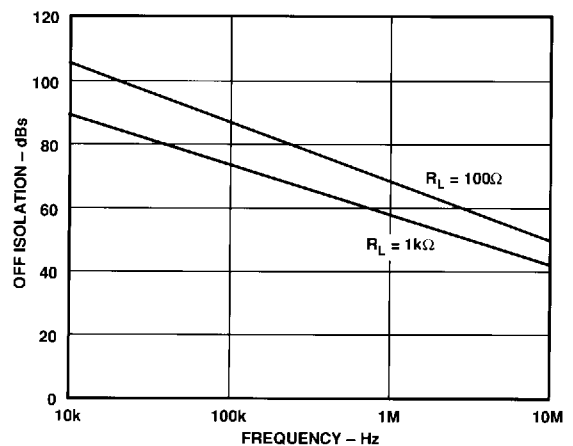
Off Isolation vs. Signal Frequency; Dual or Single 15V Supplies, $T_A = +25°C$
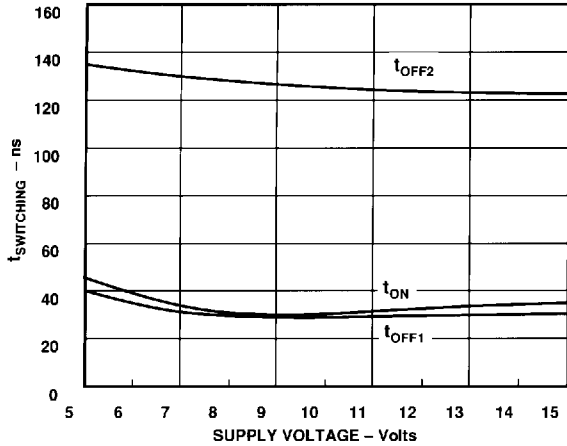
Switching Time vs. Supply Voltage (Dual Supply):
$T_A = +25°C$. (Note: See Test Circuit 4.
For $V_{DD} < 10V$, $V_S = V_{DD}$)
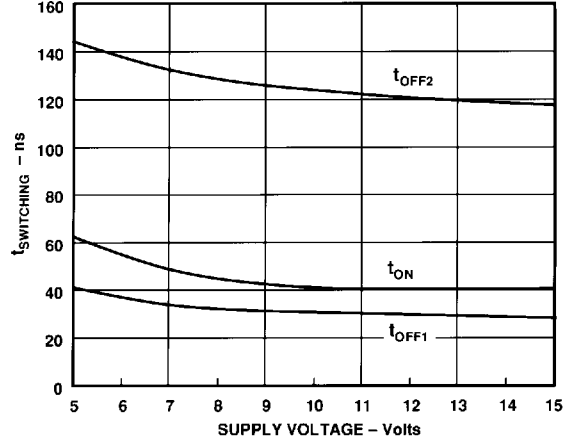
Switching Time vs. Supply Voltage (Single Supply):
$T_A = +25°C$. (Note: See Test Circuit 4.
For $V_{DD} < 10V$, $V_S = V_{DD}$)
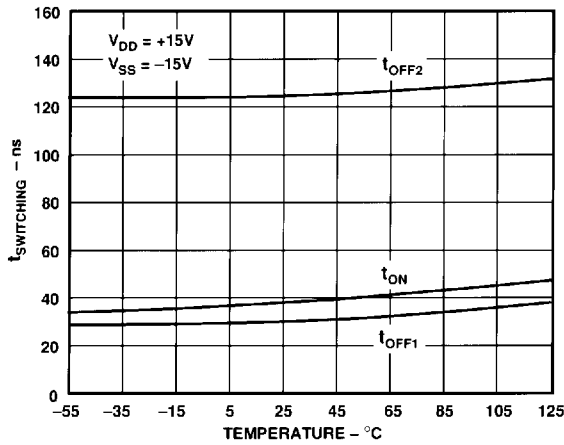
Switching Time vs. Temperature: Dual Supply Voltage
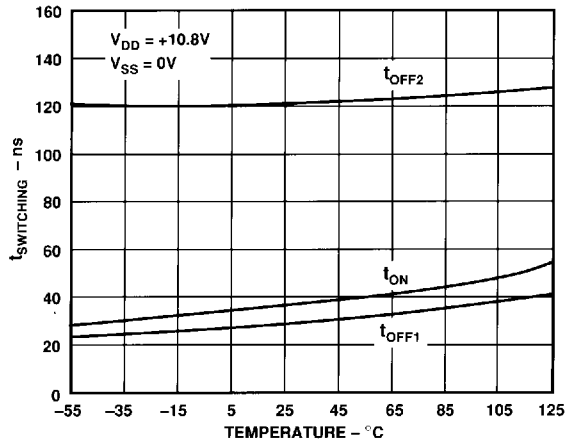
Switching Time vs. Temperature: Single Supply Voltage
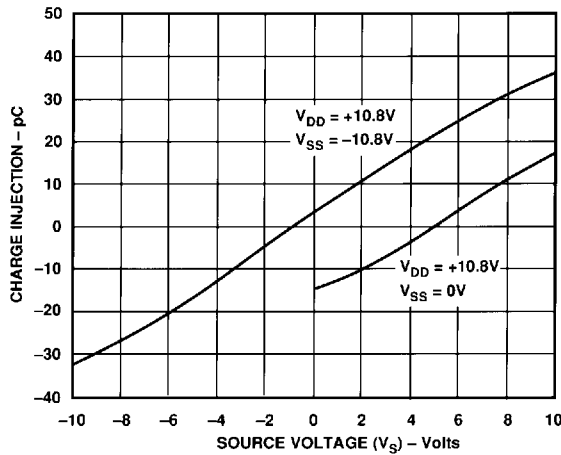
Charge Injection vs. Source Voltage (V_S) for Dual and
Single 10.8V Supplies: $T_A = +25°C$
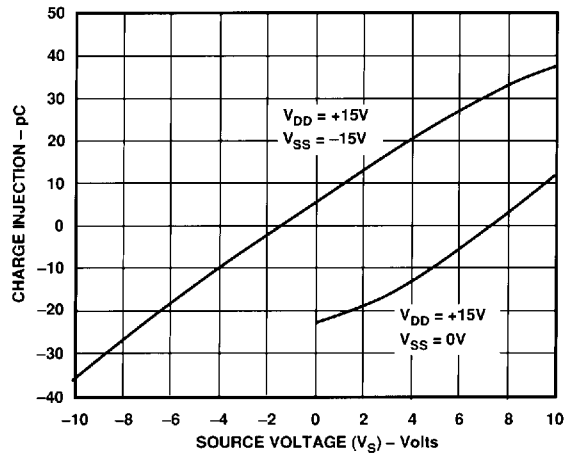
Charge Injection vs. Source Voltage (V_S) for Dual and
Single 15V Supplies: $T_A = +25°C$

REV. B

Note: All digital input signal rise and fall times measured from 10% to 90% of 3V. $t_R = t_F = 5$ns. Decoupling capacitors (0.01μF min) from V_{DD} and V_{SS} to GND are recommended to achieve specified performance.

TEST CIRCUIT 1
R_{ON}

$$R_{ON} = \frac{V1}{I_{DS}}$$
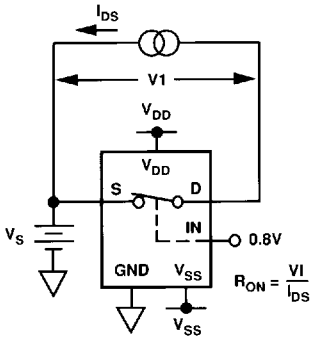
TEST CIRCUIT 2
I_S(OFF), I_D(OFF)
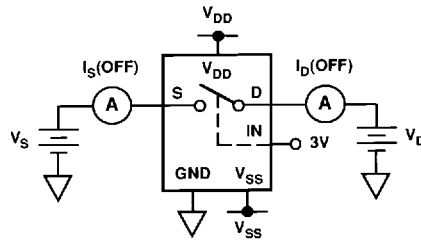
TEST CIRCUIT 3
I_D(ON)
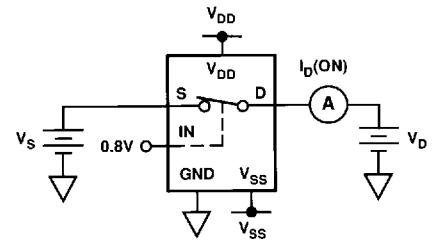
TEST CIRCUIT 4
t_{ON}, t_{OFF}, t_{OPEN}, SETTLING TIME
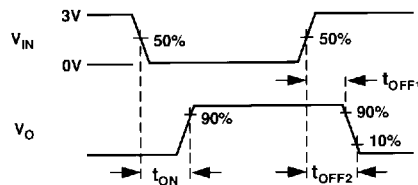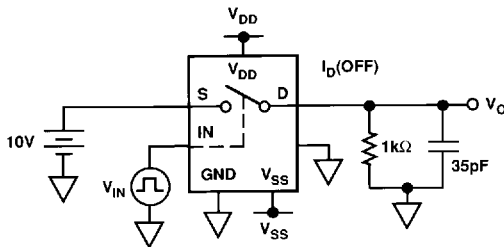
TEST CIRCUIT 5
OFF ISOLATION

OFF ISOLATION =
20 X LOG $|V_S/V_O|$
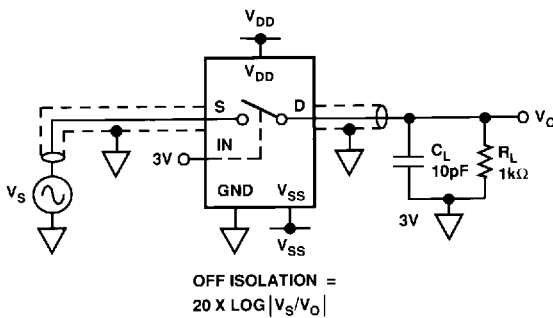
TEST CIRCUIT 6
CHANNEL-TO-CHANNEL CROSSTALK

CHANNEL ISOLATION =
20 X LOG $|V_S/V_O|$
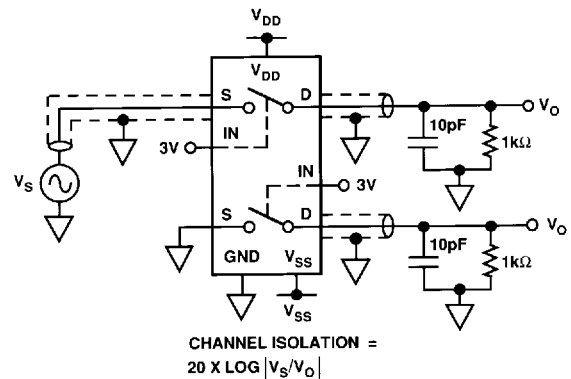
TEST CIRCUIT 7
CHARGE INJECTION

$$Q_{INJ} = C_L \times \Delta V_O$$
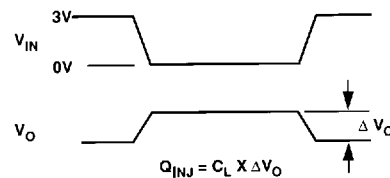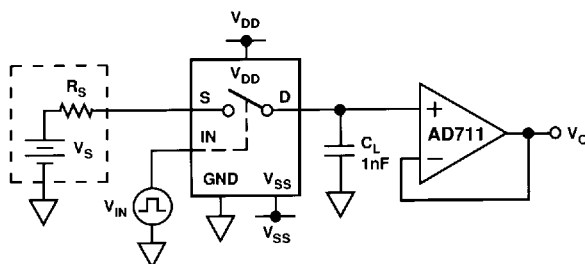
ADG201HS

SINGLE SUPPLY DISK DRIVE APPLICATION

The excellent performance of the ADG201HS with single supply operation makes it suitable in applications such as disk drives where only positive power supply voltages are normally available. The accompanying circuit shows a typical application for the ADG201HS in the read/write head switching section of a disk drive. The circuit allows data (0s and 1s) to be written to and read from a disk. The principal advantage offered by the ADG201HS is that it retains very fast switching speed with single supply operation (see Single Supply Specifications). This allows disk drives to run at higher data rates.
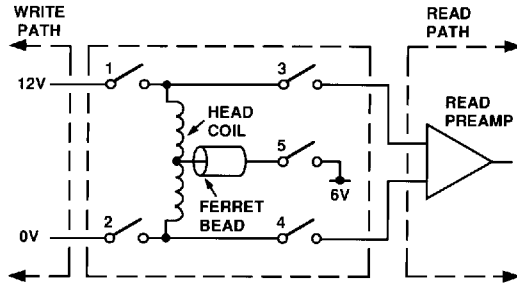
SWITCHES 1 TO 5 ALL ADG201HS

SWITCH STATES/FUNCTION

SWITCH NUMBER	WRITE "0"	WRITE "1"	READ
1	OFF	ON	OFF
2	ON	OFF	OFF
3	OFF	OFF	ON
4	OFF	OFF	ON
5	ON	ON	OFF

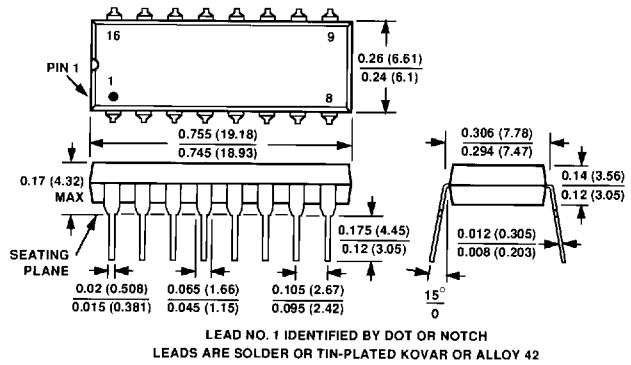*ADG201HS in the Read/Write Head Switching Circuit of a Disk Drive*

OUTLINE DIMENSIONS
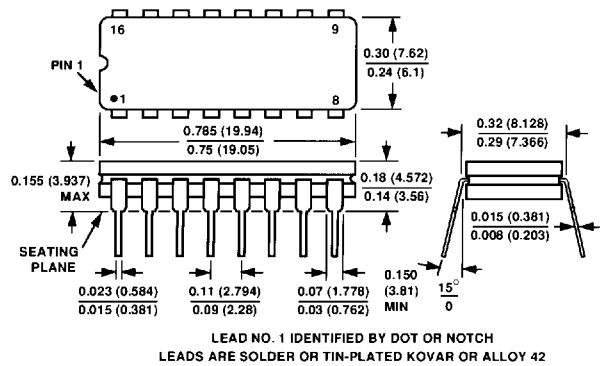
Dimensions shown in inches and (mm).

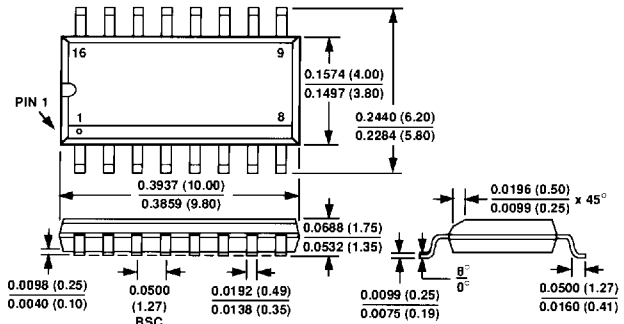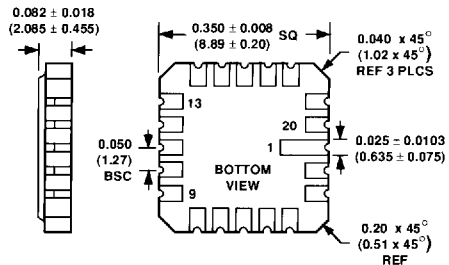### 20-Terminal Plastic Leaded Chip Carrier (P-20A)

16-Pin Plastic DIP (N-16)

LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

16-Pin Cerdip (Q-16)

LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42
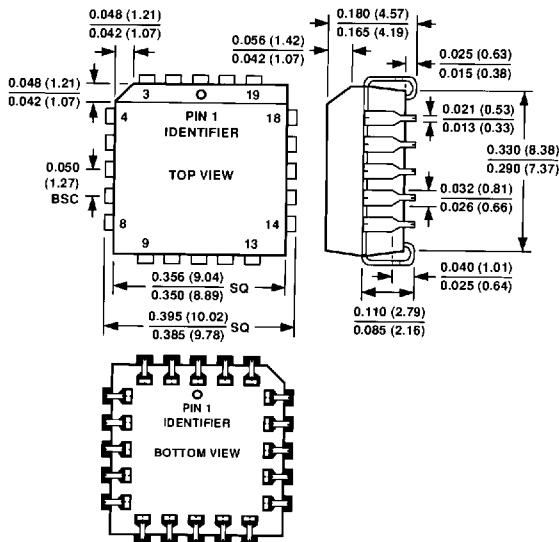
16-Lead Narrow Body SOIC (R-16A)

20-Terminal Leadless Ceramic Chip Carrier (E-20A)

C1178–10–4/88

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REV. B