CLKBIAS 700-111-01
8/16 CHANNEL CLOCK/BIAS DRIVER BOARD

CLKDRV 700-155-01
CLKBIAS DAUGHTER DRIVER BOARD

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4.1.5 CLKBIAS 700-111-01

8/16 CHANNEL CLOCK/BIAS DRIVER BOARD

4.1.5 Overview

The CLKBIAS board can be configured to output combinations of analog clock signals and/or analog bias outputs. 16 individual 12 bit digital to analog converters provide act as either bias signals or the high and low rails of an analog clock signal for driving infrared arrays. The DACs are also jumper configurable for either manual DIP switch setting or DSP programmable. Multilayer printed circuit board construction employs multiple ground/power planes for shielding.

4.1.5.1 Technical Specifications 700-111-01 CLKBIAS

- 16 individual 12 bit DACs (AD767) with buffered outputs
- Bias 30ppm/C gain drift
- Bias outputs 150mA max output current
- +/- 10 Volt output range
- Analog switch (HI201HS) based clock outputs
- 30nsec typ. 50nsec max switching times
- 6 layer PCB

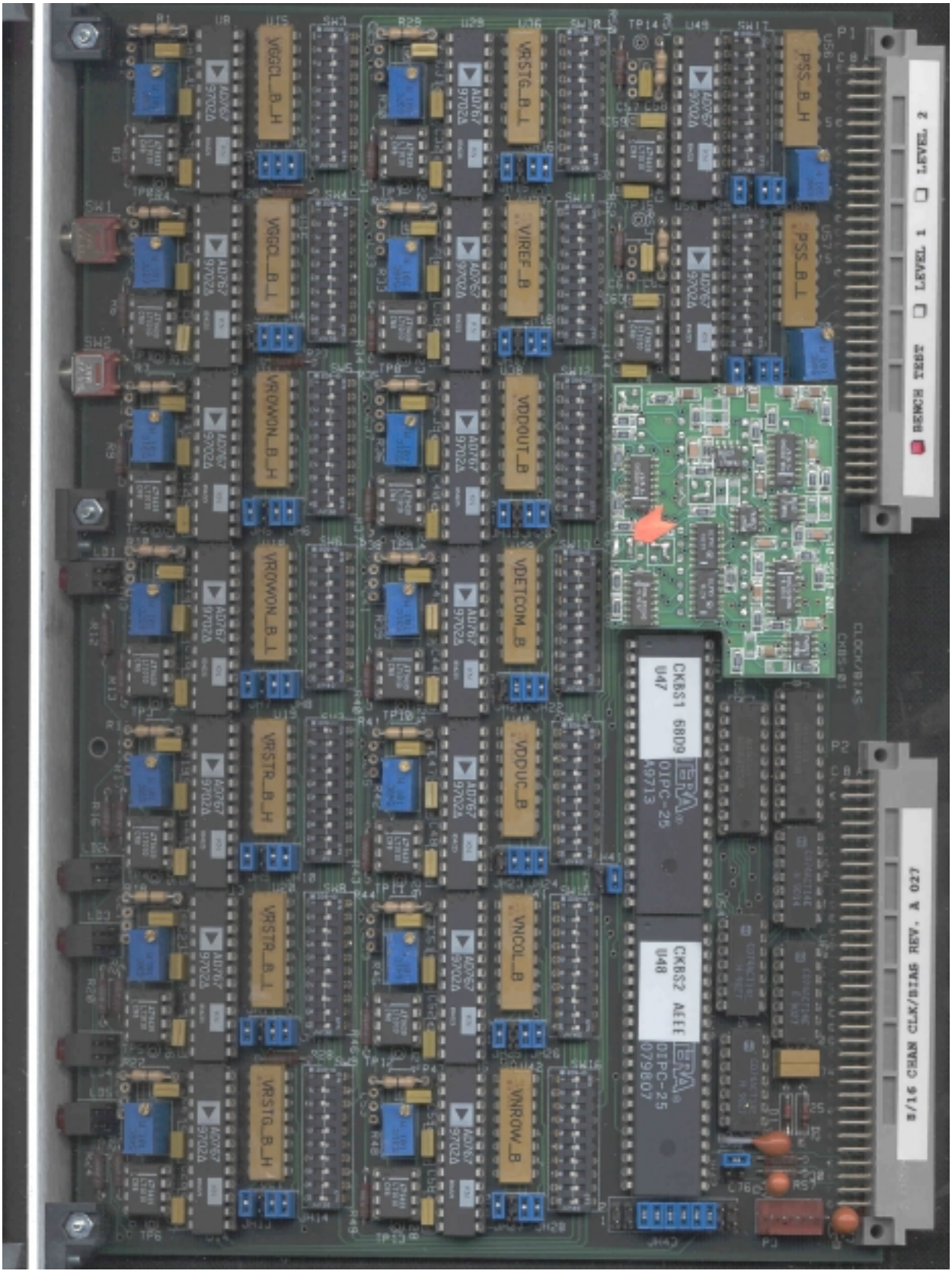
Power Requirements

- +5V 209mA Typ.
- +15V 483mA Typ.
- -15V 483mA Typ.

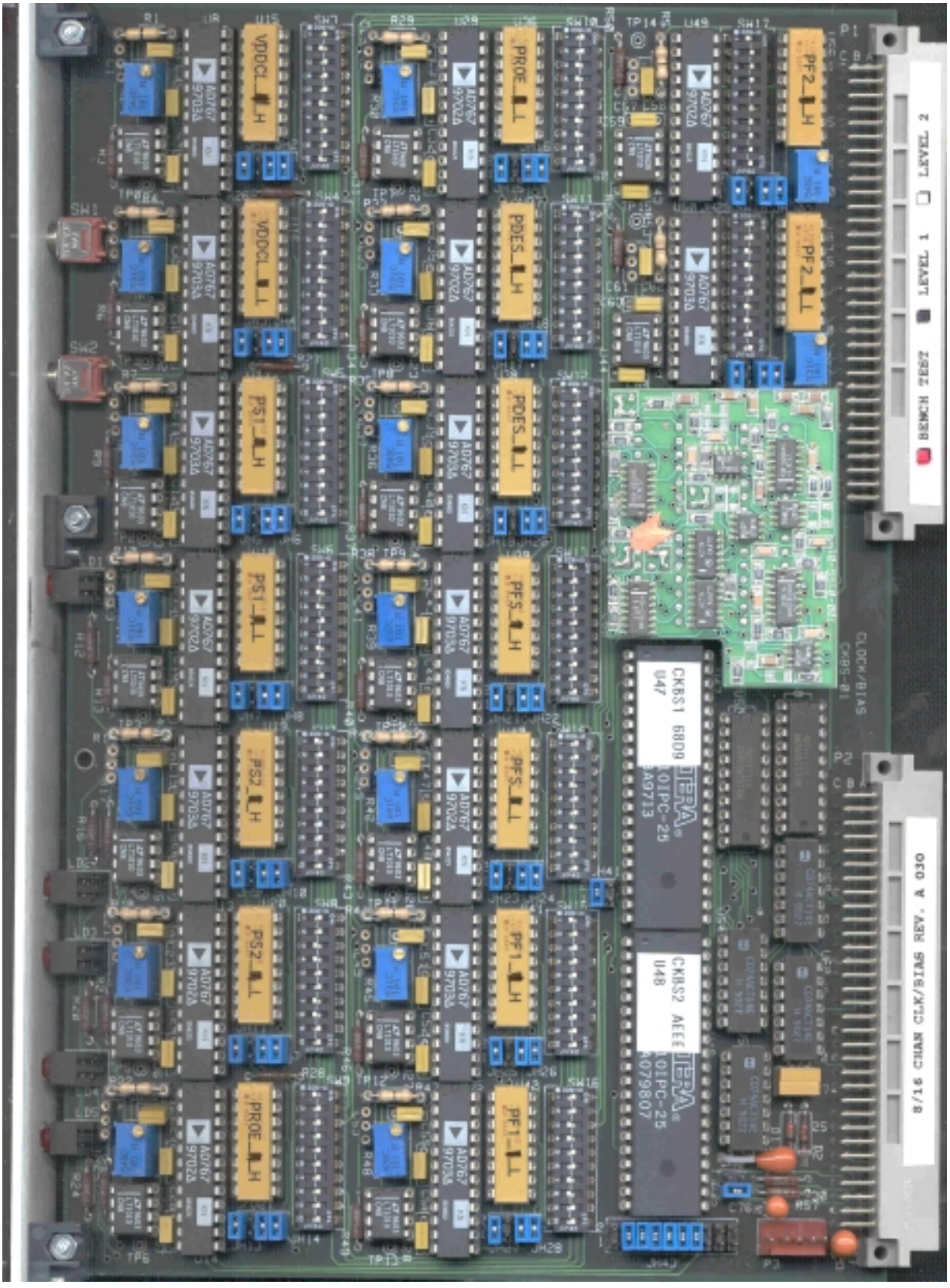
Mechanical Specifications

- Eurocard 6U (160mm x 233.35mm) Form Factor
- P1 96 pin DIN Connector,P2 DIN 41612, 96 Pin Connector
- 6 Layer PCB Construction with Internal Gnd & Power Layers

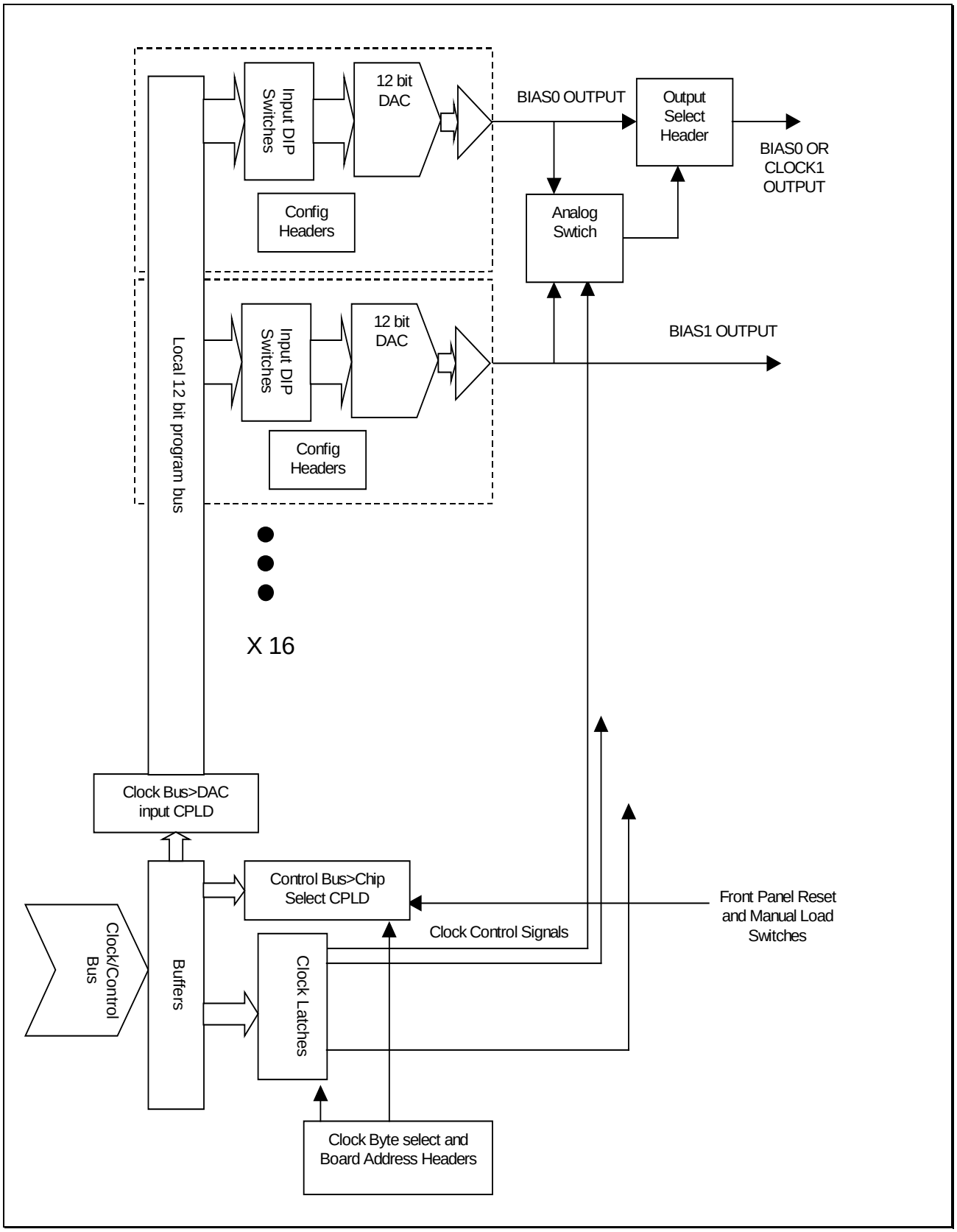
4.1.5.2 Component side photo VGGCL configuration:



4.1.5.2.1 Component side photo VDDCL configuration:



4.1.5.3 Block Diagram



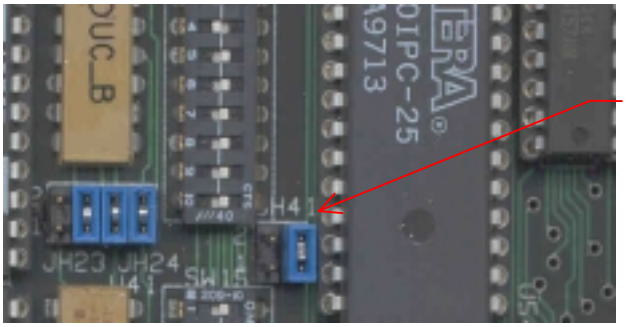
4.1.5.4 Functional Description 700-111-01 CLKBIAS

4.1.5.4.1 Inputs

The Clock Control Bus signals CB_D0 to CB_D15 are digital bus inputs to the board that are buffered and used to control the analog output switches. In addition, the Control signals CB_CW0 to CB_CW7 are used to select and program specific DAC circuits that have been shunt enabled to be programmed by the Clock DSP.

4.1.5.4.2 Input Byte Selection

Either the lower CB_D0 to CB_D7 or upper CB_D8 to CB_D15 bytes of the Clock Control Bus are selected via JH41 header. Shunting pins 1 to 2 select the High Byte, 3 to 4 the Low Byte.

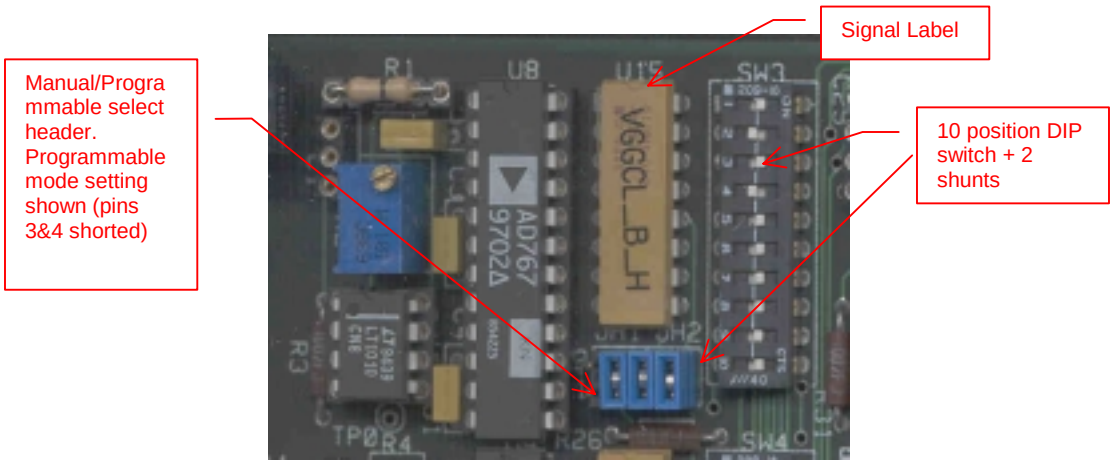


4.1.5.4.3 Control CPLDs

Two Altera EP910 CPLDs decode the Control Bus sequences for DAC programming and board control. U48 decodes the specific board, and DAC address from the Control Bus and generates a Chip Select signal CS0! To CS15!. U47 latches the 12 bit DAC program value from a specific Clock Bus cycle.

4.1.5.4.4 DAC/Bias circuit sections

There are 16 virtually identical DAC circuit sections layed out on the printed circuit.board. Each section has



input 10 position DIP switch plus 2 headers that connect to the 12bit input of the DAC. There is also a Manual/Programmable Selection Header. If the header is configured for Manual control (pins 1&2 shunted) then
the DAC will output the voltage solely set by the positions on the DIP switch +2 headers. The CPLDs are programmed to output a CS! signal (which loads the 12bits into the input on CS!'s rising edge) after a power up delay and if the front panel Manual Load switch is pressed.

If the header is set for Programmable operation then the DAC will output the voltage determined what the user enters in the Engineering window under the Set DAC window AND the DIP switch +2 headers. When set correctly, the DIP switch +2 headers bound the upper and lower voltage range available to be programmed. See the configuration section for the specific settings of each DAC section.
The DAC outputs are current buffered, optionally filtered used for array biases or are combined into analog clocks.

4.1.5.4.5 Analog Clock Switches

To create an analog clock signal, two DAC outputs are input into an high speed analog switch (Harris HI201HS). The switch is controlled by CKLCTL# (#=1-8) signals derived from the Clock Control Bus. For example if the LOW byte is selected, the CB_D0 will control the analog CLK0 switch. A downstream selection header either allows the BIAS or CLK signal to be output by the board.

4.1.5.5 Configuration and Test Connectors

4.1.5.5.1 Board Configurations for 1024x1024 InSb arrays (Raytheon 152 and 206 readouts)

Although the clocking is not implemented, the system is full configured to run the top 2 quadrants of the array separately from the bottom two. Consequently there are 4 CLKBIAS boards in the system. Two CLKBIAS boards are needed to run each ½ array. They can be differentiated by the first DAC signal generated by the board and where they run the top or bottom of the array. The VDDCL configured boards are located in slots 1 and 8 and the VGGCL configured boards are located in slots 7 and 14 a 1k x 1k InSb system.

4.1.5.5.1.1 VGGCL Configuration

In section 4.1.5.1 a photo of the "VGGCL" configuration is shown. Note that the label reads VGGCL_B_H which is the VGGCL signal for the bottom 2 quads of the array and the DAC circuit supplies the High level. The High level corresponds to the digital high state of the corresponding Clock/Control Bus signal. JH41 is set for the LOW byte so the analog clock signal VGGCL is controlled by CB_D0. A similarly configured board is used for the top 2 halves of the array. **Note that each of the DAC circuits has specific header and DIP switch settings, refer to the System portion of the documentation for more detail on array clocks and biases.**

4.1.5.5.1.2 VDDCL Configuration

In section 4.1.5.2 a photo of the "VDDCL" configuration is shown. Note that the label reads VDDCL_x_H which is the VDDCL signal for the spare (x) board of the array and the DAC circuit supplies the High level. The High level corresponds to the digital high state of the corresponding Clock/Control Bus signal. JH41 is set for the HIGH byte so the analog clock signal VDDCL is controlled by CB_D8. **Note that each of the DAC circuits has specific header and DIP switch settings, refer to the System portion of the documentation for more detail on array clocks and biases.**

4.1.5.5.1.3 Standard voltage settings

As of 10/21/99 the Bias and Clock voltage settings for the 1024 x 1024 InSb Raytheon 152 and 206 readouts are shown in the following table. Note that the voltages that are set to programmable ranges will be initialized by the CPLDs and DIP switches to the most negative value in the range, i.e. VDET,VDDUC and VGGCL will be initialized to –3.75 volts.

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BIAS VOLTAGES AS OF 3/20/98 USING some FOWLER VOLTAGES

DETECTOR BIAS	
VDDUC	***VDET***
-3.7	-3.375

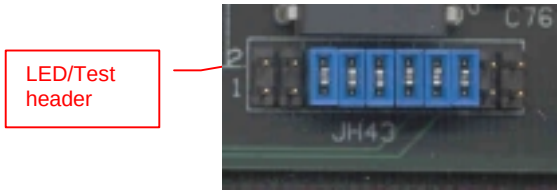
			1 LSB =	DIP SWITCH POSITION											
			VOLTS	1	2	3	4	5	6	7	8	9	10	JHX	JHXX
			9.995117188	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Board #	DAC#	signal ****= set for programmable voltage, voltage shown is max negative***													
			0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	0	VDDCL_B_H	-4.5	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON
0	1	VDDCL_B_L	-1.3	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF
0	2	PS1_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	3	PS1_B_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
0	4	PS2_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	5	PS2_B_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
0	6	PROE_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	7	PROE_B_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
0	8	PDES_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	9	PDES_B_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
0	10	PFS_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	11	PFS_B_L	-4	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON
0	12	PF1_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	13	PF1_B_L	-4	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON
0	14	PF2_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	15	PF2_B_L	-4	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON
1	0	***VGGCL_B_H****	***-3.75***	ON	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON
1	1	VGGCL_B_L	-4.5	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON
1	2	VROWON_B_H	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	3	VROWON_B_L	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
1	4	VRSTR_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
1	5	VRSTR_B_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	6	VRSTG_B_H	-2	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON
1	7	VRSTG_B_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	8	VIREF_B	-1.8	ON	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
1	9	VDDOUT_B	-1.3	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF
1	10	***VDETCOM_B****	***-3.75***	ON	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON
1	11	***VDDUC_B****	***-3.75***	ON	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON
1	12	VNCOL_B	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	13	VNROW_B	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	14	PSS_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
1	15	PSS_B_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
0	0	VDDCL_T_H	-4.5	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON
0	1	VDDCL_T_L	-1.3	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF
0	2	PS1_T_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	3	PS1_T_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
0	4	PS2_B_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	5	PS2_T_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
0	6	PROE_T_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	7	PROE_T_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
0	8	PDES_T_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	9	PDES_T_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
0	10	PFS_T_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	11	PFS_T_L	-4	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON
0	12	PF1_T_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	13	PF1_T_L	-4	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON
0	14	PF2_T_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0	15	PF2_T_L	-4	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON
1	0	***VGGCL_T_H****	***-3.75***	ON	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON
1	1	VGGCL_T_L	-4.5	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON
1	2	VROWON_T_H	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	3	VROWON_T_L	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
1	4	VRSTR_T_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
1	5	VRSTR_T_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	6	VRSTG_T_H	-2	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON
1	7	VRSTG_T_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	8	VIREF_T	-1.8	ON	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
1	9	VDDOUT_T	-1.3	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF
1	10	***VDETCOM_T****	***-3.75***	ON	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON
1	11	***VDDUC_T****	***-3.75***	ON	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON
1	12	VNCOL_T	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	13	VNROW_T	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
1	14	PSS_T_H	0	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
1	15	PSS_T_L	-6	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF

4.1.5.5.1.4 JH43 LED/Test Header

JH1 is a 20 pin header that serves the dual purpose of connecting the test signals to the front panel LEDS. The five shunts connect the following signals from the CPLD U48 to the front panel LEDS:

Signal = front panel label

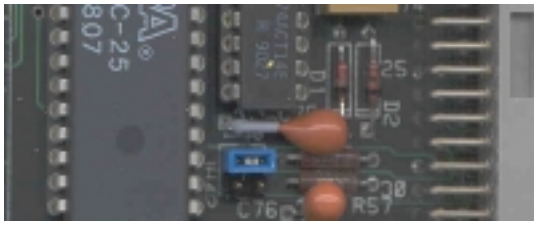
STAT0 = !RST	board reset indicator
STAT1 = ADDR0	board address0
STAT2 = ADDR1	board address1
STAT3 = HI/LO	high/low byte select
STAT4 = THISBD	board being addressed via control sequence



When used as a test header, the signals are configured to mate with an HP 1600 series Logic Analyzer 16 channel pod.

4.1.5.5.1.5 JH42 CPLD Board Address Header

JH42 sets the board address for each half of the array electronics. The VGGCL boards are set with pins 3 and 4 shunted which sets ADDR0=1, ADDR1=0 board address=1.



The VDDCL boards are set with pins 1 and 2 shunted which sets ADDR0=0, ADDR1=1 board address=2.

4.1.5.5.1.6 Manual Load and Reset Front Panel Switches

Both the front panel switches are not needed for normal system operation. They are useful for checkout and troubleshooting. When either switch is depressed, the DACs will be programmed with whatever is set

on the DIP switches and will override any previous programmed voltage. Manual load is a bit more useful for bench top testing.

4.1.6 700-155-01 Clkbias Daughter driver board

4.1.6 Overview

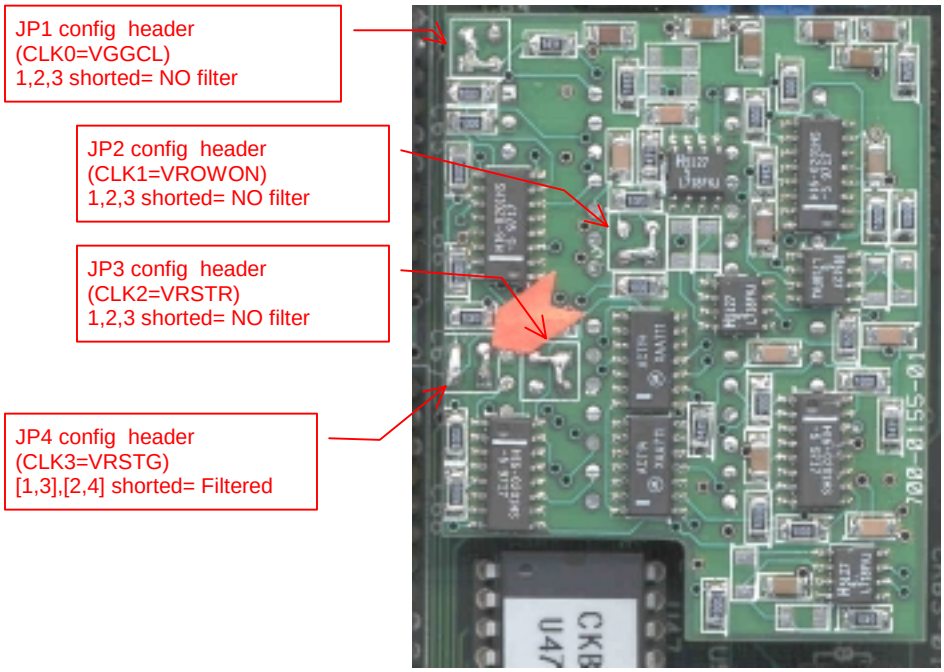
Each VGGCL and VDDCL configured CLKBIAS board has an associated 700-154-01 daughter board that provides high speed analog clocking on each of the 8 output clocks. In addition, the first 4 clocks can be jumper solder configured for output through a 2 pole Bessel filter for delayed rise and fall times.

4.1.6.1 Technical Specifications

- Harris HS201HS analog switches, clocks channels 1-8
- Harris 5127 opamp based Bessel filter on clocks channels1-4
- Surface mount daughter board for 700-0111-1 CLKBIAS boards

4.1.6.2 Component side photographs of configured daughter boards

VGGCL configuration



VDDCL configuration

Rev 1.1

JP1 config header
(CLK0=VDDCL)
1,2,3 shorted= NO filter

JP2 config header
(CLK1=PS1)
1,2,3 shorted= NO filter

JP3 config header
(CLK2=PS2)
1,2,3 shorted= NO filter

JP4 config header
(CLK3=PROE)
1,2,3 shorted= NO filter