HARDWARE REFERENCE MANUAL

PMAC PCI Lite

PCI Format 4-Axis Control Board

400-603657-xHxx

May 19, 2003

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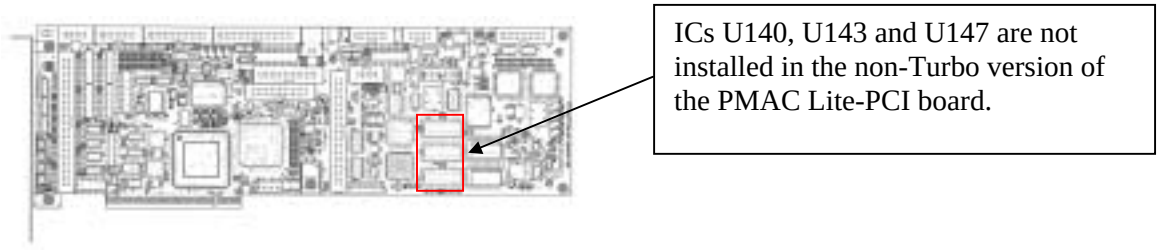
INTRODUCTION

Overview

The PMAC PCI-Lite is a member of the PMAC family of boards optimized for interface to traditional servo drives with single analog inputs representing velocity or torque commands. Its software is capable of eight axes of control, although it can have only four channels of on-board axis interface circuitry.

The PMAC PCI-Lite is a full-sized PCI-bus expansion card. While capable of PCI bus communications, with or without the optional dual-ported RAM, it does not need to be inserted into a PCI expansion slot. Communications can be done through an RS-232 or RS-422 serial port. Standalone operation is possible.

The non-Turbo version of the PMAC PCI-Lite board does not include ICs U140, U143 or U147.



Board Configuration

Base Version

The base version of the PMAC PCI-Lite provides a 1-1/2-slot board with:

- 40 MHz DSP563xx CPU
- 128k x 24 zero-wait-state flash-backed SRAM
- 512k x 8 flash memory for firmware and user backup
- Latest released firmware version
- RS-232/422 serial interface, PCI bus interface
- Four channels axis interface circuitry, each including:
  - 16-bit +/-10V analog output
  - 3-channel differential/single-ended encoder input
  - Four input flags, two output flags
  - Interface to external 16-bit serial ADC
- Display, control panel, mixed I/O, direct I/O interface ports
- Buffered expansion port
- Clock crystal with +/-100 ppm accuracy
- PID/notch/feedforward servo algorithms
- 1-year warranty from date of shipment
- One manuals CD per set of one to four PMACs in shipment (cables, mounting plates, mating connectors not included)

Option 2: Dual Ported RAM

Dual-ported RAM provides a very high-speed communications path for bus communications with the host computer through a bank of shared memory. DPRAM is advised if more than about 100 data items per second are to be passed between the controller and the host computer in either direction.

- Option 2 provides an 8k x 16 bank of on-board dual-ported RAM. The key component on the board is U1.

Option 2B: High-Speed USB Communications Interface

Option 2B provides the high-speed USB communications interface, which is a faster method of communication than the standard RS-232 communications port.

Option 5xF: CPU Speed Options

The base PMAC PCI-Lite version has a 40 MHz DSP563xx CPU. This is Option 5AF, which is automatically provided if no CPU speed option is specified.

- Option 5AF: 40 MHz DSP563xx CPU (80 MHz 56002 equivalent). This is the default CPU speed.
- Option 5CF: 80 MHz DSP563xx CPU (160 MHz 56002 equivalent).
- Option 5EF: 160 MHz DSP563xx CPU (320 MHz 56002 equivalent).

Option 6: Extended Servo Algorithm Firmware

- Option 6 provides an Extended (Pole-Placement) Servo Algorithm firmware instead of the regular servo algorithm firmware. This is required only in difficult-to-control systems (resonances, backlash, friction, disturbances, changing dynamics).

Option 6L: Special Lookahead Firmware

- Option 6L provides a special lookahead firmware for sophisticated acceleration and cornering profile execution. With the lookahead firmware, PMAC automatically controls the speed along the path (but without changing the path) to ensure that axis limits are not violated.

Option 7: Plate Mounting

- Option 7 provides a mounting plate connected to the PMAC with standoffs. It is used to install the PMAC in standalone applications.

Option 8A: High-Accuracy Clock Crystal

The PMAC PCI-Lite has a clock crystal of nominal frequency 19.6608 MHz (~20 MHz). The standard crystal's accuracy specification is +/-100 ppm.

- Option 8A provides a nominal 19.6608 MHz crystal with a +/-15 ppm accuracy specification.

Option 10: Firmware Version Specification

Normally the PMAC PCI-Lite is provided with the newest released firmware version. A label on the memory IC shows the firmware version loaded at the factory.

- Option 10 provides for a user-specified firmware version.

Option 12: Analog-to-Digital Converters

Option 12 permits the installation of 8 or 16 channels of on-board multiplexed analog-to-digital converters. One or two of these converters are read every phase interrupt. The analog inputs are not optically isolated, and each can have a 0 – 5V input range, or a +/-2.5V input range, individually selectable.

- Option 12 provides an 8-channel 12-bit A/D converter. The key components on the board are U20 and connector J30.
- Option 12A provides an additional 8-channel 12-bit A/D converter. The key component on the board is U22.

Option 15: V-to-F Converter for Analog Input

The JPAN control panel port on the PMAC PCI-Lite has an optional analog input called Wiper (because it is often tied to a potentiometer's wiper pin). PMAC PCI-Lite can digitize this signal by passing it through an optional voltage-to-frequency converter, using E-point jumpers to feed this into the Encoder 4 circuitry (no other use is permitted then), and executing frequency calculations using the "time base" feature of the encoder conversion table. The key component on the board is U18.

- Option 15 provides a voltage-to-frequency converter that permits the use of the WIPER input on the control panel port.

Option 16: Battery-Backed Parameter Memory

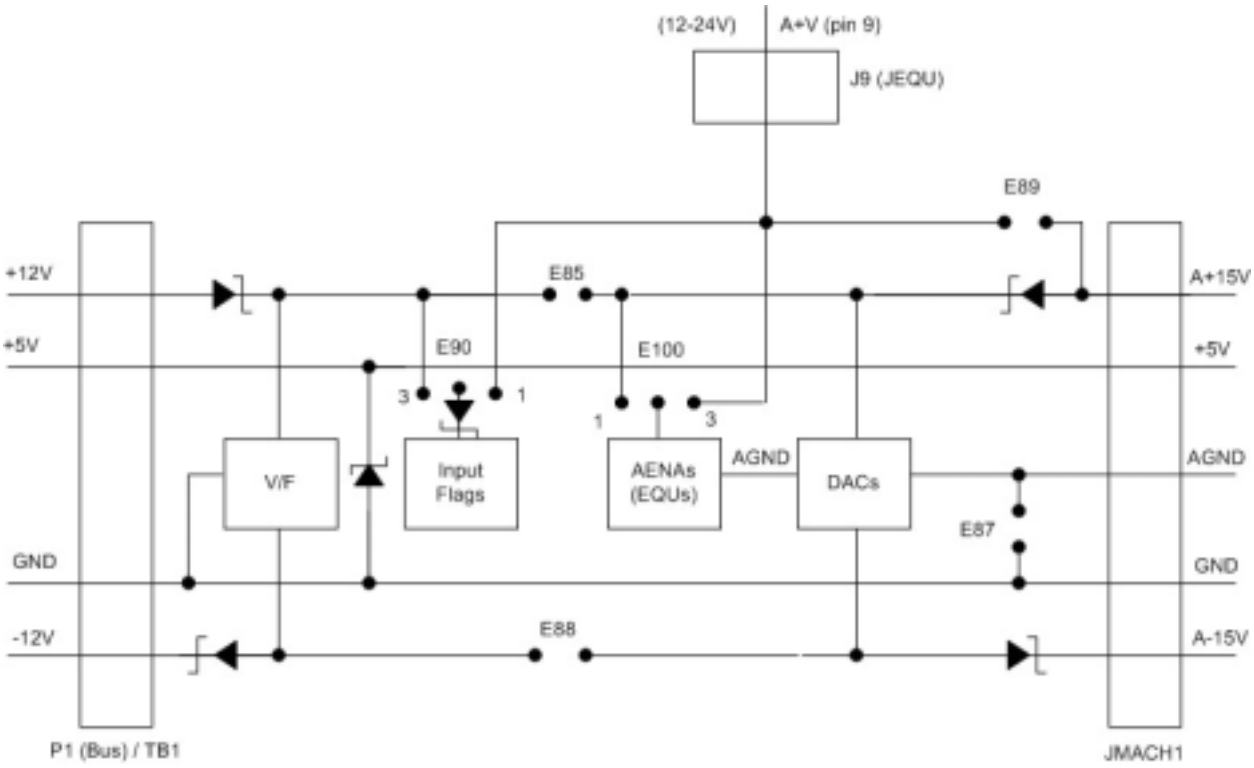
The contents of the standard memory are not retained through a power-down or reset unless they have been saved to flash memory first. Option 16 provides supplemental battery-backed RAM for real-time parameter storage that is ideal for holding machine state parameters in case of an unexpected power-down. This memory appears at addresses $A000 - $BBFF. The key components on the board are U142, U145, U149, and BT1.

- Option 16A provides a 16k x 24 bank of battery-backed parameter RAM.

HARDWARE SETUP

On the PMAC, there are many jumpers (pairs of metal prongs), called E-points. Some have been shorted together; others have been left open. These jumpers customize the hardware features of the board for a given application and must be set up appropriately. The following is an overview of the several PMAC jumpers grouped in appropriate categories. For a complete description of the jumper setup configuration, refer to the "PMAC PCI-Lite CPU Board E-Point Descriptions" chapter.

Power-Supply Configuration Jumpers



E85, E87, E88: Analog Circuit Isolation Control – These jumpers control whether the analog circuitry on the PMAC is isolated from the digital circuitry, or electrically tied to it. In the default configuration, these jumpers are off, keeping the circuits isolated from each other (provided separate isolated supplies are used).

E89-E90: Input Flag Supply Control – If E90 connects pins 1 and 2 and E89 is ON, the input flags (+LIMn, -LIMn, HMFLn) are supplied from the analog A+15V supply, which can be isolated from the digital circuitry. If E90 connects pins 1 and 2 and E89 is OFF, the input flags are supplied from a separate A+V supply through pin 9 of the J8 JEQU connector. This supply can be in the +12V to +24V range, and can be kept isolated from the digital circuitry. If E90 connects pins 2 and 3, the input flags are supplied from the digital +12V supply, and isolation from the digital circuitry is defeated.

E100: AENA/EQU Supply Control – If E100 connects pins 1 and 2, the circuits related to the AENAn, EQUn and FAULTn signals will be supplied from the analog A+15V supply, which can be isolated from the digital circuitry. If E100 connects pins 2 and 3, the circuits will be supplied from a separate A+V supply through pin 9 of the J9 JEQU connector. This supply can be in the +12V to +24V range, and can be kept isolated from the digital circuitry.

Clock Configuration Jumpers

E3-E6: Servo Clock Frequency Control –Jumpers E3 – E6 determine the servo-clock frequency by controlling how many times it is divided down from the phase-frequency. The default setting of E3 and E4 OFF, E5 and E6 ON divides the phase-clock frequency by four, creating a 2.25kHz servo-clock frequency. This setting is seldom changed.

E29-E33: Phase Clock Frequency Control – Only one of the jumpers E29 – E33, which select the phase-clock frequency, may be on in any configuration. The default setting of E31 ON, which selects a 9kHz phase-clock frequency, is seldom changed.

E34-E38: Encoder Sample Clock – Only one of the jumpers E34 – E38, which select the encoder sample clock frequency, may be on in any configuration. The frequency must be high enough to accept the maximum true count rate (no more than one count in any clock period), but a lower frequency can filter out longer noise spikes. The anti-noise digital delay filter can eliminate noise spikes up to one sample-clock cycle wide.

E40-43: Servo and Phase Clock Direction Control – Jumpers E40 – E43 determine the direction of the phase and servo clocks: all of these jumpers must be ON for the card to use its internally generated clock signals and to output these on the serial port connector. If any of these jumpers is OFF, the card will expect to input these clock signals from the serial port connector, and its watchdog timer will trip immediately if it does not receive these signals. The card number (0 – 15) for serial addressing of multiple cards on a daisychain serial cable is determined by the PMAC variable I0. See the Software Setup section in this manual for details.

E48: Option CPU Clock Frequency Control – If variable I46 is saved at a value greater than 0, I46 will determine the CPU's operational frequency (recommended). For backward compatibility, if I46 is saved at a value of 0, the CPU will operate at 40MHz if E48 is OFF, or at 60MHz if E48 is ON.

E98: DAC/ADC Clock Frequency Control – Leave E98 in its default setting of 1-2, which creates a 2.45MHz DCLK signal, unless connecting an ACC-28 A/D-converter board. In this case, move the jumper to connect pins 2 and 3, which creates a 1.22MHz DCLK signal.

Encoder Configuration Jumpers

Encoder Complementary Line Control – The selection of the type of encoder used, either single-ended or differential is made through the resistor packs configuration and not through a jumper configuration, as on older PMAC designs.

E22-E23: Control-Panel Handwheel Enable – Putting these jumpers ON ties the handwheel-encoder inputs on the JPAN control-panel port to the Channel 2 encoder circuitry. If the handwheel inputs are connected to Channel 2, no encoder should be connected to Channel 2 through the JMACH connector.

E72-E73: Control Panel Analog Input Enable – Putting these jumpers ON ties the output of the Option 10 voltage-to-frequency converter that can process the Wiper analog input on the JPAN control panel port to the Channel 4 encoder circuitry. If the frequency signal is connected to Channel 4, no encoder should be connected to Channel 4 through the JMACH connector.

E74-E75: Encoder Sample Clock Output – Putting these jumpers ON ties the encoder sample-clock signal to the CHC4 and CHC4/ lines on the JMACH port. This permits the clock signal to be used to synchronize external encoder-processing devices like the ACC-8D Option 8, interpolator board. With these jumpers ON, no encoder input signal should be connected to these pins.

Board Reset/Save Jumpers

E50: Flash-Save Enable/Disable Control – If E50 is ON (default), the active software configuration of the PMAC can be stored to non-volatile flash memory with the **SAVE** command. If the jumper on E50 is removed, this **SAVE** function is disabled, and the contents of the flash memory cannot be changed.

E51: Re-Initialization on Reset Control – If E51 is OFF (default), PMAC executes a normal reset, loading active memory from the last saved configuration in non-volatile flash memory. If E51 is ON, PMAC re-initializes on reset, loading active memory with the factory default values.

Communication Jumpers

PCI Bus Base Address Control – The selection of the base address of the card in the I/O space of the host PC's expansion bus is assigned automatically by the operating system and is not selected through a jumper configuration as ISA bus address would be.

E44-E47: Serial Baud Rate Selection – If the saved value of I46 is 0, the CPU's operational frequency is determined by the E48 jumper settings. Then the serial baud rate is determined by a combination of the setting of jumpers E44-E47 and the CPU frequency on a PMAC(1) board. If the CPU's operational frequency has been determined by a non-zero setting of I46, the serial communications baud rate is determined only by variable I54 at power-up/reset. See the Software Setup section of this manual for details.

E49: Serial Communications Parity Control – Jump pin 1 to 2 for NO serial parity; remove jumper for ODD serial parity.

E54-E65: Interrupt Source Control – These jumpers control which signals are tied to interrupt lines IR5, IR6 and IR7 on PMAC's programmable interrupt controller (PIC) as shown in the interrupt diagram. Only one signal may be tied into each of these lines.

E110: Serial Port Configure – Jump pin 1 to 2 for use of the J4 connector as RS-232. Jump pin 2 to 3 for use of the J4 connector as RS-422.

E111: Clock Lines Output Enable – Jump pin 1 to 2 to enable the Phase, Servo and Init lines on the J4 connector. Jump pin 2 to 3 to disable the Phase, Servo and Init lines on the J4 connector. For daisychained PMACs sharing the clock lines for synchronization, E111 must be on positions 1 to 2.

I/O Configuration Jumpers

E1-E2: Machine Output Supply Configure – With the default sinking output driver IC (ULN2803A or equivalent) in U13 for the J5 JOPTO port outputs, these jumpers must connect pins 1 and 2 to supply the IC correctly. If this IC is replaced with a sourcing output driver IC (UDN2981A or equivalent), these jumpers must be changed to connect pins 2 and 3 to supply the new IC correctly.

Caution

A wrong setting of these jumpers will damage the associated output IC.

E7: Machine Input Source/Sink Control – With this jumper connecting pins 1 and 2 (default) the machine input lines on the J5 JOPTO port are pulled up to +5V or the externally provided supply voltage for the port. This configuration is suitable for sinking drivers. If the jumper is changed to connect pins 2 and 3, these lines are pulled down to GND – this configuration is suitable for sourcing drivers.

E17A - E17D: Motors 1-4 Amplifier-Enable Polarity Control – Jumpers E17A through E17D control the polarity of the amplifier enable signal for the corresponding motor 1 to 4. When the jumper is ON (default), the amplifier-enable line for the corresponding motor is low true so the enable state is low-voltage output and sinking current, and the disable state is not conducting current. If the default ULN2803A sinking driver used by the PMAC is on U37, this is the fail-safe option. This allows the

circuit to fail in the disable state. With this jumper OFF, the amplifier-enable line is high true so the enable state is not conducting current, and the disable state is low-voltage output and sinking current. (This setting is not generally recommended.)

E28: Following-Error/Watchdog-Timer Signal Control – With this jumper connecting pins 2 and 3 (default), the FEFCO/ output on pin 57 of the J8 JMACH servo connector outputs the watchdog timer signal. With this jumper connecting pins 1 and 2, this pin outputs the warning following error status line for the selected coordinate system.

E101-E102: Motors 1-4 AENA/EQU voltage configure – The U37 driver IC controls the AENA and EQU signals of motors 1-4. With the default sinking output driver IC (ULN2803A or equivalent) in U37, these jumpers must connect pins 1 and 2 to supply the IC correctly. If this IC is replaced with a sourcing output driver IC (UDN2981A or equivalent), these jumpers must be changed to connect pins 2 and 3 to supply the new IC correctly.

Caution

A wrong setting of these jumpers will damage the associated output IC.

E122: XIN7 feature selection – Jump 2-3 to bring the Power Good signal into register XIN7 at Y:$E801 bit 7.

Reserved Configuration Jumpers

E0: Reserved for future use.

E109: Reserved for future use.

CPU Jumper Configuration

E10A-E10C: Flash Memory Bank Select Jumpers – The flash-memory IC in location U146 on the PMAC PCI-Lite board has the capacity for eight separate banks of firmware, only one of which can be used at any given time. The eight combinations of settings for jumpers E10A, E10B, and E10C select which bank of the flash memory is used. In the factory production process, firmware is loaded only into Bank 0, which is selected by having all of these jumpers OFF.

E18-E20: Power-Up State Jumpers – Jumper E18 must be OFF, jumpers E19 and E20 must be ON, in order for the CPU to copy the firmware from flash memory into active RAM on power-up/reset. This is necessary for normal operation of the card. (Other settings are for factory use only.)

E21: Firmware Load Jumper – If jumper E21 is ON during power-up/reset, the board comes up in bootstrap mode, which permits the loading of new firmware into the flash-memory IC on the board. When the PMAC Executive program tries to establish communications with a board in this mode, it will automatically detect that the board is in bootstrap mode and ask what file to download as the new firmware. Jumper E21 must be OFF during power-up/reset for the board to come up in normal operational mode.

E119: Watchdog Timer Jumper - Jumper E119 must be OFF for the watchdog timer to operate. This is a very important safety feature, so it is vital that this jumper be OFF in normal operation. E1 should only be put ON to debug problems with the watchdog timer circuit.

Resistor Pack Configuration: Termination Resistors

The PMAC provides sockets for termination resistors on differential input pairs coming into the board. There are no resistor packs in these sockets when shipped. If these signals are brought long distances into the PMAC board and ringing at signal transitions is a problem, SIP resistor packs may be mounted in these sockets to reduce or eliminate the ringing.

All termination resistor packs have independent resistors (no common connection) with each resistor using two adjacent pins. The following table shows which packs are used to terminate each input device:

Device	Resistor Pack	Pack Size
Encoder 1	RP61	6-pin
Encoder 2	RP63	6-pin
Encoder 3	RP67	6-pin
Encoder 4	RP69	6-pin

Resistor Pack Configuration: Differential or Single-Ended Encoder Selection

The differential input signal pairs to the PMAC have user-configurable pull-up/pull-down resistor networks to permit the acceptance of either single-ended or differential signals in one setting, or the detection of lost differential signals in another setting.

- The '+' inputs of each differential pair each have a hard-wired 1 kΩ pull-up resistor to +5V. This cannot be changed.
- The '-' inputs of each differential pair each have a hard-wired 2.2 kΩ resistor to +5V; also each has another 2.2 kΩ resistor as part of a socketed resistor pack that can be configured as a pull-up resistor to +5V, or a pull-down resistor to GND.

If this socketed resistor is configured as a pull-down resistor (the default configuration), the combination of pull-up and pull-down resistors on this line acts as a voltage divider, holding the line at +2.5V in the absence of an external signal. This configuration is required for single-ended inputs using the '+' lines alone; it is desirable for unconnected inputs to prevent the pick-up of spurious noise; it is permissible for differential line-driver inputs.

If this socketed resistor is configured as a pull-up resistor (by reversing the SIP pack in the socket), the two parallel 2.2 kΩ resistors act as a single 1.1 kΩ pull-up resistor, holding the line at +5V in the absence of an external signal. This configuration is required if encoder-loss detection is desired; it is required if complementary open-collector drivers are used; it is permissible for differential line-driver inputs even without encoder loss detection.

If Pin 1 of the resistor pack (marked by a dot on the pack) matches Pin 1 of the socket (marked by a wide white line on the front side of the board) and a square solder pin on the back side of the board, then the pack is configured as a bank of pull-down resistors. If the pack is reversed in the socket, it is configured as a bank of pull-up resistors.

The following table lists the pull-up/pull-down resistor pack for each input device:

Device	Resistor Pack	Pack Size
Encoder 1	RP60	6-pin
Encoder 2	RP62	6-pin
Encoder 3	RP66	6-pin
Encoder 4	RP68	6-pin

MACHINE CONNECTIONS

Typically, the user connections are made to a terminal block that is attached to the JMACH connector by a flat cable (Accessory 8D or 8P). The pinout numbers on the terminal block are the same as those on the JMACH connector. The possible choices for breakout boards are:

Board	Mounting	Breakout Style	Breakout Connector	Notes
ACC-8P	DIN – Rail	Monolithic	Terminal Block	Simple Phoenix contact board
ACC-8D	DIN – Rail	Monolithic	Terminal Block	Headers for connection to option boards
ACC-8DCE	DIN – Rail	Modular	D-sub connector	Fully shielded for easy CE mark compliance

Mounting

The PMAC can be mounted in one of two ways: in the PCI bus, or using standoffs.

- PCI bus: To mount in the PCI bus, simply insert the P1 card-edge connector into the PCI socket. If there is a standard PC-style housing, a bracket at the end of the PMAC board can be used to screw into the housing to hold the board down firmly.
- Standoffs: At each of the four corners of the PMAC board, there are mounting holes that can be used to mount the board on standoffs.

Power Supplies

Digital Power Supply

2A @ +5V (+/-5%) (10W)
(Eight-channel configuration with a typical load of encoders)

- The host computer provides the 5V power supply if PMAC is installed in its internal bus.

  With the board plugged into the bus, it will pull +5V power from the bus automatically and it cannot be disconnected. In this case, there must be no external +5V supply, or the two supplies will fight each other, possibly causing damage. This voltage could be measured between pins 1 and 3 of the terminal block.
- In a stand-alone configuration, when PMAC is not plugged in a computer bus, it will need an external 5V supply to power its digital circuits. The +5V line from the supply should be connected to pin 1 or 2 of the JMACH connector (usually through the terminal block), and the digital ground to pin 3 or 4. ACC-1x provides different options for the 5V power supply.

Analog Power Supply

0.3A @ +12 to +15V (4.5W)
0.25A @ -12 to -15V (3.8W)

The analog output circuitry on PMAC is optically isolated from the digital computation circuitry, and so requires a separate power supply. Bring this in on the JMACH connector. Bring the positive supply (+12 to +15V) in on the A+15V line on pin 59. Bring the negative supply (-12 to -15V) in on the A-15V line on pin 60 and the analog common in on the AGND line on pin 58.

Typically this supply can come from the servo amplifier; many commercial amplifiers provide such a supply, or an external supply may be used. ACC-2x provides different options for the ± 15V power supply. Even with an external supply, the AGND line should be tied to the amplifier common. It is possible to get the power for the analog circuits from the bus, but doing so defeats optical isolation. In this case, no new connections need to be made. However, be sure jumpers E85, E87, E88, E89, and E90 are set up for this circumstance. (The card is not shipped from the factory in this configuration.)

Overtravel Limits and Home Switches

When assigned for the dedicated uses, these signals provide important safety and accuracy functions. +LIMn and -LIMn are direction-sensitive overtravel limits, that must be actively held low (sourcing current from the pins to ground) to permit motion in their direction. The direction sense of +LIMn and -LIMn is as follows: +LIMn should be placed at the negative end of travel, and -LIMn should be placed at the positive end of travel.

Resistor Pack Configuration: Flag and Digital Inputs Voltage Selection

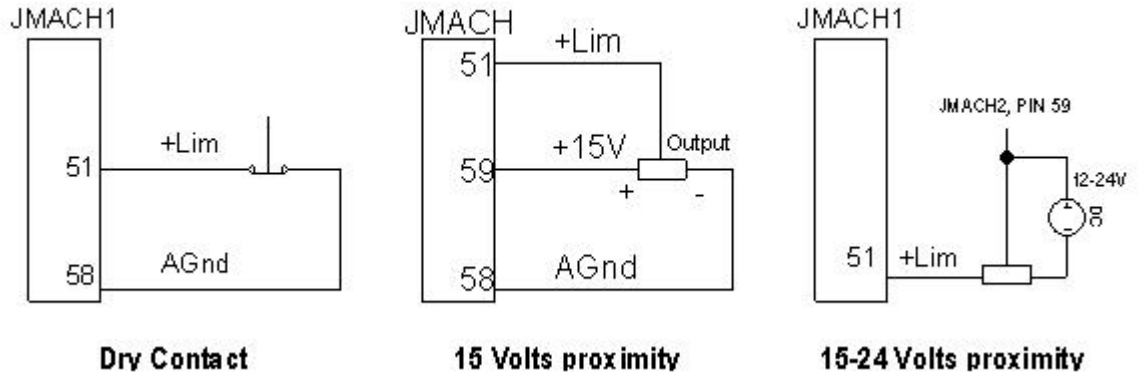
The PMAC is provided with 6-pin sockets for SIP resistor packs for the input flag sets. Each PMAC is shipped without resistor packs installed. If the flag or digital inputs circuits are in the 12V to 15V range, no resistor pack should be installed in these sockets. For flags or digital inputs at 5V levels, quad 1kΩ SIP resistor packs (1KSIP6C) should be installed in these sockets. The following table lists the voltage selection resistor pack sockets for each input device:

Device	Resistor Pack
Flags 1	RP77
Flags 2	RP83
Flags 3	RP89
Flags 4	RP94

Types of Overtravel Limits

PMAC expects a closed-to-ground connection for the limits to be considered not on fault. This arrangement provides a failsafe condition and therefore it cannot be reconfigured differently in PMAC.

Usually a passive normally closed switch is used. If a proximity switch is needed instead, use a 15V normally closed to ground NPN sinking type sensor.



Jumper E89, E90 and E100 must be set appropriately for the type of sensor used.

Home Switches

While normally closed-to-ground switches are required for the overtravel limits inputs, the home switches could be either normally closed or normally open types. The polarity is determined by the home sequence setup, through the I-variables I902, I907, ... I977. However, for the following reasons, the same type of switches used for overtravel limits are recommended:

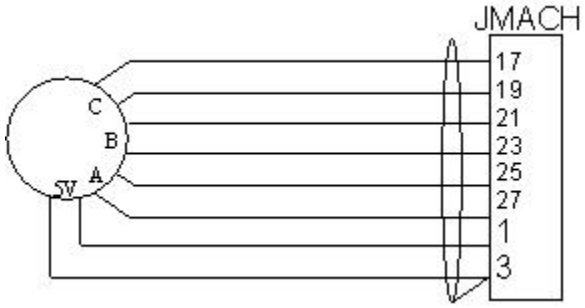
- Normally closed switches are proven to have greater electrical noise rejection than normally open types.
- Using the same type of switches for every input flag simplifies maintenance stock and replacements.

Motor Signals Connections (JMACH Connectors)

Incremental Encoder Connection

Each JMACH connector provides two +5V outputs and two logic grounds for powering encoders and other devices. The +5V outputs are on pins 1 and 2; the grounds are on pins 3 and 4. The encoder signal pins are grouped by number: all those numbered 1 (CHA1, CHA1/, CHB1, CHC1, etc.) belong to encoder #1. Usually, the encoder number matches the motor number, but it is not necessary. If the PMAC is not plugged into a bus and drawing its +5V and GND from the bus, use these pins to bring in +5V and GND from the power supply. Connect the A and B (quadrature) encoder channels to the appropriate terminal block pins. For encoder 1, the CHA1 is pin 25, CHB1 is pin 21. If there is a single-ended signal, leave the complementary signal pins floating — do not ground them. However, if single-ended encoders are used, check the settings of the jumpers E18 to E21 and E24 to E27. For a differential encoder, connect the complementary signal lines -- CHA1/ is pin 27, and CHB1/ is pin 23. The third channel (index pulse) is optional; for encoder 1, CHC1 is pin 17, and CHC1/ is pin 19.

Example: differential quadrature encoder connected to channel #1:



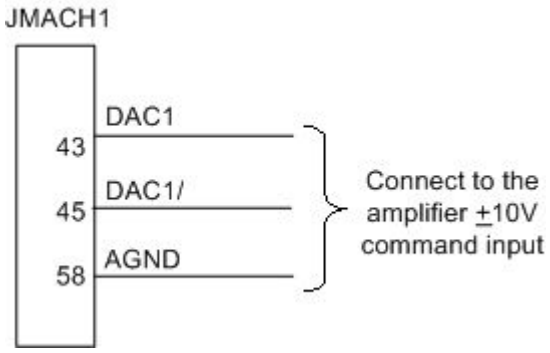
DAC Output Signals

If PMAC is not performing the commutation for the motor, only one analog output channel is required to command the motor. This output channel can be either single-ended or differential, depending on what the amplifier is expecting. For a single-ended command using PMAC channel 1, connect DAC1 (pin 43) to the command input on the amplifier. Connect the amplifier's command signal return line to PMAC's AGND line (pin 58). In this setup, leave the DAC1/ pin floating. Do not ground it.

For a differential command using PMAC channel 1, connect DAC1 (pin 43) to the plus-command input on the amplifier. Connect DAC1/ (pin 45) to the minus-command input on the amplifier. PMAC's AGND should still be connected to the amplifier common. If the amplifier is expecting separate sign and magnitude signals, connect DAC1 (pin 43) to the magnitude input. Connect AENA1/DIR1 (pin 47) to the sign (direction input). Amplifier signal returns should be connected to AGND (pin 58). This format requires some parameter changes on PMAC. (See Ix02 and Ix25.) Jumper E17 controls the polarity of the direction output. This may have to be changed during the polarity test. This magnitude-and-direction mode is suited for driving servo amplifiers that expect this type of input, and for driving voltage-to-frequency (V/F) converters, such as PMAC's ACC-8D Option 2 board, for running stepper motor drivers.

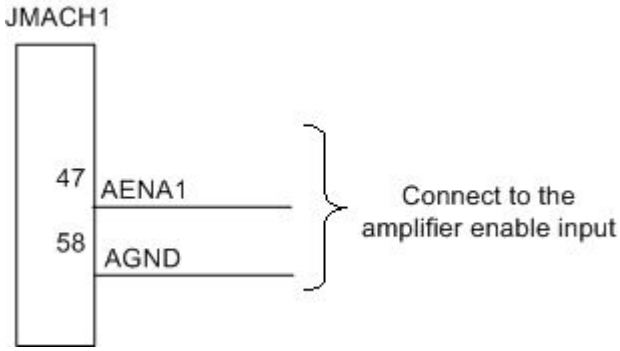
If using PMAC to commutate the motor, use two analog output channels for the motor. Each output may be single-ended or differential, just as for the DC motor. The two channels must be consecutively numbered, with the lower-numbered channel having an odd number (e.g., use DAC1 and DAC2 for a motor, or DAC3 and DAC4, but not DAC2 and DAC3, or DAC2 and DAC4). For our motor #1 example, connect DAC1 (pin 43) and DAC2 (pin 45) to the analog inputs of the amplifier. If using the complements as well, connect DAC1/ (pin 45) and DAC2/ (pin 46) the minus-command inputs; otherwise leave the complementary signal outputs floating. To limit the range of each signal to +/- 5V, use parameter Ix69. Any analog output not used for dedicated servo purposes may be utilized as a general-purpose analog output. Usually this is done by defining an M-variable to the digital-to-analog-converter register (suggested M-variable definitions M102, M202, etc.), then writing values to the M-variable. The analog outputs are intended to drive high-impedance inputs with no significant current draw. The 220Ω output resistors will keep the current draw lower than 50 mA in all cases and prevent damage to the output circuitry, but any current draw above 10 mA can result in noticeable signal distortion.

Example:



Amplifier Enable Signal (AENAx/DIRn)

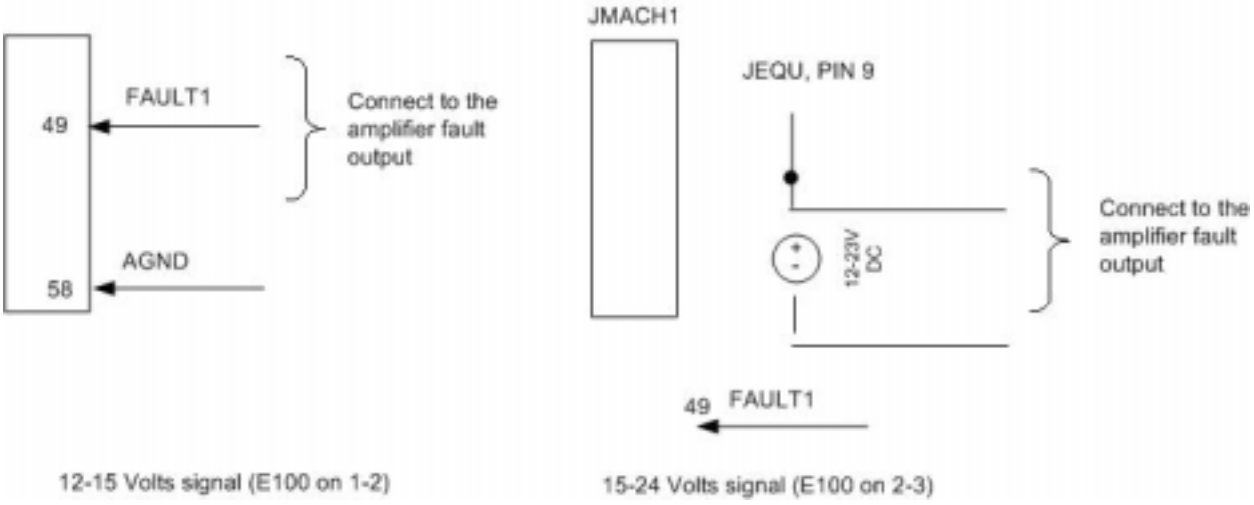
Most amplifiers have an enable/disable input that permits complete shutdown of the amplifier regardless of the voltage of the command signal. PMAC's AENA line is meant for this purpose. If not using a direction and magnitude amplifier or voltage-to-frequency converter, use this pin to enable and disable the amplifier (wired to the enable line). AENA1/DIR1 is pin 47. This signal is an open-collector output with a 3.3 kΩ pull-up resistor to +V, which is a voltage selected by jumper E100. The pull-up resistor packs are RP43 for channels 1-4. For early tests, this amplifier signal should be under manual control.



This signal could be either sinking or sourcing as determined by chips U37. (See jumpers E100-E102.) For 24V operation, E100 must connect pins 2-3 and a separate power supply must be brought on pins 9-7 of the J9 JEQU connector. The polarity of the signal is controlled by jumpers E17A to E17D. The default is low-true (conducting) enable. Also the amplifier enable signal could be manually controlled by setting Ix00=0 and using the suggested definition of the Mx14 variable.

Amplifier Fault Signal (FAULTn)

This input can take a signal from the amplifier so PMAC knows when the amplifier is having problems, and can shut down action. The polarity is programmable with I-variable Ix25 (I125 for motor #1) and the return signal is analog ground (AGND). FAULT1 is pin 49. With the default setup, this signal must be actively pulled low for a fault condition. In this setup, if nothing is wired into this input, PMAC will consider the motor not to be in a fault condition. The amplifier fault signal could be monitored using the properly defined Mx23 variable.



Some amplifiers share the fault output with the enable\disable status output. In this case a special PLC code must be written with the following sequence:

- Disable the amplifier fault input (see Ix25)
- Enable the motor (J/ command).
- Wait for the amplifier fault input to be false (monitor Mx23).
- Re-enable the amplifier fault input (see Ix25).

General-Purpose Digital Inputs and Outputs (JOPTO Port)

PMAC's J5 or JOPTO connector provides eight general-purpose digital inputs and eight general-purpose digital outputs. Each input and each output has its own corresponding ground pin in the opposite row. The 34-pin connector was designed for easy interface to OPTO-22 or equivalent optically isolated I/O modules. Delta Tau's Accessory 21F is a six-foot cable for this purpose. Characteristics of the JOPTO port on the PMAC:

- 16 I/O points. 100mA per channel, up to 24V
- Hardware selectable between sinking and sourcing in groups of eight; default is all sinking (inputs can be changed simply by moving a jumper; sourcing outputs must be special-ordered or field-configured)
- Eight inputs, eight outputs only; no changes. Parallel (fast) communications to PMAC CPU
- Not opto-isolated; easily connected to Opto-22 (PB16) or similar modules through ACC-21F cable

Jumper E7 controls the configuration of the eight inputs. If it connects pins 1 and 2 (the default setting), the inputs are biased to +5V for the OFF state, and they must be pulled low for the ON state. If E7 connects pins 2 and 3, the inputs are biased to ground for the OFF state, and must be pulled high for the ON state. In either case, a high voltage is interpreted as a 0 by the PMAC software, and a low voltage is interpreted as a 1.

Caution

Do not connect these outputs directly to the supply voltage, or damage to the PMAC will result from excessive current draw.

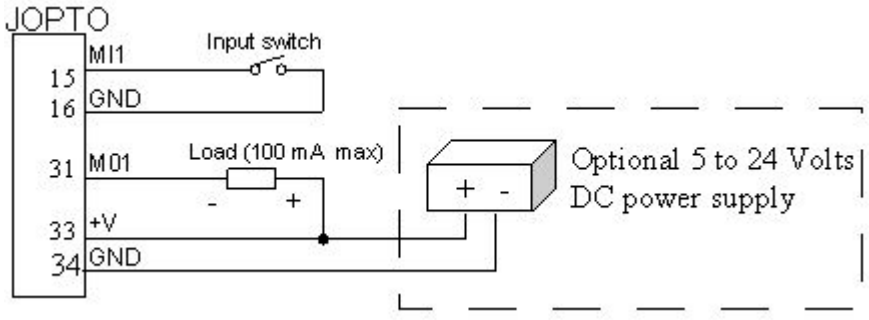
Having Jumpers E1 and E2 set wrong can damage the IC. The +V output on this connector has a 2A fuse, F1, for excessive current protection.

PMAC is shipped standard with a ULN2803A sinking (open-collector) output IC for the eight outputs. These outputs can sink up to 100mA and have an internal 3.3 kΩ pull-up resistor to go high (RP18). A high-side voltage (+5 to +24V) may be provided to pin 33 of the JOPTO connector, and allow this to pull up the outputs by connecting pins 1 and 2 of jumper E1. Also, jumper E2 must connect pins 1 and 2 for a ULN2803A sinking output.

It is possible for these outputs to be sourcing drivers by substituting a UDN2981A IC for the ULN2803A. This U13 IC is socketed, and so may be replaced easily. For this driver, the internal resistor packs pull-down instead. With a UDN2981A driver IC, Jumper E1 must connect pins 2 and 3, and Jumper E2 must connect pins 2 and 3.

The outputs can be configured individually to a different output voltage by removing the internal pull-up resistor pack RP18 and connecting a separate external pull-up resistor to the desired voltage level to each output.

Example: Standard configuration using the ULN2803A sinking (open-collector) output IC



Control-Panel Port I/O (JPAN Port)

The J2 (JPAN) connector is a 26-pin connector with dedicated control inputs, dedicated indicator outputs, a quadrature encoder input, and an analog input. The control inputs are low-true with internal pull-up resistors. They have predefined functions unless the control-panel-disable I-variable (I2) has been set to 1. If this is the case, they may be used as general-purpose inputs by assigning M-variable to their corresponding memory-map locations (bits of Y address $FFC0).

Command Inputs

JOG-/, JOG+/, PREJ/ (return to pre-jog position), and HOME/ affect the motor selected by the FDPn/ lines (see below). The ones that affect a coordinate system are STRT/ (run), STEP/, STOP/ (abort), and HOLD/ (feed hold) affect the coordinate system selected by the FDPn/ lines.

Caution

It is not a good idea to change the selector inputs while holding one of the jog inputs low, for releasing the jog input will not stop the previously selected motor. This can lead to a dangerous situation.

Selector Inputs

The four low-true BCD-coded input lines FDP0/ (LSBit), FDP1/, FDP2/, and FDP3/ (MSBit) form a low-true BCD-coded nibble that selects the active motor and coordinate system (simultaneously). Usually, these are controlled from a single 4-bit motor/coordinate-system selector switch. The motor selected with these input lines will respond to the motor-specific inputs. It will also have its position following function turned on (Ix06 is set to 1 automatically.); the motor just de-selected has its position following function turned off (Ix06 is set to 0 automatically.).

Alternate Use

If I2 has been set to 1, the discrete inputs can be used for parallel-data servo feedback or master position. The ACC-39 Handwheel Encoder Interface board provides 8-bit parallel counter data from a quadrature encoder to these inputs. Refer to the ACC-39 manual and Parallel Position Feedback Conversion section in the Setting Up A Motor chapter for more details.

Reset Input

Input INIT/ (reset) affects the entire card. It has the same effect as cycling power or a host $$$ command. It is hard-wired, so it retains its function even if I2 is set to 1.

Handwheel Inputs

The handwheel inputs HWCA and HWCB can be connected to the second encoder counter on PMAC with jumpers E22 and E23. If these jumpers are ON, nothing else should be connected to the Encoder 2 inputs. The signal can be interpreted either as quadrature or as pulse (HWCA) and direction (HWCB), depending on the value of I905. I905 also controls the direction sense of this input. Make sure that the Encoder 2 jumper E26 is set for single ended signals, connecting pins 1 and 2.

Optional Voltage to Frequency Converter

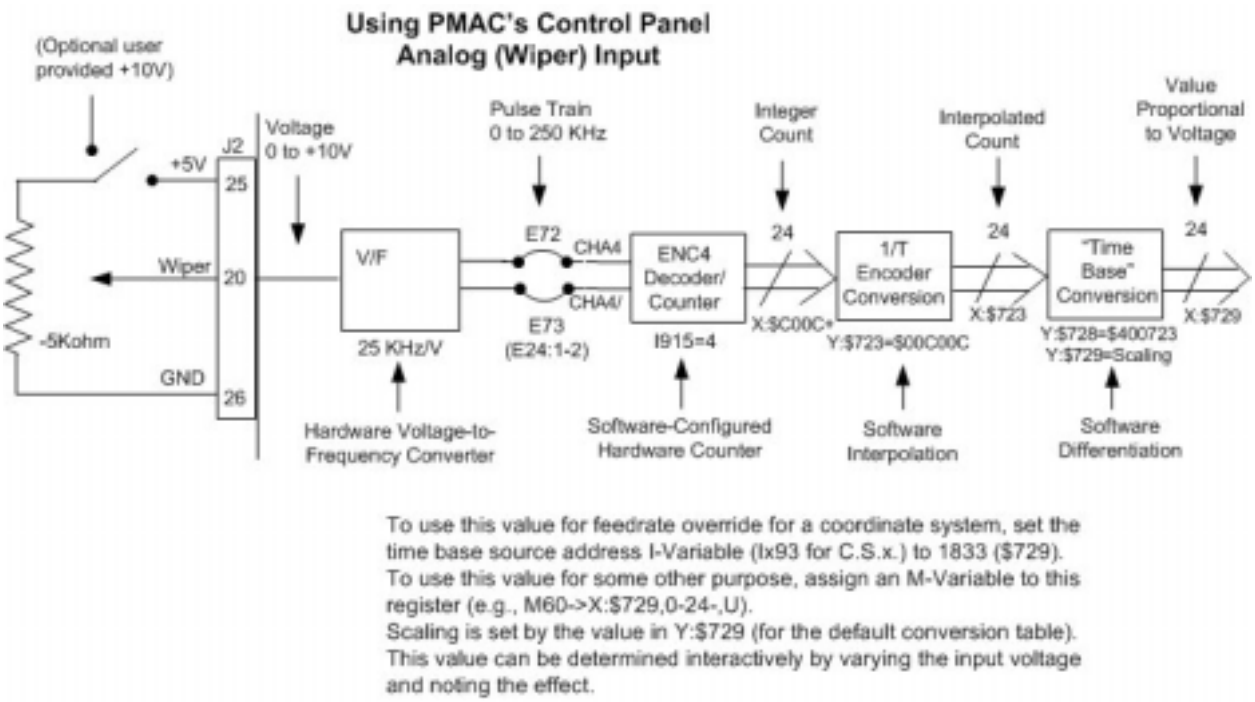
The Wiper analog input (0 to +10V on PMAC referenced to digital ground) provides an input to a voltage-to-frequency converter (V/F) with a gain of 25kHz/V, providing a range of 0-250kHz. The output of the V/F can be connected to the Encoder 4 counter using jumpers E72 and E73. If these jumpers are ON, nothing else should be connected to the Encoder 4 inputs. Make sure that the Encoder 4 jumper E24 is set for single-ended signals, connecting pins 1 and 2. This feature requires Option15.

Frequency Decode

When used in this fashion, set up Encoder 4 for pulse-and-direction decode by setting I915 to 0 or 4. A value of 4 is usually used, because with CHB4 (direction) unconnected, a positive voltage causes the counter to count up. The encoder conversion table can then take the difference in the counter each servo cycle and scale it, providing a value proportional to frequency, and therefore to the input voltage. Usually this is used for feedrate override (time base control), but the resulting value can be used for any purpose. The resulting value in the default setup can be found at X:$729,24.

Power Supply

For the V/F converter to work, PMAC must have +/-12V supply referenced to digital ground. If PMAC is in a bus configuration, usually this comes through the bus connector from the bus power supply. In a standalone configuration, this supply must be brought through the bus connector (or the supply terminal block), or it must be jumpered over from the analog side with E85, E87, and E88, defeating the optical isolation on the board.



Thumbwheel Multiplexer Port (JTHW Port)

The Thumbwheel Multiplexer Port, or Multiplexer Port, on the JTHW (J3) connector has eight input lines and eight output lines. The output lines can be used to multiplex large numbers of inputs and outputs on the port, and Delta Tau provides accessory boards and software structures (special M-variable definitions) to capitalize on this feature. Up to 32 of the multiplexed I/O boards may be daisychained on the port, in any combination.

- The ACC-18 Thumbwheel Multiplexer board provides up to 16 BCD thumbwheel digits or 64 discrete TTL inputs per board. The TWD and TWB forms of M-variables are used for this board.
- The ACC-34x family Serial I/O Multiplexer boards provide 64 I/O point per board, optically isolated from PMAC. The TWS form of M-variables is used for these boards.
- The ACC-8D Option 7 Resolver-to-Digital Converter board provides up to four resolver channels whose absolute positions can be read through the thumbwheel port. The TWR form of M-variables is used for this board.
- The ACC-8D Option 9 Yaskawa™ Absolute Encoder Interface board can connect to up to four of these encoders. The absolute position is read serially through the multiplexer port on power up.

If none of these accessory boards is used, the inputs and outputs on this port may be used as discrete, non-multiplexed I/O. They map into PMAC's processor space at Y address $FFC1. The suggested M-variable definitions for this use are M40 to M47 for the eight outputs, and M50 to M57 for the eight inputs. The ACC-27 Optically Isolated I/O board buffers the I/O in this non-multiplexed form, with each point rated to 24V and 100mA.

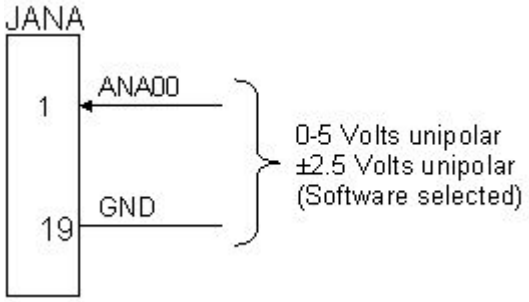
Optional Analog Inputs (JANA Port)

The JANA port is present only if Option 12 is ordered for the PMAC. Option 12 provides eight 12-bit analog inputs (ANAI00-ANAI07). Option 12A provides eight additional 12-bit analog inputs (ANA08-ANAI15) for a total of 16 inputs. The analog inputs can be used as unipolar inputs in the 0V to +5V range, or bi-polar inputs in the -2.5V to +2.5V range.

The analog-to-digital converters on PMAC require +5V and -12V supplies. These supplies are not isolated from digital +5V circuitry on PMAC. If the PMAC is plugged into the PCI bus, the supplies are taken from the bus power supply. In a standalone application, the supplies must be brought in on terminal block TB1. The -12V and matching +12V supply voltages are available on the J30 connector to supply the analog circuitry providing the signals.

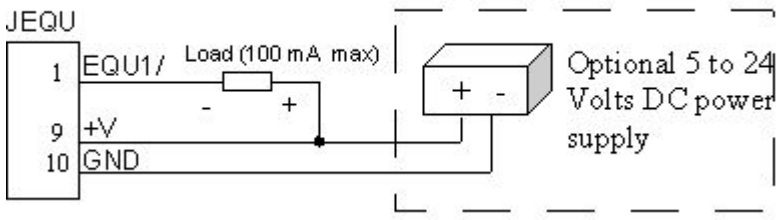
Only one pair of analog-to-digital converter registers is available to the PMAC processor at any given time. The data appears to the processor at address Y:$FFC8. The data from the selected analog input 0 to 7 (ANAI00-ANAI07) appears in the low 12 bits; the data from the selected analog input 8 to 15 (ANAI08-ANAI15) appears in the high 12 bits (this data is present only if Option 12A has been ordered). The input is selected and the conversion is started by writing to this same word address Y:$FFC8. A value of 0 to 7 written into the low 12 bits selects the analog input channel of that number (ANAI00-ANAI07) to be converted in unipolar mode (0V to +5V). A value of 0 to 7 written into the high 12 bits selects the analog input channel numbered eight greater (ANAI08-ANAI15) in unipolar mode. If the value written into either the low 12 bits or the high 12 bits is eight higher (8 to 15), the same input channel is selected, but the conversion is in bipolar mode (-2.5V to +2.5V).

PMAC variables I60 and I61 allow an automatic conversion of the analog inputs. Setting I60=$FFC8 and I61 with the number of converted registers desired minus one, the converted data can be found in registers $0708 to $070F. See the PMAC Software Reference manual for further details.



Compare Equal Outputs Port (JEQU Port)

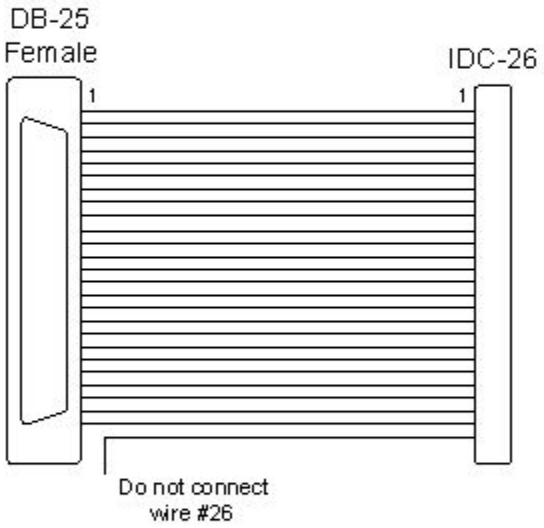
The compare-equals (EQU) outputs have a dedicated use of providing a signal edge when an encoder position reaches a pre-loaded value. This is very useful for scanning and measurement applications. Instructions for use of these outputs are presented in the PMAC's User Manual.



Outputs can be configured sinking or sourcing by replacing the chips U37 and configuring the jumpers E101-102. The voltage levels can be individually configured by removing resistor pack RP43 and connecting an external pull-up resistor in each output to the desired voltage level.

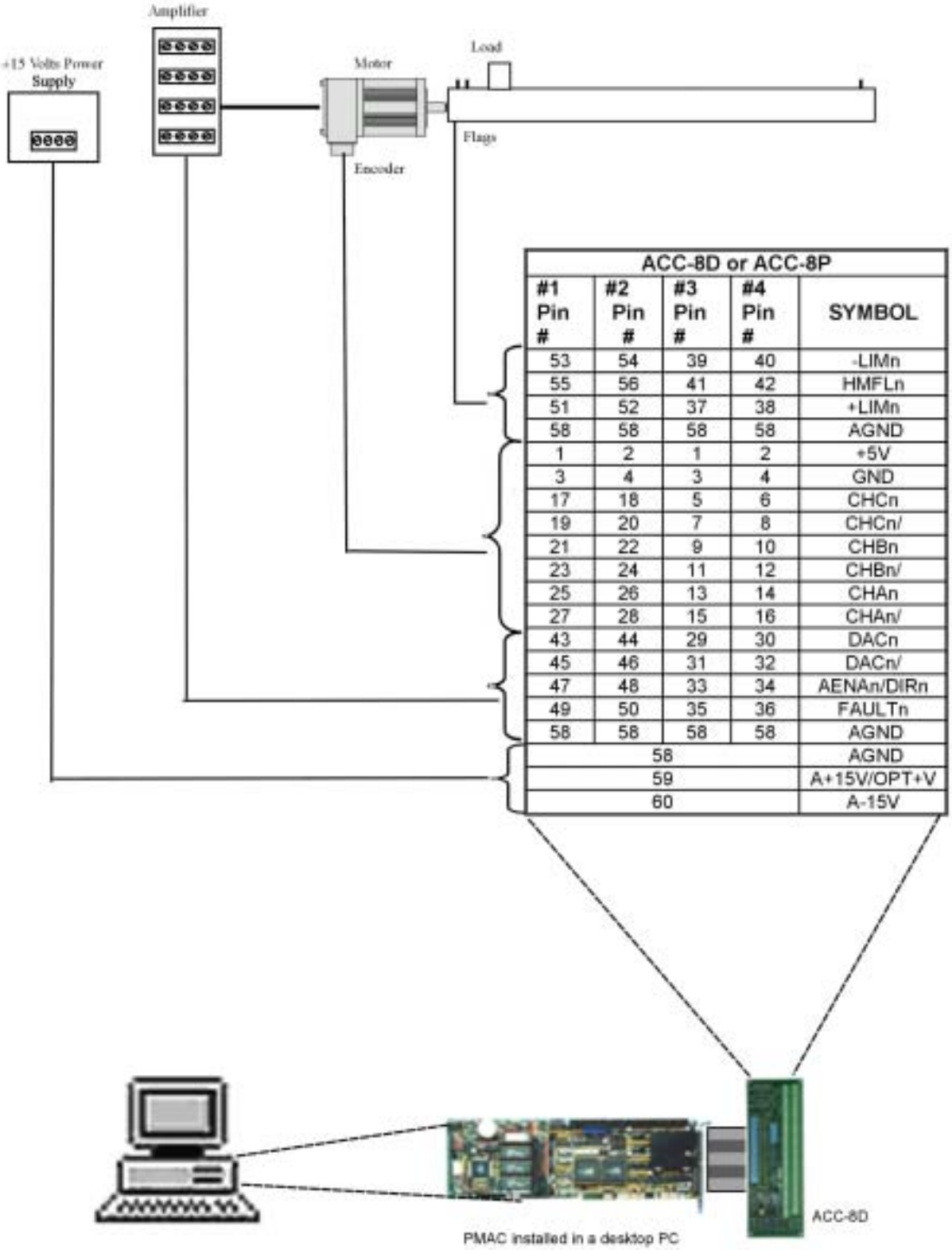
Serial Port (JRS422 Port)

For serial communications, use a serial cable to connect the PC's COM port to the PMAC's J4 serial port connector. Delta Tau provides the Accessory 3D cable to connect the PMAC-PCI to a DB-25 connector. Standard DB-9-to-DB-25 or DB-25-to-DB-9 adapters may be needed for a particular setup. Jumper E110 selects between RS-232 and RS422 signal types for the J4 connector. If a cable needs to be made, use a flat cable prepared with flat-cable type connectors as indicated in the following diagram:



PMAC (IDC-26)	PC (DB-25)
1	1
2	14
3	2 (TXD)
4	15
5	3 (RXD)
6	16
7	4 (RTS)
8	17
9	5 (CTS)
10	18
11	6 (DSR)
12	19
13	7 (Gnd)
14	20 (DTR)
15	8
16	21
17	9
18	22
19	10
20	23
21	11
22	24
23	12
24	25
25	13
26	No connect

Machine Connections Example



ACC-8D or ACC-8P				
#1 Pin #	#2 Pin #	#3 Pin #	#4 Pin #	SYMBOL
53	54	39	40	-LIMn
55	56	41	42	HMFLn
51	52	37	38	+LIMn
58	58	58	58	AGND
1	2	1	2	+5V
3	4	3	4	GND
17	18	5	6	CHCn
19	20	7	8	CHCn/
21	22	9	10	CHBn
23	24	11	12	CHBn/
25	26	13	14	CHAn
27	28	15	16	CHAn/
43	44	29	30	DACn
45	46	31	32	DACn/
47	48	33	34	AENAn/DIRn
49	50	35	36	FAULTn
58	58	58	58	AGND
58				AGND
59				A+15V/OPT+V
60				A-15V

Note: For this configuration, jumpers E85, E87, E88, E89, and E90 are left at the default settings

PMAC PCI-LITE SOFTWARE SETUP

Note

The PMAC PCI-Lite requires the use of V1.17 or newer firmware. There are few differences between the previous V1.16H firmware and the V1.17 firmware other than the addition of internal support for the Flex CPU design.

Communications

Delta Tau provides communication tools that take advantage of the PCI bus Plug & Play feature of 32-bits Windows® based computers. With PEWIN32 Pro, a PMAC PCI-Lite board plugged in a PCI bus slot will be recognized by the operating system when the computer is booted up. The available PCI address, Dual Ported RAM address and Interrupt lines are set automatically by the operating system and can be checked (but not modified) in the resources page of the device manager.

PMAC I-Variables

PMAC has a large set of Initialization parameters (I-variables) that determine the personality of the card for a specific application. Many of these are used to configure a motor properly. Once set up, these variables may be stored in non-volatile EAROM memory (using the **SAVE** command) so the card is always configured properly (PMAC loads the EAROM I-variable values into RAM on power-up).

The easiest way to program, set up and troubleshoot PMAC is by using the PMAC Executive Program PEWIN and its related add-on packages P1Setup and PMACPlot. These software packages are available by ordering the ACC-9WN accessory.

The programming features and configuration variables for the PMAC are fully described in the PMAC User and Software manuals.

Operational Frequency and Baud Rate Setup

Note

Older PMAC boards required a start-up PLC for setting the operational frequency at 80 MHz. That method is not compatible with the PMAC PCI-Lite board and will shut down the board when used.

The operational frequency of the CPU is set in software by the PMAC I46 I- variable. If this variable is set to 0, PMAC firmware looks at the jumper E48 to set the operational frequency. If I46 is set to a value greater than 0, the operational frequency is set to 10MHz * (I46 + 1), regardless of the jumper setting. If the desired operational frequency is higher than the maximum rated frequency for that CPU, the operational frequency will be reduced to the rated maximum. It is always possible to operate the Flex CPU board at a frequency below its rated maximum. I46 is used only at power-up/reset. To change the operational frequency, set a new value of I46, issue a **SAVE** command to store this value in non-volatile flash memory. Then issue a **$$$** command to reset the controller.

To determine the frequency at which the CPU is actually operating, issue the **TYPE** command to the PMAC. The PMAC will respond with five data items, the last of which is `CLK Xn`, in which *n* is the multiplication factor from the 20MHz crystal frequency (not 10MHz). *n* should be equivalent to (I46+1)/2 if I46 is not requesting a frequency greater than the maximum rated for that CPU board. *n* will be 2 for 40MHz operation, 4 for 80MHz operation, and 8 for 160MHz operation.

If the CPU's operational frequency has been determined by (a non-zero setting of) I46, the serial communications baud rate is determined at power-up/reset by variable I54 alone according to the following table:

I54	Baud Rate	I54	Baud Rate
0	600	8	9600
1	900	9	14,400
2	1200	10	19,200
3	1800	11	28,800
4	2400	12	38,400
5	3600	13	57,600
6	4800	14	76,800
7	7200	15	115,200*
* The CPU must be run at an exact multiple of 30MHz in order to use 115,200 baud serial communications. Otherwise, the baud rate will not be exact enough to ensure proper communications.			

The card number (0 – 15) for serial addressing of multiple cards on a daisychain serial cable is determined by variable I0. Jumpers E40 – E43 determine the direction of the phase and servo clocks. All of these jumpers must be ON for the card to use its internally generated clock signals and to output these on the serial port connector. If any of these jumpers is OFF, the card will expect to input these clock signals from the serial port connector, and its watchdog timer will trip immediately if it does not receive these signals.

Serial Addressing Card Number

I0 controls the card number for software addressing purposes on a multi-drop serial communications cable. If I2 is set to 2, the PMAC must be addressed with the @n command where *n* matches the value of I0 on the board, before it will respond. If the PMAC receives the @n command where *n* does not match I0 on the board, it will stop responding to commands on the serial port. No two boards on the same serial cable may have the same value of I0.

If the @@ command is sent over the serial port, all boards on the cable will respond to action commands. However, only the board with I0 set to 0 will respond to the host with handshake characters and/or data responses. All boards on the cable will respond to control-character action commands such as <CTRL-R>, regardless of the current addressing.

Note

RS-422 serial interfaces must be used on all PMAC boards for multi-drop serial communications. This will not work with RS-232 interfaces. Typically, multiple PMAC boards on the same serial cable will share servo and phase clock signals over the serial port cable for tight synchronization. If the servo and phase clock lines are connected between multiple PMACs, only one of the PMAC boards can be set up to output these clocks (E40 – E43 all ON for a PMAC PCI-Lite). All of the other boards in the chain must be set up to input these clocks (one or more of the jumpers E40 – E43 OFF for a PMAC PCI-Lite).

Any PMAC PCI-Lite board with one or more of E40 – E43 OFF is expecting its Servo and Phase clock signals externally from a Card 0. If it does not receive these clock signals, the watchdog timer will immediately shut down the board and the red LED will light.

If the PMAC PCI-Lite is set to receive external Servo and Phase clock signals for synchronization purposes, but is not using multi-drop serial communications, I0 does not need to be changed from 0.

To set up a board to communicate as Card 1 to Card 15 on a multi-drop serial cable, first communicate with the board as Card 0. Set I0 to specify the card number (software address) that the board will have on the multi-drop cable. Also, set I1 to 2 to enable the serial software addressing. Store these values to the non-volatile flash memory with the **SAVE** command. Then turn off power. If the board is to input its clocks, remove any of the E40-E43 jumpers. Connect the multi-drop cable. Restore power to the system.

Option 16 Supplemental Battery-Backed Memory

If Option 16 supplemental battery-backed parameter memory is ordered, an extra bank of memory with battery backup circuitry is provided. This option can be ordered only if the main memory is flash backed (Option 4A, 5A, 5B, or 5C). This memory is for user parameter storage only. From PMAC programs it can be accessed with M-variables only (L-variables also in compiled PLCs). The on-line direct-memory read and write commands can be used from the host computer as well.

With M-variable access, arrays can be created with indirect addressing techniques by pointing a second M-variable to the definition of a first M-variable that points into this memory area. For example, with the M-variable definitions:

```
M0->L:$A000           ; 1st long word of Opt. 16 RAM; floating point
M10->Y:$BC000,0,16    ; Low 16 bits of M0 def., with pointer address
```

The following code segment could load a sine table into the first 360 words of the Option 16 RAM:

```
P1=0
WHILE (P1<360)
  M10=$A000+P1        ; Sets address that M0 points to
  M0=SIN(P1)          ; Puts value in register that M0 points to
  P1=P1+1
ENDWHILE
```

Note

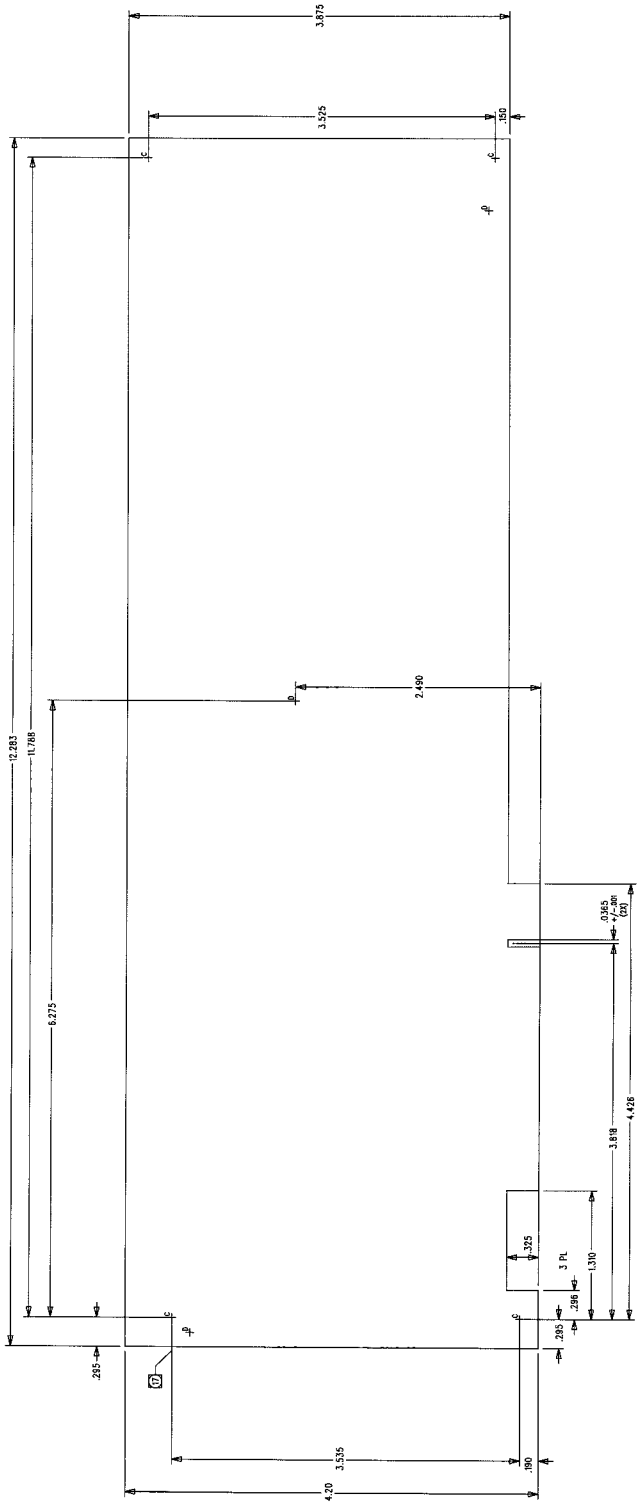
This technique is not possible with L-variables in compiled PLCs. But it is possible with M-variables in compiled PLCs.

Physically, the Option 16 memory is a 16k x 24 bank of battery-backed static RAM. It maps into the PMAC and PMAC2 at addresses $A000 to $BFFF, on both the X and Y data buses, an 8k x 48 block of address space. Addresses Y:$BC00 to Y:$BFFF are double-mapped with the main flash-backed RAM for the M-variable definitions, and should not be used for user parameter storage.

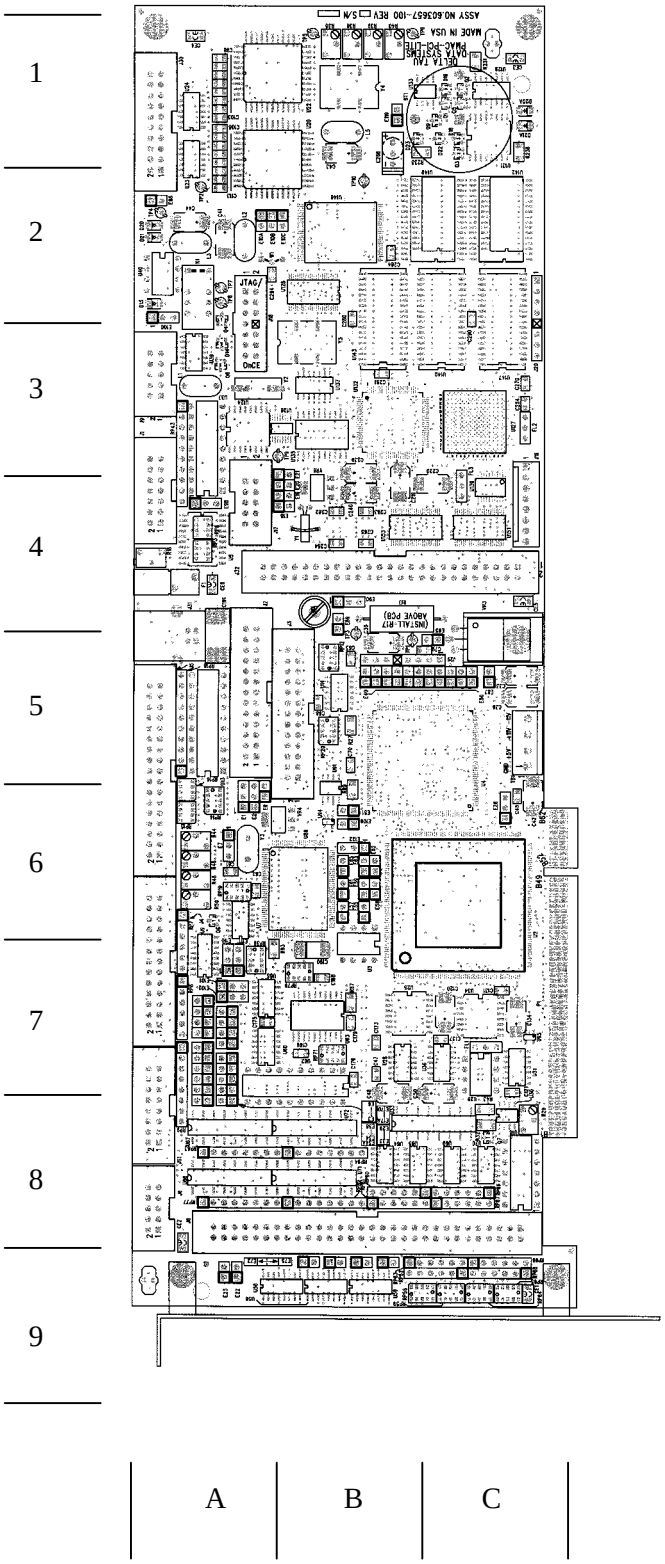
Any value written into the Option 16 memory will be retained automatically through a power-down or reset; no **SAVE** operation is required. The power draw on the battery is low enough that typically battery life will be limited only by the quoted 10-year life of the battery.

HARDWARE REFERENCE SUMMARY

PMAC PCI-Lite Board Dimensions — Part Number 603657-100



PMAC PCI-Lite Board Layout. Part Number 603657-10x



Feature	Location	Feature	Location
E0	A6	E55	B7
E1	A6	E57	B7
E2	A6	E58	B7
E3	A8	E59	B7
E4	A8	E61	B7
E5	A7	E62	B7
E6	A7	E63	B6
E7	A6	E65	B6
E10A	A2	E72	A9
E10B	A2	E73	A9
E10C	B2	E74	A9
E17A	A8	E75	B9
E17B	A8	E85	B5
E17C	A8	E87	C5
E17D	A7	E88	A2
E18	B4	E89	B5
E19	B4	E90	B5
E20	B4	E98	A4
E21	B4	E100	A3
E22	A9	E101	A7
E23	A9	E102	A7
E28	C6	E109	B6
E29	A8	E110	A7
E30	A8	E111	A7
E31	A8	E119	B6
E32	A8	E122	B6
E33	A8	D15	A3
E34	A8	D20	A2
E34A	A8	D20A	C1
E35	A8	D21	A2
E36	A8	D21A	C1
E37	A8	F1	A4
E38	A8	J1	A4
E40	B5	J2	A5
E41	B5	J3	B5
E42	B5	J4	A7
E43	B5	J5	A5
E44	B5	J6	A9
E45	B5	J8	B9
E46	C5	J9	A3
E47	C5	J17	A4
E48	C5	J30	A1
E49	C5	J31	A5
E50	C5	JS1	A8
E51	B6	TB1	C6

PMAC PCI-Lite Connectors and Indicators

J1 - Display Port (JDISP Port)

The JDISP connector allows connection of the ACC-12 or ACC-12A liquid crystal displays, or of the ACC-12C vacuum fluorescent display. Both text and variable values may be shown on these displays through the use of the **DISPLAY** command, executing in either motion or PLC programs.

J2 - Control-Panel Port (JPAN Port)

The JPAN connector is a 26-pin connector with dedicated control inputs, dedicated indicator outputs, a quadrature encoder input, and an analog input (requires PMAC Option 15). The control inputs are low true with internal pull-up resistors. They have predefined functions unless the control-panel-disable I-variable (I2) has been set to 1. If this is the case, they may be used as general-purpose inputs by assigning M-variable to their corresponding memory-map locations (bits of Y address $FFC0).

J3 - Thumbwheel Multiplexer Port (JTHW Port)

The Thumbwheel Multiplexer Port, or Multiplexer Port, on the JTHW connector has eight input lines and eight output lines. The output lines can be used to multiplex large numbers of inputs and outputs on the port, and Delta Tau provides accessory boards and software structures (special M-variable definitions) to capitalize on this feature. Up to 32 of the multiplexed I/O boards may be daisychained on the port, in any combination.

J4 - Serial Port (JRS422 Port)

For serial communications, use a serial cable to connect the PC's COM port to the PMAC's serial port connector. Delta Tau provides the accessory 3D cable for this purpose, which connects PMAC to a DB-25 connector. Standard DB-9-to-DB-25 or DB-25-to-DB-9 adapters may be needed for a particular setup.

J5 - General-Purpose Digital Inputs and Outputs (JOPTO Port)

PMAC's JOPTO connector provides eight general-purpose digital inputs and eight general-purpose digital outputs. Each input and each output has its own corresponding ground pin in the opposite row. The 34-pin connector was designed for easy interface to OPTO-22 or equivalent optically isolated I/O modules. Delta Tau's Accessory 21F is a six-foot cable for this purpose.

J6 – Expansion Port (JXIO Port)

This port is used only when connecting to optional PMAC accessory boards.

J8 - Machine Connectors (JMACH Port)

The primary machine interface connector is JMACH, labeled J8 on the PMAC. It contains the pins for four channels of machine I/O: analog outputs, incremental encoder inputs, and associated input and output flags, plus power-supply connections.

J9 – Compare Equal Outputs Port (JEQU Port)

The compare-equals (EQU) outputs have a dedicated use of providing a signal edge when an encoder position reaches a pre-loaded value. This is useful for scanning and measurement applications. Instructions for use of these outputs are presented in the PMAC's User Manual.

J17 - Serial Port (JRS232 Port)

This connector applies only to the turbo version of the PMAC PCI-Lite board. It allows PMAC to communicate through its auxiliary RS-232 serial port.

J30 – Optional Analog to Digital Inputs (JANA Port)

This optional port is used to bring in the analog signals for the optional analog to digital inputs set. This feature provides up to 16 analog inputs in the range of 0 to 5V unipolar or ±2.5V bipolar.

J31 – Optional Universal Serial Bus Port (JUSB Port)

This optional port allows communication with PMAC through a standard USB connection.

JS1 – Expansion Ports (JS1 Port)

This port is used only when connecting to optional PMAC accessory boards.

TB1 – Power Supply Terminal Block (JPWR Connector)

This terminal block may be used as an alternative power supply connector if PMAC is not installed in a PCI-bus.

LED Indicators

D20 and D20A: when these green LEDs are lit, they indicate that power is applied to the +5V input.

D21 and D21A: when these red LEDs are lit, they indicate that the watchdog timer has tripped and shut down the PMAC.

D15: The PMAC has an interlock circuit that drops out the ±15V supplies to the analog outputs through a fail-safe relay if any supply on PMAC is lost. In this case the green LED D15 will be off.

Fuse

The 5V output through the J5 JOPTO connector is protected by F1, which is a 2-Amp fuse of the following type:

Manufacturer: LittleFuse

Part Number: 021-273002-004

PMAC PCI-LITE E-POINT JUMPER DESCRIPTIONS

E0: Reserved for Future Use

E Point & Physical Layout	Location	Description	Default
E0 	A6	For future use.	No jumper

E1 - E2: Machine Output Supply Voltage Configure

E Point & Physical Layout	Location	Description	Default
E1 	A6	Jump pin 1 to 2 to apply +V (+5V to 24V) to pin 10 of U13 (should be ULN2803A for sink output configuration) JOPTO Machine outputs M01-M08. ***Caution*** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 2 to 3 to apply GND to pin 10 of U13 (should be UDN2981A for source output configuration).	1-2 Jumper installed
E2 	A6	Jump pin 1 to 2 to apply GND to pin 10 of U13 (should be ULN2803A for sink output configuration). ***Caution*** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 2 to 3 to apply +V (+5V to 24V) to pin 10 of U13 (should be UDN2981A for source output configuration).	1-2 Jumper installed

E3 - E6: Servo Clock Frequency Control

The servo clock (which determines how often the servo loop is closed) is derived from the phase clock (see E98, E29 - E33) through a divide-by-N counter. Jumpers E3 through E6 control this dividing function.

E3	E4	E5	E6	Servo Clock = Phase Clock Divided By N	Default & Physical Layout E3 E4 E5 E6  Location A8 A8 A7 A7
On	On	On	On	N = divided by 1	
Off	On	On	On	N = divided by 2	
On	Off	On	On	N = divided by 3	
Off	Off	On	On	N = divided by 4	Only E5 and E6 ON
On	Off	On	On	N = divided by 5	
Off	On	Off	On	N = divided by 6	
On	Off	Off	On	N = divided by 7	
Off	Off	Off	On	N = divided by 8	
On	On	On	Off	N = divided by 9	
Off	On	On	Off	N = divided by 10	
On	Off	On	Off	N = divided by 11	
Off	Off	On	Off	N = divided by 12	
On	On	Off	Off	N = divided by 13	
Off	On	Off	Off	N = divided by 14	
On	Off	Off	Off	N = divided by 15	
Off	Off	Off	Off	N = divided by 16	

Note: Adjust the setting of I-variable I10 to match the servo interrupt cycle time set by E98, E3 – E6, E29 – E33, and the crystal clock frequency. I10 holds the length of a servo interrupt cycle, scaled so that 8,388,608 equals one millisecond. Since I10 has a maximum value of 8,388,607, the servo interrupt cycle time should always be less than a millisecond (unless the basic unit of time on PMAC should be something other than a millisecond). To have a servo sample time greater than one millisecond, the sampling may be slowed in the software with variable Ix60.

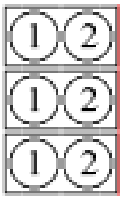
Frequency can be checked on J4 pins 21 & 22. It can also be checked from the software by typing RX:0 in the PMAC terminal at 10 second intervals and dividing the difference of successive responses by 10000. The resulting number is the approximate Servo Clock frequency kHz.

Note: If E40-E43 are not all ON, the phase clock is received from an external source through the J4 serial-port connector, and the settings of E3 – E6 are not relevant.

E7: Machine Input Source/Sink Control

E Point & Physical Layout	Location	Description	Default
E7  	A6	Jump pin 1 to 2 to apply +5V to input reference resistor SIP pack; this will bias MI1 to MI8 inputs to +5V for OFF state; then input must be grounded for ON state. Jump pin 2 to 3 to apply GND to input reference resistor SIP pack; this will bias MI1 to MI8 inputs to GND for OFF state; then input must be pulled up for ON state (+5V to +24V).	1-2 Jumper installed

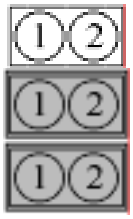
E10A, B, C: Flash Memory Bank Select

E Point & Physical Layout	Location	Description	Default
E10A  **E10C**	A2	Remove all three jumpers to select flash memory bank with factory-installed firmware. Use other configurations to select one of the seven flash memory banks.	No jumpers installed

E17A-D: Amplifier Enable/Direction Polarity Control

E Point & Physical Layout	Location	Description	Default
E17A  	A8	Jump 1-2 for high-true AENA1. Remove jumper for low-true AENA1.	No jumper installed
E17B  	A8	Jump 1-2 for high-true AENA2. Remove jumper for low-true AENA2.	No jumper installed
E17C  	A8	Jump 1-2 for high-true AENA3. Remove jumper for low-true AENA3.	No jumper installed
E17D  	A7	Jump 1-2 for high-true AENA4. Remove jumper for low-true AENA4.	No jumper installed
Note: Low-true enable is the fail-safe option because of the sinking (open-collector) ULN2803A output driver IC.			

E18 – E20: Power-Up/Reset Load Source

E Point & Physical Layout	Location	Description	Default
E18  **E20**	B4	Remove jumper E18. Jump E19. Jump E20 to read flash IC on power-up/reset. Other combinations are for factory use only; the board will not operate in any other configuration.	No E18 jumper installed. Jump E19 and E20.

E21: Power-Up/Reset Load Source

E Point & Physical Layout	Location	Description	Default
E21 	B4	Jump pin 1 to 2 to reload firmware through serial or bus port. Remove jumper for normal operation.	No jumper

E22 - E23: Control Panel Handwheel Enable

E Point & Physical Layout	Location	Description	Default
E22 	A9	Jump pin 1 to 2 to obtain handwheel encoder signal from front panel at J2-16 for CHB2 (ENC2-B).	No jumper
E23 	A9	Jump pin 1 to 2 to obtain handwheel encoder signal from front panel at J2-22 for CHA2 (ENC2-A).	No jumper
Note: With these jumpers ON, no encoder should be wired into ENC2 on JMACH1. Jumper E26 must connect pins 1-2, because these are single-ended inputs. This function is unrelated to the encoder brought in on J2 through ACC-39.			

E28: Following Error/Watchdog Timer Signal Control

E Point & Physical Layout	Location	Description	Default
E28 	C6	Jump pin 1 to 2 to allow warning following error (Ix12) for the selected coordinate system to control FEFCO/ on J8-57. Jump pin 2 to 3 to cause Watchdog timer output to control FEFCO/. Low TRUE output in either case.	2-3 Jumper installed

E29 - E33: Phase Clock Frequency Control

Jumpers E29 through E33 control the speed of the phase clock, and, indirectly, the servo clock, which is divided down from the phase clock (see E3 - E6). No more than one of these five jumpers may be on at a time.

					Phase Clock Frequency		Default &	
E29	**E30**	**E31**	**E32**	**E33**	**E98 Connects Pins 1 and 2**	**E98 Connects Pins 2 and 3**	**Physical Layout**	**Location**
On	Off	Off	Off	Off	2.26 kHz	1.13 kHz	 **E29**	A8
Off	On	Off	Off	Off	4.52 kHz	2.26 kHz	 **E30**	A8
Off	Off	On	Off	Off	9.04 kHz	4.52 kHz	 **E31**	A8
Off	Off	Off	On	Off	18.07 kHz	9.04 kHz	 **E32**	A8
Off	Off	Off	Off	On	36.14 kHz	18.07 kHz	 **E33**	A8
Note: If E40-E43 are not all ON, the phase clock is received from an external source through the J4 serial-port connector, and the settings of E29 – E33 are not relevant.								

E34A - E38: Encoder Sampling Clock Frequency Control

Jumpers E34A - E38 control the encoder-sampling clock (SCLK) used by the gate array ICs. No more than one of these six jumpers may be on at a time.

						SCLK Clock Frequency	Default & Physical Layout
E34A	**E34**	**E35**	**E36**	**E37**	**E38**		E34A E34 E35 E36 E37 E38  A8 A8 A8 A8 A8 A8
On	Off	Off	Off	Off	Off	19.6608 MHz	
Off	On	Off	On	Off	Off	9.8304 MHz	E34 ON
Off	Off	On	Off	Off	Off	4.9152 MHz	
Off	Off	Off	On	Off	Off	2.4576 MHz	
Off	Off	Off	Off	On	Off	1.2288 MHz	
Off	Off	Off	Off	Off	On	External Clock 1 to 30MHz maximum input on CHC4 & CHC4/	

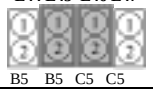
E40 - E43: Clock Direction Control

Jumpers E40 – E43 determine the direction of the phase and servo clocks. All of these jumpers must be ON for the card to use its internally generated clock signals and to output these on the serial port connector. If any of these jumpers is OFF, the card will expect to input these clock signals from the serial port connector, and its watchdog timer will trip immediately if it does not receive these signals. The card number (0 – 15) for serial addressing of multiple cards on a daisychain serial cable is determined by the PMAC variable I0. See the Software Setup section in this manual for details.

E Point & Physical Layout	Location	Description	Default
E40  **E43**	A2	Install all of these jumpers for the card to use its internally-generated clock signals and to output these on the serial port connector. If any of these jumpers is OFF, the card will expect to input these clock signals from the serial port connector.	Jumpers E40-E43 installed

E44 - E47: Serial Port Baud Rate

Jumpers E44 - E47 control the baud rate for serial communications if the saved value of I46 is 0 and jumper E48 controls the CPU frequency. If the saved value of I46 is greater than 0, I46 controls the CPU frequency and I54 controls the baud rate.

Baud Rate Control "E" Points				Baud Rate		Default & Physical Layout
E44	**E45**	**E46**	**E47**	**I46=0 E48 OFF**	**I46=0 E48 ON**	
On	On	On	On	Disabled	Disabled	
Off	On	On	On	600	900	
On	Off	On	On	800*	1200	
Off	Off	On	On	1200	1800	
On	On	Off	On	1600*	2400	
Off	On	Off	On	2400	3600	
On	Off	Off	On	3200*	4800	
Off	Off	Off	On	4800	7200	
On	On	On	Off	6400*	9600	
Off	On	On	Off	9600	14400	
On	Off	On	Off	12800*	19200	
Off	Off	On	Off	19200	28800	
On	On	Off	Off	25600*	38400	
Off	On	Off	Off	38400	57600	
On	Off	Off	Off	51200*	76800	
Off	Off	Off	Off	76800	115200	

E48: CPU Clock Frequency Control (Option CPU Section)

E48 controls the CPU clock frequency only if the saved value of I46 is 0. If the saved value of I46 is greater than 0, I46 controls the CPU frequency.

E Point & Physical Layout	Location	Description	Default
E48 	C5	Jump pins 1 and 2 to multiply crystal frequency by three inside CPU for 60MHz operation. Remove jumper to multiply crystal frequency by two inside CPU for 40 MHz operation.	Jumper installed (Option 5, 5B) Jumper not installed (Standard, Option 4A, 5A)

E49: Serial Communications Parity Control

E Point & Physical Layout	Location	Description	Default
E49 	C5	Jump pin 1 to 2 for no serial parity. Remove jumper for odd serial parity.	Jumper installed

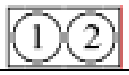
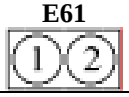
E50: Flash Save Enable/Disable

E Point & Physical Layout	Location	Description	Default
E50 	C5	Jump pin 1 to 2 to enable save to flash memory. Remove jumper to disable save to flash memory.	Jumper Installed

E51: Normal/Re-Initializing Power-Up

E Point & Physical Layout	Location	Description	Default
E51 	B6	Jump pin 1 to 2 to re-initialize on power-up/reset. Remove jumper for Normal power-up/reset.	No jumper installed

E54 - E65: Host Interrupt Signal Select

E Point & Physical Layout	Location	Description	Default
E55 	B7	Jump pin 1 to 2 to allow EQU4 to interrupt host-PC at PMAC interrupt level IR7.	No jumper installed
E57 	B7	Jump pin 1 to 2 to allow EQU3 to interrupt host-PC at PMAC interrupt level IR7.	No jumper installed
E58 	B7	Jump pin 1 to 2 to allow MI2 to interrupt host-PC at PMAC interrupt level IR6.	No jumper installed
E59 	B7	Jump pin 1 to 2 to allow Axis Expansion Int-0 to interrupt host-PC at PMAC interrupt level IR6.	No jumper installed
E61 	B7	Jump pin 1 to 2 to allow EQU2 to interrupt host-PC at PMAC interrupt level IR6.	No jumper installed
E62 	B7	Jump pin 1 to 2 to allow MI1 to interrupt host-PC at PMAC interrupt level IR5.	No jumper installed
E63 	B6	Jump pin 1 to 2 to allow Axis Expansion Int-1 to interrupt host-PC at PMAC interrupt level IR5.	No jumper installed
E65 	B6	Jump pin 1 to 2 to allow EQU1 to interrupt host-PC at PMAC interrupt level IR5.	No jumper installed

E72 - E73: Panel Analog Time Base Signal Enable

E Point & Physical Layout	Location	Description	Default
E72 	A9	Jump pin 1 to 2 to allow V-to-F converter FOUT derived from Wiper input on J2 to connect to CHA4.	No jumper installed
E73 	A9	Jump pin 1 to 2 to allow V-to-F converter FOUT/ derived from Wiper input on J2 to connect to CHA4/.	No jumper installed
Note: With these jumpers ON, no encoder should be wired into ENC4 on JMACH. E27 must connect pins 1 to 2 because these are single-ended inputs. Variable I915 should be set to 4 to create a positive voltage (frequency) number in PMAC.			

E74 - E75: Clock Output Control For Ext. Interpolation

E Point & Physical Layout	Location	Description	Default
E74 	A9	Jump pin 1 to 2 to allow SCLK/ to output on CHC4/.	No jumper installed
E75 	B9	Jump pin 1 to 2 to allow SCLK to output on CHC4.	No jumper installed
Note: SCLK out permits synchronous latching of analog encoder interpolators such as ACC-8D Option 8.			

E85: Host-Supplied Analog Power Source Enable

E Point & Physical Layout	Location	Description	Default
E85 	B5	Jump pin 1 to pin 2 to allow A+14V to come from PC bus. Ties amplifier and PMAC power supply together. Defeats OPTO coupling. ***Note*** If E85 is changed, E88 and E87 must also be changed. See E90.	No jumper

E87 - E88: Host-Supplied Analog Power Source Enable

E Point & Physical Layout	Location	Description	Default
E87 	C5	Jump pin 1 to pin 2 to allow AGND to come from PC bus. Ties amplifier and PMAC GND together. Defeats OPTO coupling. ***Note*** If E87 is changed, E85 and E88 must be changed also. See E90.	No jumper
E88 	A2	Jump pin 1 to pin 2 to allow A-14V to come from PC bus. Ties amplifier and PMAC power supply together. Defeats OPTO coupling. ***Note*** Note that if E88 is changed, E87 and E85 must be changed also. See E90.	No jumper

E89: Amplifier-Supplied Switch Pull-Up Enable

E Point & Physical Layout	Location	Description	Default
E89 	B5	Jump pin 1 to 2 to use A+15V on J8 (JMACH1) pin 59 as supply for input flags. Remove jumper to use A+15V/OPT+V from J9 pin 9 as supply for input flags. ***Note*** This jumper setting is only relevant if E90 connects pin 1 to 2.	Jumper installed

E90: Host-Supplied Switch Pull-Up Enable

E Point & Physical Layout	Location	Description	Default
E90 	B5	Jump pin 1 to 2 to use A+15V from J8 pin 59 as supply for input flags (E89 ON) {flags should be tied to AGND} or A+15V/OPT+V from J8 pin 11 as supply for input flags (E89 OFF) {flags should be tied to separate 0V reference}. Jump pin 2 to 3 to use +12V from PC bus connector P1 pin B09 as supply for input flags (flags should be tied to GND). See E85, E87, E88 and PMAC Opto-isolation diagram.	1-2 Jumper installed

E98: DAC/ADC Clock Frequency Control

E Point & Physical Layout	Location	Description	Default
E98 	A4	Jump 1-2 to provide a 2.45MHz DCLK signal to DACs and ADCs. Jump 2-3 to provide a 1.22MHz DCLK signal to DACs and ADCs. Important for high accuracy A/D conversion on ACC-28. ***Note*** This also divides the phase and servo clock frequencies in half. See E29-E33, E3-E6, I10	1-2 Jumper installed

E100: Output Flag Supply Select

E Point & Physical Layout	Location	Description	Default
E100 	A3	Jump pin 1 to 2 to apply analog supply voltage A+15V to U37 flag output driver IC. Jump pin 2 to 3 to apply flag supply voltage OPT+V to U37 flag output driver IC.	1-2 Jumper installed

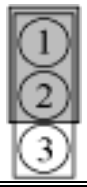
E101 - E102: Motors 1-4 Amplifier Enable Output Configure

E Point & Physical Layout	Location	Description	Default
E101 	A7	Jump pin 1 to 2 to apply A+15V/A+V (as set by E100) to pin 10 of U37 AENAn & EQUn driver IC (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply GND to pin 10 of U37 (should be UDN2981A for source output configuration). ***Caution*** The jumper setting must match the type of driver IC, or damage to the IC will result.	1-2 Jumper installed
E102 	A7	Jump pin 1 to 2 to apply GND to pin 10 of U37 AENAn & EQUn (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply A+15V/A+V (as set by E100) to pin 10 of U37 (should be UDN2981A for source output configuration). ***Caution*** The jumper setting must match the type of driver IC, or damage to the IC will result.	1-2 Jumper installed

E109: Reserved for Future Use

E Point & Physical Layout	Location	Description	Default
E109 	B6	For future use.	No jumper

E110: Serial Port Configure

E Point & Physical Layout	Location	Description	Default
E110 	A7	Jump pin 1 to 2 to use the J4 connector as RS-232. Jump pin 2 to 3 to use the J4 connector as RS-422.	1-2 Jumper installed

E111: Clock Lines Output Enable

E Point & Physical Layout	Location	Description	Default
E111 	A7	Jump pin 1 to 2 to enable the Phase, Servo and Init lines on the J4 connector. Jump pin 2 to 3 to disable the Phase, Servo and Init lines on the J4 connector. E111 on positions 1 to 2 is necessary for daisychained PMACs sharing the clock lines for synchronization.	1-2 Jumper installed

E119: WATCHDOG DISABLE JUMPER

E Point & Physical Layout	Location	Description	Default
E119 	B6	Jump pin 1 to 2 to disable Watchdog timer (for test purposes only). Remove jumper to enable Watchdog timer.	No jumper

E122: XIN Feature Selection

E Point & Physical Layout	Location	Description	Default
E122 	B6	Jump 2-3 to bring the Power Good signal into register XIN7 at Y:$E801 bit 7.	2-3 Jumper installed

PMAC PCI-LITE MATING CONNECTORS

This section lists several options for each connector. Choose an appropriate one for your application.

Base Board Connectors

J1 (JDISP)/Display

1. Two 14-pin female flat cable connector Delta Tau P/N 014-R00F14-0K0, T&B Ansley P/N 609-1441
2. 171-14 T&B Ansley standard flat cable stranded 14-wire
3. Phoenix varioface modules type FLKM14 (male pins) P/N 22 81 02 1

J2 (JPAN)/Control Panel

1. Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0, T&B Ansley P/N 609-2641
2. 171.26.T&B Ansley standard flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J3 (JTHW)/Multiplexer Port

1. Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0, T&B Ansley P/N 609-2641
2. 171-26 T&B Ansley standard flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J4 (JRS422)/RS232 OR 422/Serial Communications

1. Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0, T&B Ansley P/N 609-2641
2. 171-26 T&B Ansley standard flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J5 (JOPT)/OPTO I/O

1. Two 34-pin female flat cable connector Delta Tau P/N 014-R00F34-0k0, T&B Ansley P/N 609-3441
2. 171-34 T&B Ansley standard flat cable stranded 34-wire
3. Phoenix varioface module type FLKM 34 (male pins) P/N 22 81 06 3

J6 (JXIO)/Expansion Board

1. Two 10-pin female flat cable connector Delta Tau P/N 014-R00F10-0K0, T&B Ansley P/N 609-1041
2. 171-10 T&B Ansley standard flat cable stranded 10-wire
3. Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

J8 (JMACH)/Machine Connector

1. Two 60-pin female flat cable connector Delta Tau P/N 014-R00F60-0K0, T&B Ansley P/N 609-6041 available as ACC 8P or 8D
2. 171-60 T&B Ansley standard flat cable stranded 60-wire
3. Phoenix varioface module type FLKM 60 (male pins) P/N 22 81 09 2

Note

Normally, J8 is used with Acc-8P or Acc-8D with Option P, which provides complete terminal strip fan-out of all connections.

JS1/A-D Inputs 1-4

1. Two 16-pin female flat cable connector Delta Tau P/N 014-R00F16-0K0, T&B Ansley P/N 609-1641
2. 171-16 T&B Ansley standard flat cable stranded 16-wire
3. PHOENIX varioface module type FLKM 16 (male pins) P/N 22 81 03 4

JEQU/Position Compare

1. Two 10-pin female flat cable connector Delta Tau P/N 014-R00F10-0K0, T&B Ansley P/N 609-1041
2. 171-10 T&B Ansley standard flat cable stranded 10-wire
3. Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

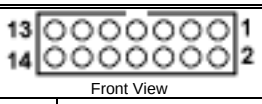
JANA/Analog Inputs Option

1. Two 20-pin female flat cable connector Delta Tau P/N 014-R00F20-0K0, T&B Ansley P/N 609-2041
2. 171-20 T&B Ansley standard flat cable stranded 20-wire
3. Phoenix varioface modules type FLKM20 (male pins)

PMAC PCI-LITE CONNECTOR PINOUTS

J1: Display Port Connector

J1 JDISP (14-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	VDD	Output	+5V power	Power supply out
2	VSS	Common	PMAC common	
3	RS	Output	Read strobe	TTL signal out
4	VEE	Output	Contrast adjust. Vee	0 to +5Vdc *
5	E	Output	Display enable	High is enable
6	R/W	Output	Read or write	TTL signal out
7	DB1	Output	Display Data1	
8	DB0	Output	Display Data0	
9	DB3	Output	Display Data3	
10	DB2	Output	Display Data2	
11	DB5	Output	Display Data5	
12	DB4	Output	Display Data4	
13	DB7	Output	Display Data7	
14	DB6	Output	Display Data6	

* Controlled by potentiometer R1.

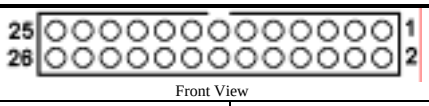
The JDISP connector is used to drive the 2 line x 24 character (Acc-12), 2 x 40 (Acc-12A) LCD, or the 2 x 40 vacuum fluorescent (Acc-12C) display unit. The **DISPLAY** command may be used to send messages and values to the display.

See:

Program Commands: DISPLAY
Accessories; ACC-12, 12A, 12C, ACC16D
Memory Map: Y:$0780 - $07D1

J2: Control Panel Port Connector

J2 JPAN (26-Pin Connector)



Front View

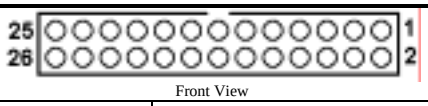
Pin #	Symbol	Function	Description	Notes
1	+5V	Output	+5V power	For Remote Panel
2	GND	Common	PMAC common	
3	FPD0/	Input	Motor/C.S. Select Bit 0	Low Is True
4	JOG-/	Input	Jog In - Dir.	Low Is Jog -
5	FPD1/	Input	Motor/C.S. Select Bit 1	Low Is True
6	JOG+/	Input	Jog In + Dir.	Low Is Jog +
7	PREJ/	Input	Return to prejog position	Low Is Return Equiv To J= Cmd
8	STRT/	Input	Start program run	Low Is Start Equiv To R Cmd
9	STEP/	Input	Step through program	Low Is Step Equiv To S Or Q
10	STOP/	Input	Stop program run	Low Is Stop Equiv To A
11	HOME/	Input	Home search command	Low Is Go Home Equiv To Hm
12	HOLD/	Input	Hold motion	Low Is Hold Equiv To H
13	FPD2/	Input	Motor/C.S. Select Bit 2	Low Is True
14	FPD3/	Input	Motor/C.S. Select Bit 3	Low Is True
15	INIT/	Input	Reset PMAC	Low Is Reset Equiv To $$$
16	HWCA	Input	Handwheel Encoder A Channel	5v Ttl Sq. Pulse Must Use E23 (Cha2)
17	IPLD/	Output	In Position Ind. (C.S.)	Low Lights Led
18	BRLD/	Output	Buffer Request Ind.	Low Lights Led
19	ERLD/	Output	Fatal Follow Err (C.S.)	Low Lights Led
20	WIPER	Input	Feed Pot Wiper	0 To +10v Input Must use E72, E73 Cha4)
21	(SPARE)	N.C.		
22	HWCB	Input	Handwheel Enc. B Channel	5v Ttl Sq. Pulse Must Use E22 (Chb2)
23	F1LD/	Output	Warn Follow Err (C.S.)	Low Lights Led
24	F2LD/	Output	Watchdog Timer	Low Lights Led
25	+5V	Output	+5V power	For Remote Panel
26	GND	Common	PMAC common	

The JPAN connector can be used to connect Acc-16 (Control Panel), or customer-provided I/O, to the PMAC, providing manual control of PMAC functions via simple toggle switches. If the automatic control panel input functions are disabled (I2=1), the inputs become general-purpose TTL inputs, and the coordinate system (C.S.) specific outputs pertain to the host-addressed coordinate system.

See Also:
Control panel inputs, Accessories: ACC-16, ACC-39
I-variables: I2, Ix06. I/O and Memory Map Y:$FFC0. Suggested M-variables M20 - M32

J3: Multiplexer Port Connector

J3 JTHW (26-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	GND	Common	PMAC Common	
2	GND	Common	PMAC Common	
3	DAT0	Input	Data-0 Input	Data input from multiplexed accessory
4	SEL0	Output	Select-0 Output	Multiplexer select output
5	DAT1	Input	Data-1 Input	Data input from multiplexed accessory
6	SEL1	Output	Select-1 Output	Multiplexer select output
7	DAT2	Input	Data-2 Input	Data input from multiplexed accessory
8	SEL2	Output	Select-2 Output	Multiplexer select output
9	DAT3	Input	Data-3 Input	Data input from multiplexed accessory
10	SEL3	Output	Select-3 Output	Multiplexer select output
11	DAT4	Input	Data-4 Input	Data input from multiplexed accessory
12	SEL4	Output	Select-4 Output	Multiplexer select output
13	DAT5	Input	Data-5 Input	Data input from multiplexed accessory
14	SEL5	Output	Select-5 Output	Multiplexer select output
15	DAT6	Input	Data-6 Input	Data input from multiplexed accessory
16	SEL6	Output	Select-6 Output	Multiplexer select output
17	DAT7	Input	Data-7 Input	Data input from multiplexed accessory
18	SEL7	Output	Select-7 Output	Multiplexer select output
19	N.C.	N.C.	No Connection	
20	GND	Common	PMAC Common	
21	BRLD/	Output	Buffer Request	Low is buffer req.
22	GND	Common	PMAC Common	
23	IPLD/	Output	In Position	Low is in position
24	GND	Common	PMAC Common	
25	+5V	Output	+5vdc Supply	Power supply out
26	INIT/	Input	PMAC Reset	Low is reset

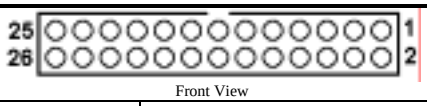
The JTHW multiplexer port provides eight inputs and eight outputs at TTL levels. While these I/O can be used in unmultiplexed form for 16 discrete I/O points, most users will utilize PMAC software and accessories to use this port in multiplexed form to greatly multiply the number of I/O that can be accessed on this port. In multiplexed form, some of the SELn outputs are used to select which of the multiplexed I/O are to be accessed.

See:

I/O and Memory Map Y:$FFC1
Suggested M-variables M40 - M58
M-variable formats TWB, TWD, TWR, TWS
ACC-8D Opt 7, ACC-8D Opt 9, ACC-18, ACC-34x, NC Control Panel

J4: Serial Port Connector

J4 JRS422 (26-Pin Connector)



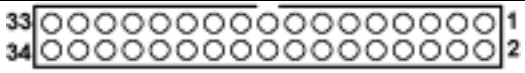
Front View

Pin #	Symbol	Function	Description	Notes
1	CHASSI	Common	PMAC Common	
2	S+5V	Output	+5Vdc Supply	Deactivated by E8
3	RD-	Input	Receive data	Diff. I/O low true **
4	RD+	Input	Receive data	Diff. I/O high true *
5	SD-	Output	Send data	Diff. I/O low true **
6	SD+	Output	Send data	Diff. I/O high true *
7	CS+	Input	Clear to send	Diff. I/O high true **
8	CS-	Input	Clear to send	Diff. I/O low true *
9	RS+	Output	Req. To send	Diff. I/O high true **
10	RS-	Output	Req. To send	Diff. I/O low true *
11	DTR	Bidirect	Data term read	Tied to DSR
12	INIT/	Input	PMAC Reset	Low is reset
13	GND	Common	PMAC Common	**
14	DSR	Bidirect	Data Set Ready	Tied to DTR
15	SDIO-	Bidirect	Special Data	Diff. I/O low true
16	SDIO+	Bidirect	Special Data	Diff. I/O high true
17	SCIO-	Bidirect	Special Ctrl.	Diff. I/O low true
18	SCIO+	Bidirect	Special Ctrl.	Diff. I/O high true
19	SCK-	Bidirect	Special Clock	Diff. I/O low true
20	SCK+	Bidirect	Special Clock	Diff. I/O high true
21	SERVO-	Bidirect	Servo Clock	Diff. I/O low true ***
22	SERVO+	Bidirect	Servo Clock	Diff. I/O high true ***
23	PHASE-	Bidirect	Phase Clock	Diff. I/O low true ***
24	PHASE+	Bidirect	Phase Clock	Diff. I/O high true ***
25	GND	Common	PMAC Common	
26	+5V	Output	+5Vdc Supply	Power supply out

The JRS422 connector provides the PMAC with the ability to communicate both in RS422 and RS232. In addition, this connector is used to daisychain interconnect multiple PMACs for synchronized operation.
Jumper E110 selects between RS-232 or RS-422 signal types.
Jumper E110 enables or disables the use of the Phase, Servo and Init lines.
* **Note:** Required for communications to an RS-422 host port.
** **Note:** Required for communications to an RS-422 or RS-232 host port.
*** **Note:** Output on card with E40-E43 all ON. Input on card with any of E40-E43 OFF. These pins permit full synchronization of multiple PMACs through sharing of phase and servo clocks. If synchronization is desired, these lines should be connected even if serial communications is not used.
See:
Serial Communications
Synchronizing PMAC to other PMACs

J5: I/O Port Connector

J5 JOPT (34-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	MI8	Input	Machine Input 8	Low is true
2	GND	Common	PMAC Common	
3	MI7	Input	Machine Input 7	Low is true
4	GND	Common	PMAC Common	
5	MI6	Input	Machine Input 6	Low is true
6	GND	Common	PMAC Common	
7	MI5	Input	Machine Input 5	Low is true
8	GND	Common	PMAC Common	
9	MI4	Input	Machine Input 4	Low is true
10	GND	Common	PMAC Common	
11	MI3	Input	Machine Input 3	Low is true
12	GND	Common	PMAC Common	
13	MI2	Input	Machine Input 2	Low is true
14	GND	Common	PMAC Common	
15	MI1	Input	Machine Input 1	Low is true
16	GND	Common	PMAC Common	
17	MO8	Output	Machine Output 8	Low-true (sinking); High-true (sourcing)
18	GND	Common	PMAC Common	
19	MO7	Output	Machine Output 7	Low-true (sinking); High-true (sourcing)
20	GND	Common	PMAC Common	
21	MO6	Output	Machine Output 6	Low-true (sinking); High-true (sourcing)
22	GND	Common	PMAC Common	
23	MO5	Output	Machine Output 5	Low-true (sinking); High-true (sourcing)
24	GND	Common	PMAC Common	
25	MO4	Output	Machine Output 4	Low-true (sinking); High-true (sourcing)
26	GND	Common	PMAC Common	
27	MO3	Output	Machine Output 3	Low-true (sinking); High-true (sourcing)
28	GND	Common	PMAC Common	
29	MO2	Output	Machine Output 2	Low-true (sinking); High-true (sourcing)
30	GND	Common	PMAC Common	
31	MO1	Output	Machine Output 1	Low-true (sinking); High-true (sourcing)
32	GND	Common	PMAC Common	
33	+V	Input/ Output	+V Power I/O	(+V = +5v to +24v) +5v out from PMAC, +5 to +24v in from external source, diode isolation from PMAC
34	GND	Common	PMAC Common	

This connector provides means for eight general purpose inputs and eight general purpose outputs. Inputs and outputs may be configured to accept or provide either +5 volt or +24 volt signals. Outputs can be made sourcing with an IC (U13 to UDN2981) and jumper (E1 & E2) change. E7 controls whether the inputs are pulled up or down internally. Outputs are rated at 100mA per channel.

J6: Auxiliary I/O Port Connector

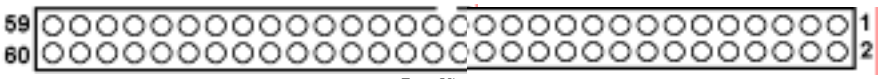
J6 JXIO (10-Pin Connector)

Front View

Pin #	Symbol	Function	Description	Notes
1	CHA1	Input	Enc. A Ch. Pos.	AXIS #1 for resolver
2	CHB1	Input	Enc. B Ch. Pos.	AXIS #1 for resolver
3	CHC1	Input	Enc. C Ch. Pos.	AXIS #1 for resolver
4	CHA3	Input	Enc. A Ch. Pos.	AXIS #3 for resolver
5	CHB3	Input	Enc. B Ch. Pos.	AXIS #3 for resolver
6	CHC3	Input	Enc. C Ch. Pos.	AXIS #3 for resolver
7	E63	Input	Interrupt IR4	Interrupt from EXP BRD
8	E59	Input	Interrupt IR5	Interrupt from EXP BRD
9	SCLK	Output	Encoder Clock	Encoder sample rate
10	DCLK	Output	D to A, A to D Clock	DAC and ADC clock for all channels

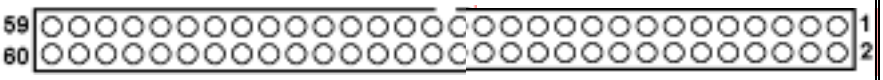
This connector is used for miscellaneous I/O functions related to expansion cards that are used with PMAC.

J8: Machine Port Connector

J8 JMACH (60-Pin Header)	 Front View			
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	+5V	Output	+5v power	For encoders, 1
2	+5V	Output	+5v power	For encoders, 1
3	GND	Common	Digital common	
4	GND	Common	Digital common	
5	CHC3	Input	Encoder C Ch. Pos	2
6	CHC4	Input	Encoder C Ch. Pos	2
7	CHC3/	Input	Encoder C Ch. Neg	2,3
8	CHC4/	Input	Encoder C Ch. Neg	2,3
9	CHB3	Input	Encoder B Ch. Pos	2
10	CHB4	Input	Encoder B Ch. Pos	2
11	CHB3/	Input	Encoder B Ch. Neg	2,3
12	CHB4/	Input	Encoder B Ch. Neg	2,3
13	CHA3	Input	Encoder A Ch. Pos	2
14	CHA4	Input	Encoder A Ch. Pos	2
15	CHA3/	Input	Encoder A Ch. Neg	2,3
16	CHA4/	Input	Encoder A Ch. Neg	2,3
17	CHC1	Input	Encoder C Ch. Pos	2
18	CHC2	Input	Encoder C Ch. Pos	2
19	CHC1/	Input	Encoder C Ch. Neg	2,3
20	CHC2/	Input	Encoder C Ch. Neg	2,3
21	CHB1	Input	Encoder B Ch. Pos	2
22	CHB2	Input	Encoder B Ch. Pos	2
23	CHB1/	Input	Encoder B Ch. Neg	2,3
24	CHB2/	Input	Encoder B Ch. Neg	2,3
25	CHA1	Input	Encoder A Ch. Pos	2
26	CHA2	Input	Encoder A Ch. Pos	2
27	CHA1/	Input	Encoder A Ch. Neg	2,3
28	CHA2/	Input	Encoder A Ch. Neg	2,3
29	DAC3	Output	Ana. Out pos. 3	4
30	DAC4	Output	Ana. Out pos. 4	4
31	DAC3/	Output	Ana. Out neg. 3	4,5
32	DAC4/	Output	Ana. Out neg. 4	4,5
33	AENA3/DIR3	Output	Amp-ENA/dir. 3	6
34	AENA4/DIR4	Output	Amp-ENA/dir. 4	6
35	FAULT3	Input	Amp-fault 3	7
36	FAULT4	Input	Amp-fault 4	7
37	+LIM3	Input	Neg end limit 3	8,9
38	+LIM4	Input	Neg end limit 4	8,9
39	-LIM3	Input	Pos end limit 3	8,9

J8: Machine Port Connector

J8 JMACH (60-Pin Header) Continued



Front View

Pin #	Symbol	Function	Description	Notes
40	-LIM4	Input	Pos End Limit 4	8,9
41	HMFL3	Input	Home-Flag 3	10
42	HMFL4	Input	Home-Flag 4	10
43	DAC1	Output	Ana. Out Pos. 1	4
44	DAC2	Output	Ana. Out Pos. 2	4
45	DAC1/	Output	Ana. Out Neg. 1	4,5
46	DAC2/	Output	Ana. Out Neg. 2	4,5
47	AENA1/DIR1	Output	Amp-ENA/Dir. 1	6
48	AENA2/DIR2	Output	Amp-ENA/Dir. 2	6
49	FAULT1	Input	Amp-Fault 1	7
50	FAULT2	Input	Amp-Fault 2	7
51	+LIM1	Input	Neg End Limit 1	8,9
52	+LIM2	Input	Neg End Limit 2	8,9
53	-LIM1	Input	Pos End Limit 1	8,9
54	-LIM2	Input	Pos End Limit 2	8,9
55	HMFL1	Input	Home-Flag 1	10
56	HMFL2	Input	Home-Flag 2	10
57	FEFCO/	Output	FE/Watchdog Out	Indicator/Driver
58	AGND	Input	Analog Common	
59	A+15V/OPT+V	Input	Analog +15v Supply	
60	A-15V	Input	Analog -15v Supply	

The J8 connector is used to connect PMAC to the first four channels (Channels 1, 2, 3, and 4) of servo amps, flags, and encoders.

Note 1: In standalone applications, these lines can be used as +5V power supply inputs to power PMAC's digital circuitry. However, if a terminal block is available on a version of PMAC, it is preferable to bring the +5V power in through the terminal block.

Note 2: Referenced to digital common (GND). Maximum of ± 12V permitted between this signal and its complement.

Note 3: Leave this input floating if not used (i.e., digital single-ended encoders). In this case, jumper (E18 - 21, E24 - 27) for channel should hold input at 2.5V.

Note 4: ± 10V, 10mA max, referenced to analog common (AGND).

Note 5: Leave floating if not used. Do not tie to AGND. In this case, AGND is the return line.

Note 6: Functional polarity controlled by jumper(s) E17. Choice between AENA and DIR use controlled by Ix02 and Ix25.

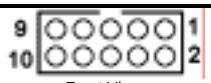
Note 7: Functional polarity controlled by variable Ix25. Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software. Automatic fault function can be disabled with Ix25.

Note 8: Pins marked *-LIMn* should be connected to switches at the positive end of travel. Pins marked *+LIMn* should be connected to switches at the negative end of travel.

Note 9: Must be conducting to 0V (usually AGND) for PMAC to consider itself not into this limit. Automatic limit function can be disabled with Ix25.

Note 10: Functional polarity for homing or other trigger use of HMFLn controlled by Encoder/Flag Variable 2 (I902, I907, etc.) HMFLn selected for trigger by Encoder/Flag Variable 3 (I903, I908, etc.). Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software.

J9 (JEQU): Position-Compare Connector

J9 JEQU (10-Pin Connector)			 Front View	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	EQU1/	Output	Enc. 1 comp-EQ	Low is true
2	EQU2/	Output	Enc. 2 comp-EQ	Low is true
3	EQU3/	Output	Enc. 3 comp-EQ	Low is true
4	EQU4/	Output	Enc. 4 comp-EQ	Low is true
5	EQU5/	Output	Amp enable 1	Low is true
6	EQU6/	Output	Amp enable 2	Low is true
7	EQU7/	Output	Amp enable 3	Low is true
8	EQU8/	Output	Amp enable 4	Low is true
9	A+V	Supply	Positive supply	+5v to +24v
10	AGND	Common	Analog ground	
This connector provides the position-compare outputs and the amplifier enable outputs for the four servo interface channels. The board is equipped with a ULN2803A or equivalent open-collector driver IC on U37. It may be replaced with UDN2891A or equivalent open-emitter driver (E101-E102 must be changed), or a 74ACT563 or equivalent 5V CMOS driver.				

J30 (JANA) Analog Input Port Connector (Optional)

Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	ANAI00	Input	Analog input 0	0-5v or +/-2.5v range
2	ANAI01	Input	Analog input 1	0-5v or +/-2.5v range
3	ANAI02	Input	Analog input 2	0-5v or +/-2.5v range
4	ANAI03	Input	Analog input 3	0-5v or +/-2.5v range
5	ANAI04	Input	Analog input 4	0-5v or +/-2.5v range
6	ANAI05	Input	Analog input 5	0-5v or +/-2.5v range
7	ANAI06	Input	Analog input 6	0-5v or +/-2.5v range
8	ANAI07	Input	Analog input 7	0-5v or +/-2.5v range
9	ANAI08	Input	Analog input 8	0-5v or +/-2.5v range [1]
10	ANAI09	Input	Analog input 9	0-5v or +/-2.5v range [1]
11	ANAI10	Input	Analog input 10	0-5v or +/-2.5v range [1]
12	ANAI11	Input	Analog input 11	0-5v or +/-2.5v range [1]
13	ANAI12	Input	Analog input 12	0-5v or +/-2.5v range [1]
14	ANAI13	Input	Analog input 13	0-5v or +/-2.5v range [1]
15	ANAI14	Input	Analog input 14	0-5v or +/-2.5v range [1]
16	ANAI15	Input	Analog input 15	0-5v or +/-2.5v range [1]
17	GND	Common	PMAC common	Not isolated from digital
18	+12V	Output	Pos. supply volt.	To power ext. Circuitry
19	GND	Common	PMAC common	Not isolated from digital
20	-12V	Output	Neg. supply volt	To power ext circuitry
The JANA connector provides the inputs for the eight or 16 optional analog inputs on the PMAC2. [1] Only present if Option-12A ordered.				

J31 (JUSB) Universal Serial Bus Port (Optional)

Pin #	Symbol	Function
1	VCC	N.C.
2	D-	Data-
3	D+	Data+
4	GND	GND
5	Shell	Shield
6	Shell	Shield

JS1: A/D Port 1 Connector

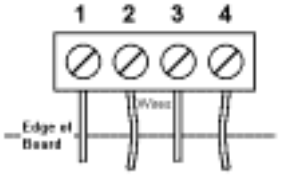
JS1 (16-Pin Header)

Front View

Pin #	Symbol	Function	Description	Notes
1	DCLK	Output	D to A, A to D Clock	DAC and ADC clock for chan 1, 2, 3, 4
2	BDATA1	Output	D to A Data	DAC data for chan 1, 2, 3, 4
3	ASEL0/	Output	Chan Select Bit 0	Select for chan 1, 2, 3, 4
4	ASEL1/	Output	Chan Select Bit 1	Select for chan 1, 2, 3, 4
5	CNVRT01	Output	A to D Convert	ADC convert sig. Chan 1, 2, 3, 4
6	ADCIN1	Input	A to D Data	ADC data for chan 1, 2, 3, 4
7	OUT1/	Output	Amp Enable/Dir	Amp enable/dir. for chan 1
8	OUT2/	Output	Amp Enable/Dir	Amp enable/dir. for chan 2
9	OUT3/	Output	Amp Enable/Dir	Amp enable/dir. for chan 3
10	OUT4/	Output	Amp Enable/Dir	Amp enable/dir. for chan 4
11	HF41	Input	Amp Fault	Amp fault input for chan 1
12	HF42	Input	Amp Fault	Amp fault input for chan 2
13	HF43	Input	Amp Fault	Amp fault input for chan 3
14	HF44	Input	Amp Fault	Amp fault input for chan 4
15	+5V	Output	+5v Supply	Power supply out
16	GND	Common	PMAC Common	

TB1 (JPWR) External Power Supply Connection

TB1 (JPWR)



Top View

Pin #	Symbol	Function	Description	Notes
1	GND	Common	Digital ground	
2	+5V	Input	+5v supply	Ref. to digital GND
3	+12V	Input	+12v to +15v supply	Ref. to digital GND
4	-12V	Input	-12v to -15v supply	Ref. to digital GND

This terminal block may be used as an alternative power supply connector if PMAC is not installed in a PCI-bus. The +5V powers the digital electronics. The +12V and -12V (if jumpers E85, E87, and E88 are installed) power the analog output stage. This defeats the optical isolation on PMAC.

To keep the optical isolation between the digital and analog circuits on PMAC, provide analog power (+/-12V to +/-15V & AGND) through the JMACH connector instead of the bus connector or this terminal block.