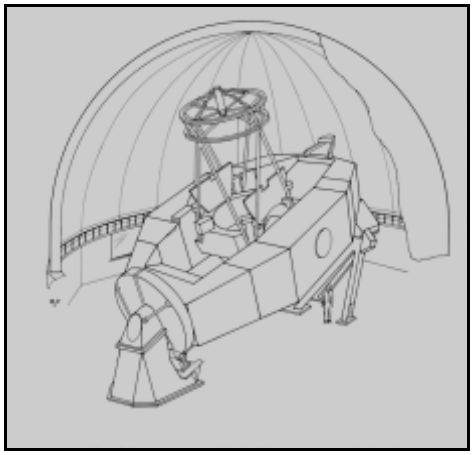
REV	DESCRIPTION	DATE	BY
-	Initial Release	3/27/08	EAW

T3-3002
Safety Board CPLD Programming Guide
Revision: -



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1 Programming Guide Overview

This programming guide will give all the steps to program the Safety Board CPLD. If any modifications are required to the CPLD logic, the main schematic used for this project may be modified and saved. Then, follow all steps outlined below.

Note: a simpler, programming only solution could have been employed, but since this is low, non-production type of programming, going through all the steps from the start using the schematic seems to be a more flexible approach that allows CPLD logic modification.

Also, the screen shots shown below may not match exactly depending on the version of the ISE software used, however, at the time of this document versions 9 and 10 were very similar in look an operation.

2 Equipment and Tools Required

The table below lists the equipment and tools required to complete programming.

Item #	Qty	Model / Part Number	Description
1	1	Xilinx ISE Software 10.1	Xilinx Software for Design & Programming
2	1	Xilinx DLC9 Platform Cable USB	TCS3 Lab System
3	1	+5V TCS3 Power Supply	+5V Power for Safety Board
4	1	Safety Board	Safety Board to be programmed
5	REF	Xilinx Safety Board ISE Project, Rev D	http://irtfweb.ifa.hawaii.edu/~tcs3/tcs3/Design/Safety_Board_CPLD/SB_CPLD_RevD.zip

Table 1 Required equipment

3 Explanation of Xilinx Project Files

Before continuing to the setup section, the required Xilinx ISE project files should be explained. There are many files that are created automatically when using Xilinx ISE and this can be confusing when first using the tool. Below are the required files for the project. Any other files present in the directory may be deleted if desired or can be ignored. All files are contained in the *main* directory, "Safety_Board_Rev_D", for example. All other subdirectories may be deleted or ignored. Rev D is used in the examples. If a higher revision exists, substitute that revision for Rev D.

File	Description
SB_WD.ise	Main Xilinx ISE project file.
Safety_brd_CPLD_schematic.sch	ISE Safety Board CPLD Logic Schematic file
logic_locked.ucf	CPLD pinout assignment & timing constraints
Rev_Block_Main.sym	Symbol for main rev block used in schematic.
Rev_Block.sym	Symbol for rev block used in schematic.
IFA_Title_Block.sym	Symbol for title block used in schematic.
cpld_all_scm.pdf	**NOT REQUIRED** Useful PDF of all design elements in Xilinx library for CPLD.

Table 2 Required Xilinx files.

4 Test Setup

Follow these steps to setup for programming:

1. Install Xilinx ISE Software if not already installed.

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2. Connect the Xilinx Platform Cable USB DLC9 to the PC via USB and to the Safety Board JTAG header via the ribbon cable (red dotted wire on ribbon represents pin #1).

3. Connect the +5V power supply to the Safety Board. Apply power.

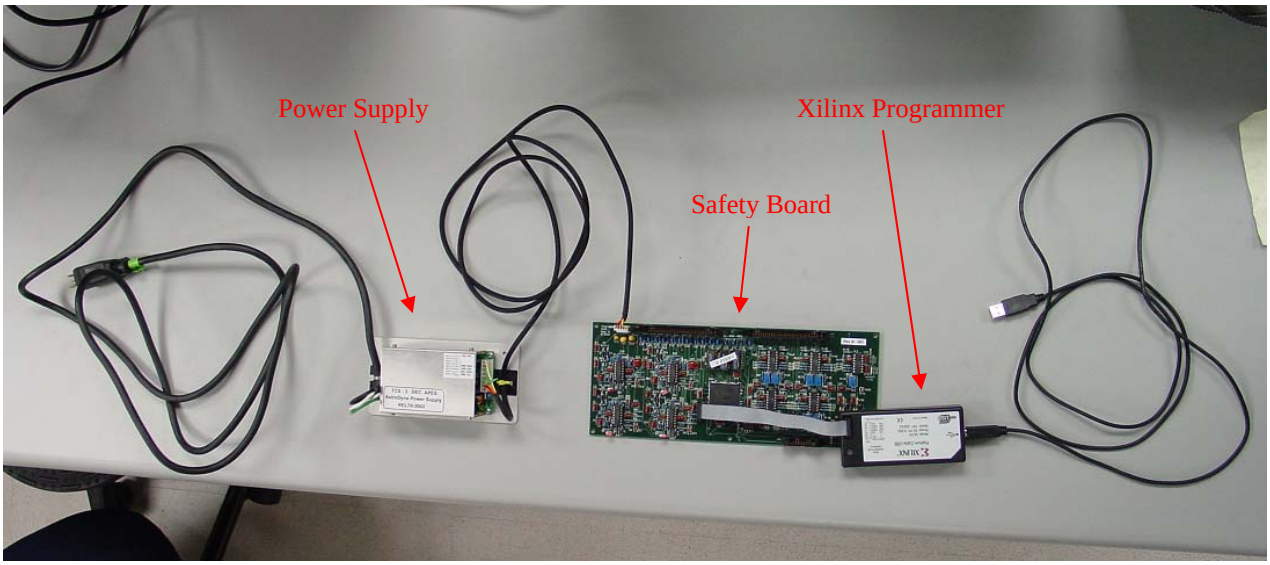

Figure 1 Hardware programming setup (Rev C Safety Board shown).

5 Programming

5.1 Start Xilinx ISE & Open Project

1. Start the Xilinx ISE software.

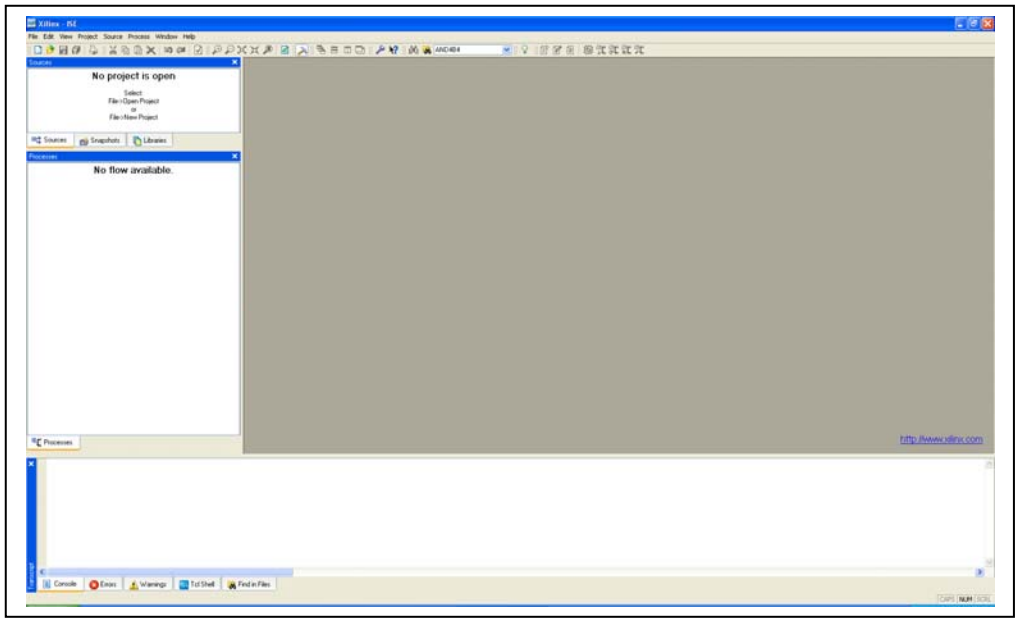

Figure 2 Xilinx ISE main window.

2. Open the Safety Board project, “Safety_Board_Rev_C.ise” using File->Open Project.

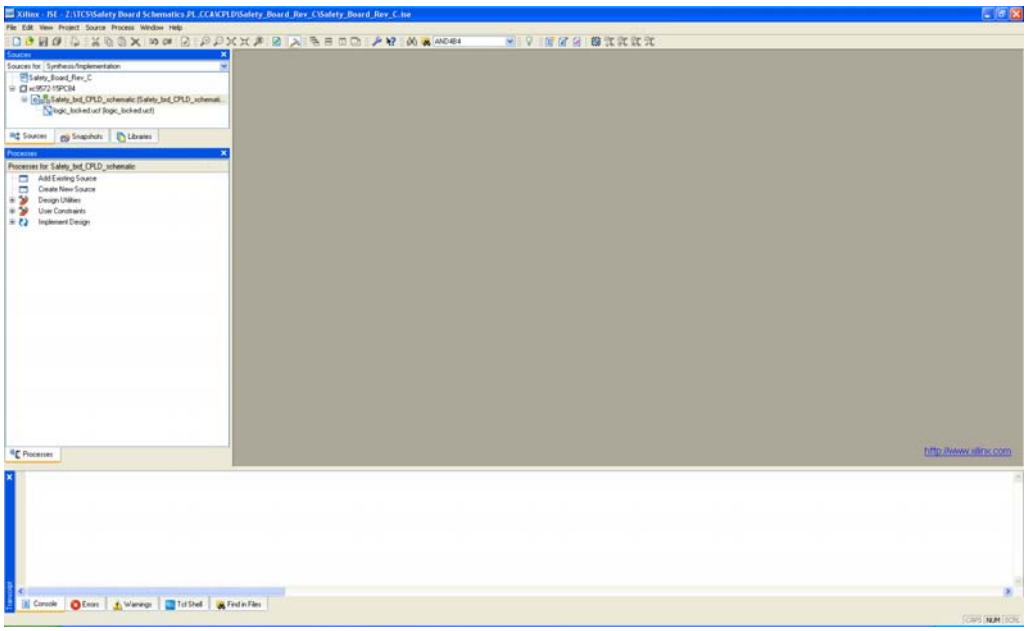

Figure 3 Xilinx ISE with project open.

5.2 Implement Design

1. Expand the “Implement Design” heading in the “Processes” window. Then expand the sub-heading “Generate Programming File”.

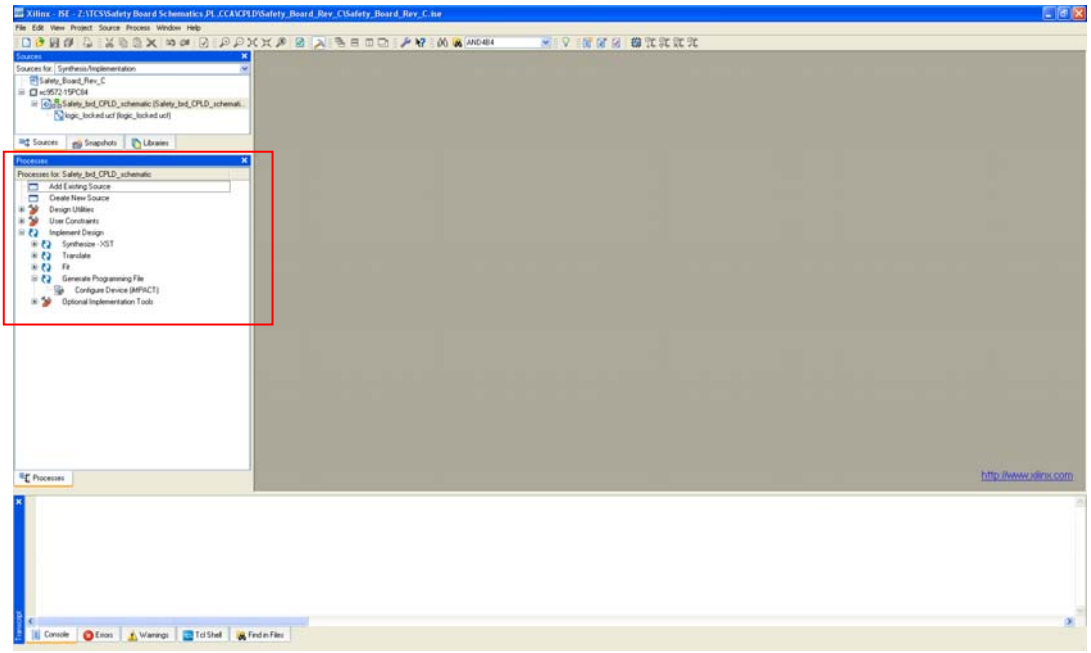

Figure 4 Expanded “Processes” window.

From the Processes menu, select (right click) Implement Design->Rerun All.

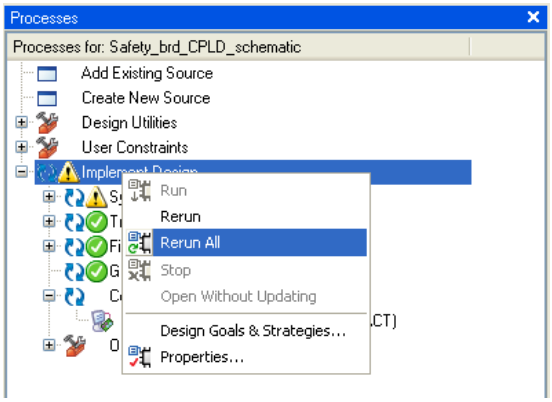

Figure 5 "Rerun All" command.

The blue arrows in the "Processes" window under "Implement Design" will begin to rotate. When the ISE tool is finished with the final step of generating the program file, the window will look similar to:

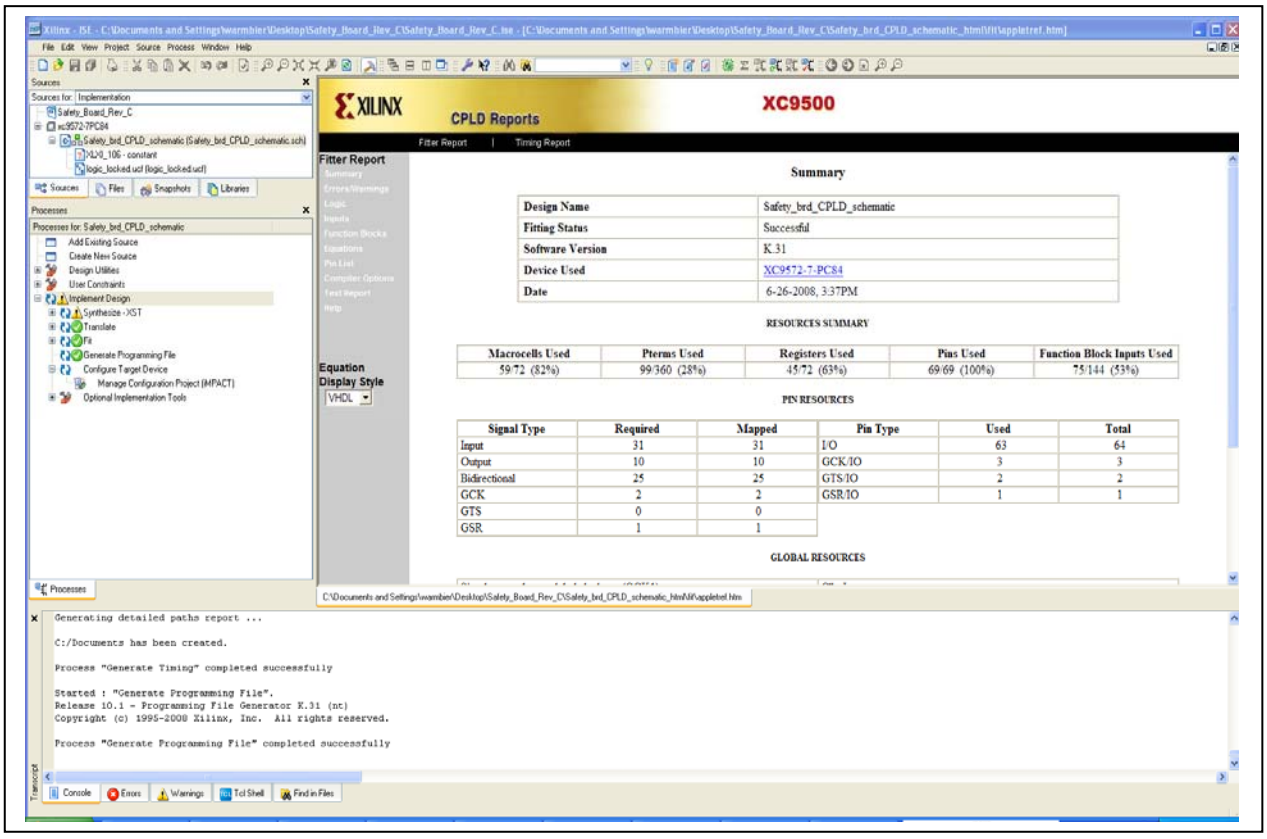

Figure 6 Implementation completion screen.

5.3 Programming the CPLD

1. Select (double click) on "Configure Device (IMPACT)" in the "Processes" window. Select "Configure devices using Boundary-Scan (JTAG)". Click Finish.

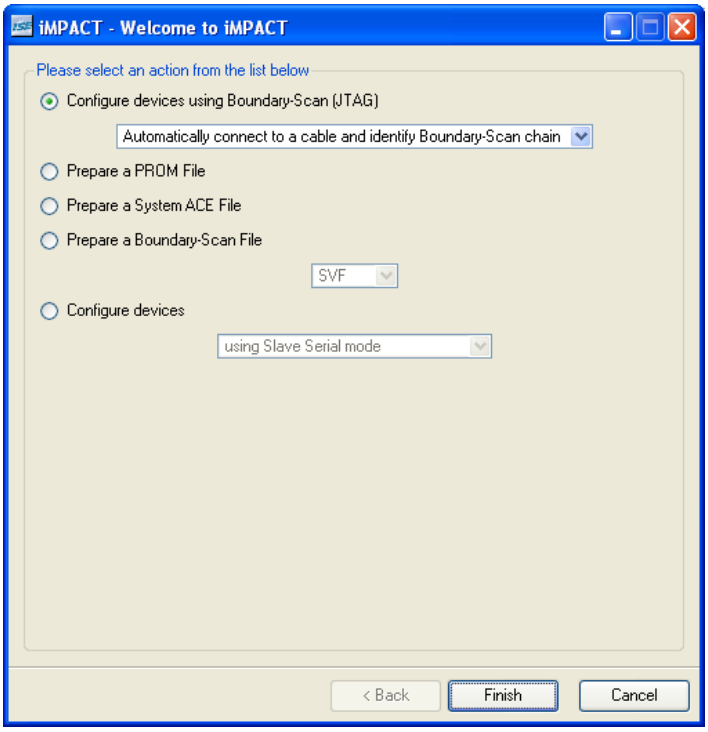

Figure 7 Programming iMPACT window.

2. A window will automatically pop up. Select "Safety_brd_CPLD_schematic.jed". This file was automatically created by ISE. Click Open.

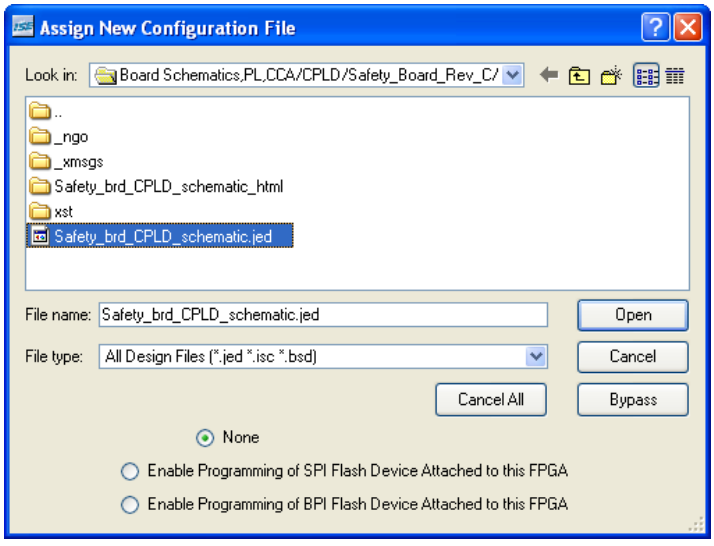

Figure 8 Assign configuration file.

The window will now look like:

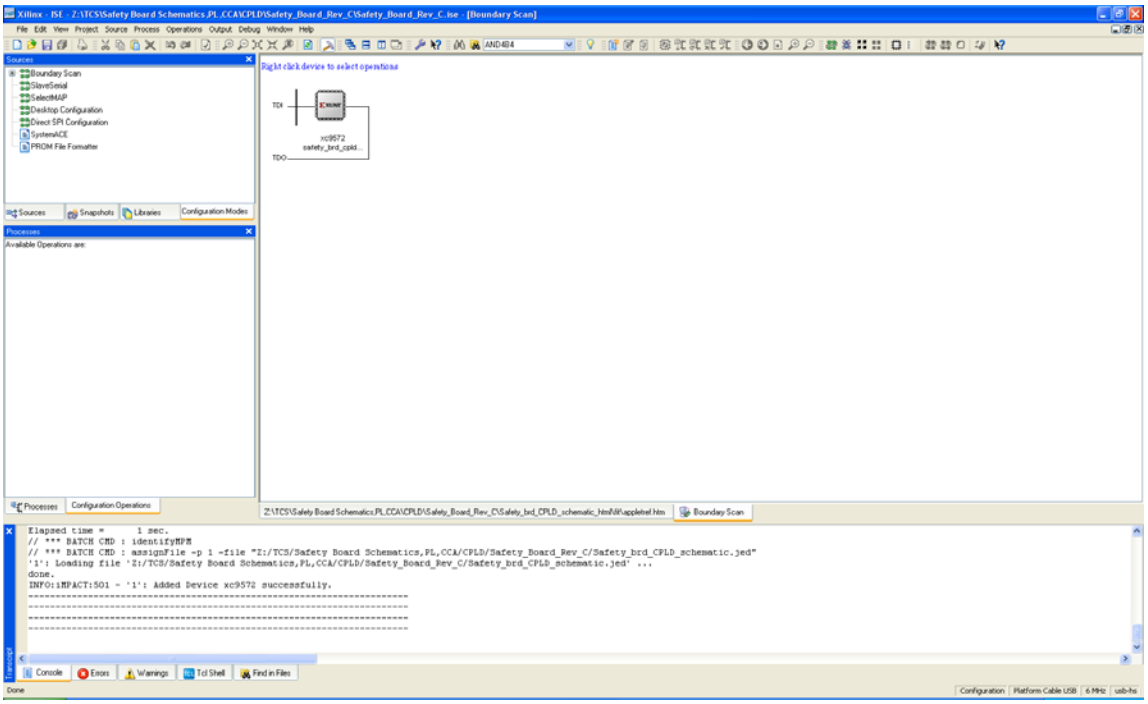

Figure 9 Main programming window.

3. Select “Program” via a right mouse click on the green graphic of the CPLD or under the “Processes” window.

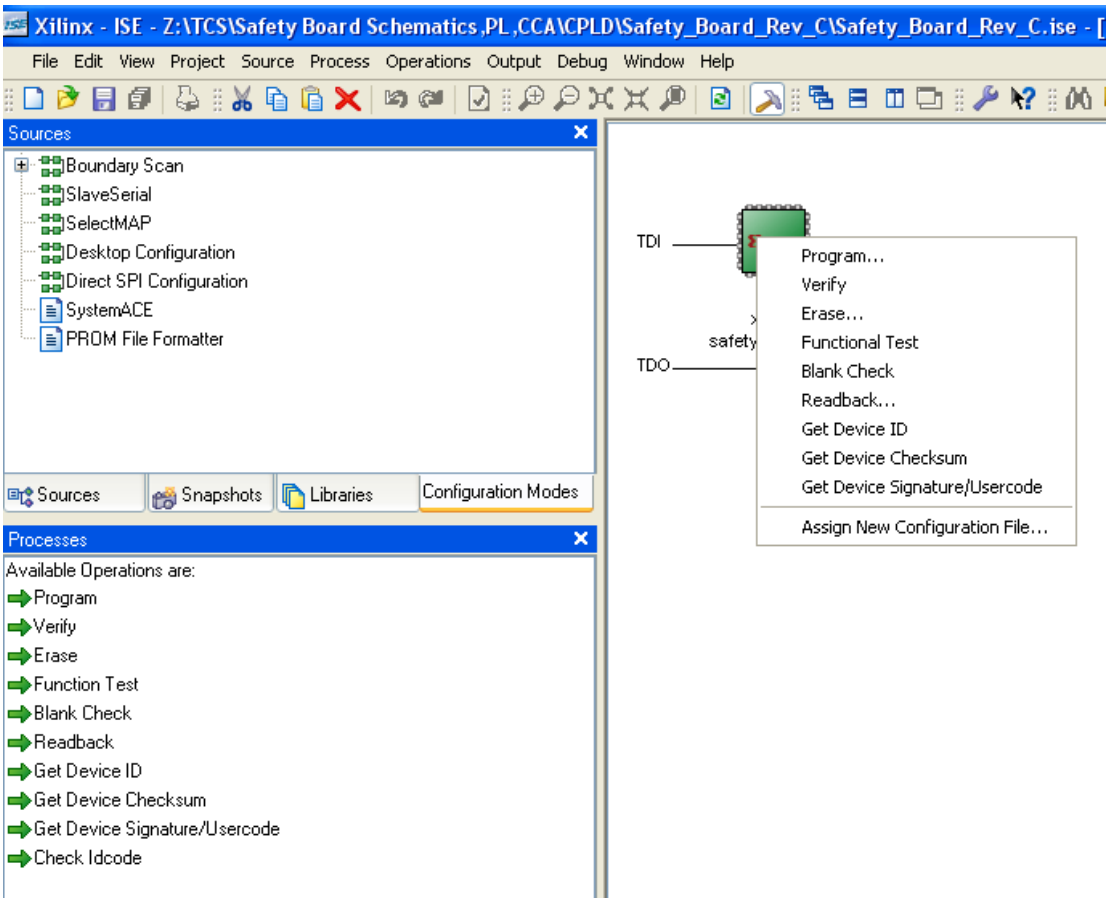

Figure 10 Process selection window.

4. Erase CPLD (optional). If the CPLD is new, it may not have write protection on. However, if this is a part that was previously programmed for the Safety Board, it will likely have write protect on. This requires a separate erase cycle. Select “Erase” via a right mouse click on the green graphic of the CPLD or under the “Processes” window.

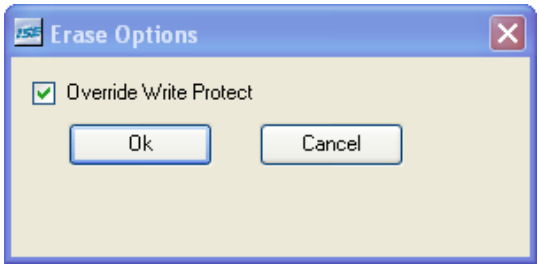

Figure 11 Erase Options window.

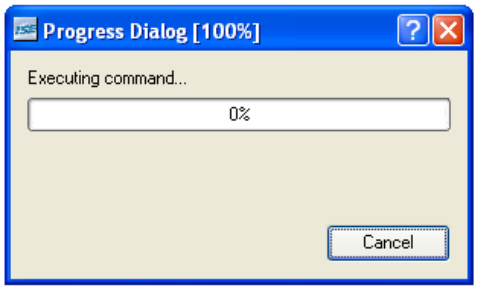

Figure 12 Erase progress window.

5. Select “Program” via a right mouse click on the green graphic of the CPLD or under the “Processes” window. From the window that pops up, select “Verify”, “Erase Before Programming”, and “Write Protect”.

   Note: “Write Protect” is used because as Xilinx states, “The write security bits provide added protection against accidental device erasure or reprogramming when the JTAG pins are subject to noise, such as during system power-up.”

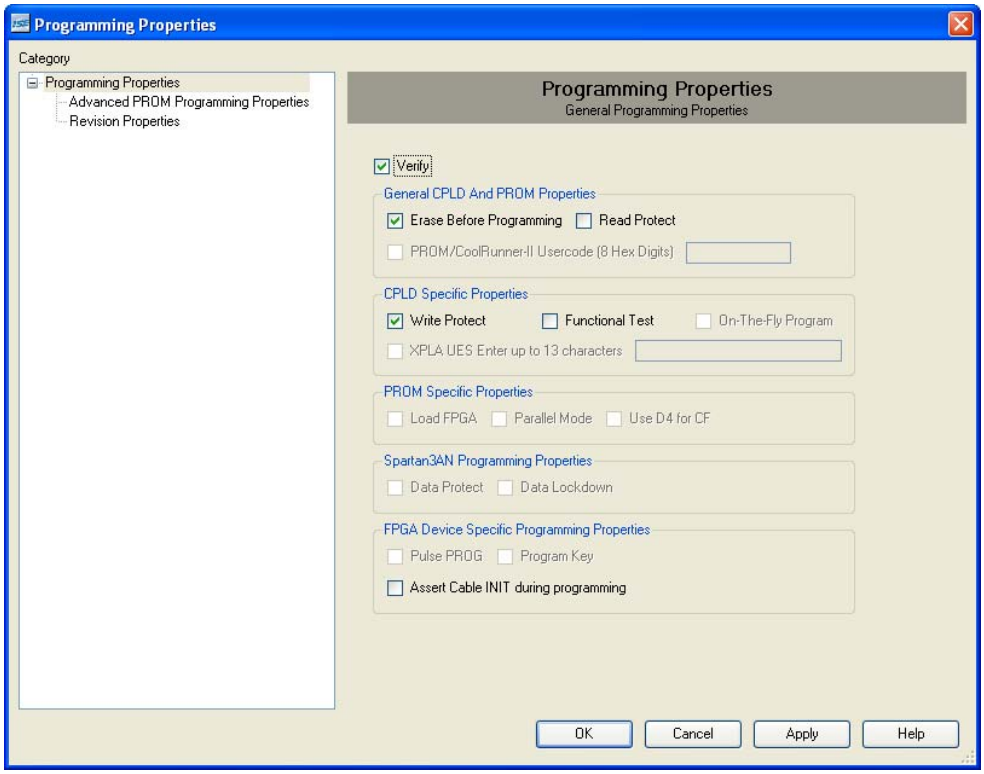

Figure 13 Programming Properties window.

A progress window will pop up.

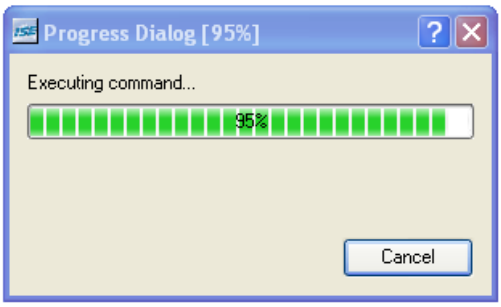

Figure 14 Programming progess window.

Upon completion, the “Transcript” window should have an indication that says “Programming completed successfully”.

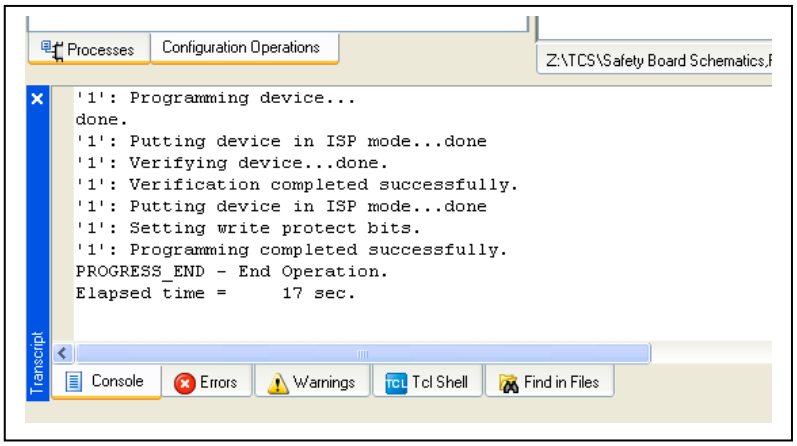

Figure 15 Transcript window.

6 Completion

The CPLD is now programmed. Power down the +5V supply and disconnect the programmer. The Safety Board must now be tested using the Safety Board Test Procedure before it is to be used in the IRTF TCS.

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